PERFORMANCE AND ANALYSIS OF ULTRA DEEP SUB MICRON TECHNOLOGY USING COMPLEMENTRY METAL OXIDE SEMICONDUCTOR INVERTER

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ABSTRACT

CMOS technology had attained remarkable to progress and advances thus this progress had been achieved by certain downsizing of the MOSFETs. The dimension of the MOSFETs were scaled upon by factor which has historically found to be 0.7 in very large scale integration technology, power and delay analysis have become crucial design concern. tn this paper we emphasize the comparative study of delay, average power and leakage power of CMOS inverter in Ultra Deep Submicron Technology range. This study shows variation of following as follows by delay to UDSM technology and also for average power and leakage power by diminishing to certain technology. The simulation results are taken for 45nm in Ultra Deep Submicron Technology range with the help of Cadence Tool and also analyzing the effect of load capacitance, transistor width and supply voltage on average power and delay of CMOS inverter of 45nm technology. Therefore the analysis has done with the aim to observe about the certain variation in delay and power with variation in transistor width in UDSM CMOS inverter and also had variation in load capacitance and supply voltage had been studied

KEYWORDS

UDSM, CMOS Inverter, Average Power, Delay, Leakage Power.

1. INTRODUCTION

The performance of the circuit can be enhanced by scaling MOSFETs to smaller dimension, which also reduces the space complexity. The dimension normally refers to the channel length of the transistor. The key process that defines the minimum dimension in a technology, eventually led to channel length below 1 urn, referred to submicron era. After this we had gone another scaling limit and will below .35um barrier, referred to Deep submicron (DSM) era. Scaling continued its relentless pace and then we entered a new era, where the minimum features of MOSFETs are being shifted to dimension below Deep submicron, so called Ultra Deep Submicron (UDSM) technology. The important challenges in this generation of IC designing is the increase in power dissipation in the circuit which reduces the battery -power, it also effect the reliability of the circuit due to interconnect aging process and accelerated device.[I] The major

advantage of power analysis is the battery life of equipment is directly related to power dissipation. Delay analysis also has importance in synthesis of VLSI design. Integrated circuit designer have constantly sought accurate and effect delay evaluation technique that will variety of option and better utilize the design space [2]. There are different secondary effects like body bias effect, channel length modulation effect, velocity saturation effect, drain induced barrier lowering (DIBL) etc which will modify power and delay models [3]. The most popular delay model in DSM range is described I nth power law [4]. , Where velocity saturation is main consideration. This paper represents simulation of CMOS inverter by considering MOSFET's channel length 45nm technology for UDSM range. The result shows how the leakage power, average power and delay depend on different design parameter for DSM and UDSM technology.

This paper organized in such a way that, after the description of UDSM technology MOSFET in section I, section II and section III contain brief description of delay and power modelling of CMOS Inverter. Simulation results and analysis are mentioned in section IV; section V includes summary and conclusion.

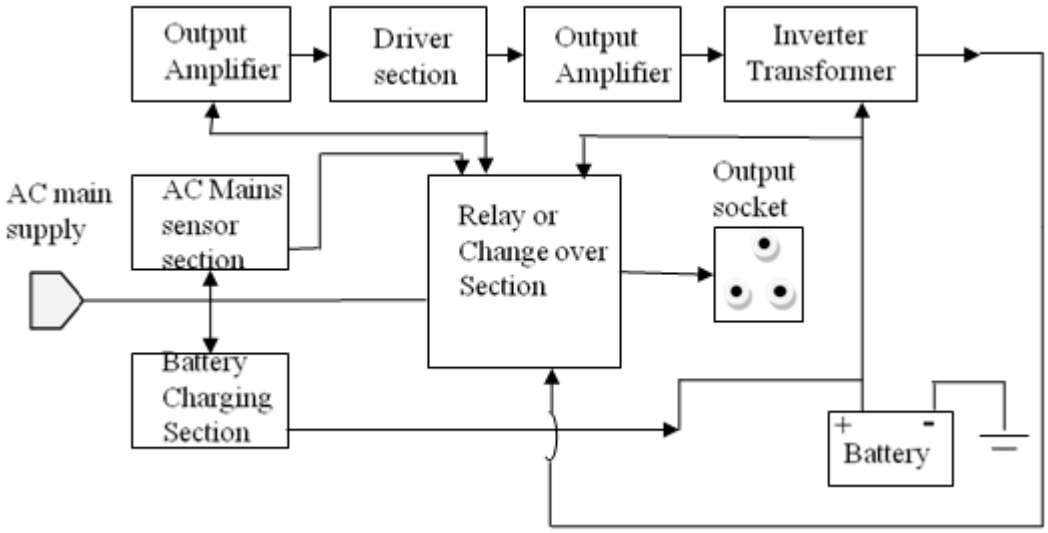

Figure 1: Block diagram of inverter

2. DELAY EXPRESSION FOR CMOS CIRCUIT

Using nth power law [4], the delay model of CMOS inverter can be derived. This equation implies for both fast input case and slow input case. The critical transition time to for input

$$t_{TO}=\frac{Cc\,Vdd}{2Ido}\;\frac{(n+1)(1-vt)^{n}}{(1-vt)^{n+1}-(Vv-Vt)^{n+1}} \quad (1)$$

Where Vv = $V_{INV/}$ V_{DD} and V_{v} = $V_{TO}/V_{DD.}$ Then the delay $t_{d,}$ the delay from 0.5 V_{DD} of input to 0.5 V_{DD} of output and the effective transition time tout can be expressed as follows tout can be used as for next logic gate.

($t_o \leq t_{TO}$; for faster input)

$$t_d = t_T \left\{\frac{1}{2} - \frac{1-V_T}{n+1} + \frac{(V_v - V_t)^{n+1}}{(n+1)(1-Vt)^n}\right\} + \frac{1}{2}\frac{C_o V_{DD}}{ID_O} \quad (2)$$

$$t_{out} = \{\frac{C_O\, V_{DD}\, v_{DO^2}}{0.7I_{do}(4V_{DO}-1)}\} \quad (3)$$

(t_t for slower input)

$$t_d = t_T[v_t - \frac{1}{2} + \{(v_v - v_T)^{n+1} + \frac{(n+1)(1-V_T)^n}{2t_T \frac{I_{DO}}{C_O V_{DD}}}\}^{\frac{1}{n+1}} \quad (4)$$

$$t_{out} = \{\frac{c_o v_{DD}}{0.71D_O}(\frac{1-V_T}{\frac{t_d}{t_T} - \frac{1}{2-V_T}})^n\} \quad (5)$$

Where n = velocity saturation index, Co is an output capacitance and $V_{DD} = d_o/V_{DD}$.

3. POWER DISSIPATION IN CMOS INVERTER

The average power over the interval is

$$p_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\, dt \quad (6)$$

Where E is the energy consumed over some time interval T is the integral of instaneous power

$$E = \int_0^T i_{DD}(t)V_{DD}dt \quad (7)$$

P (t) is the instantaneous power drawn from power supply is proportional to supply current i(t) is supply voltage V_{DD}

$$P(t) = i(t)V_{DD} \quad (8)$$

In CMOS inverter circuit, three types of power dissipation occur.

A. Leakage power dissipation

When static current flows from V_{DD} to ground node, without degrading inputs are called leakage power and the main components of leakage power in the OFF state at band to band tunneling, sub-threshold leakage (I_{sub}), gate induced drain leakage, gate tunneling leakage.

B. Short circuit power

From α-power law [6], the short circuit power dissipation model is

$$P_{sht.ckt.power} = V_{DD}t_T I_{DO}\frac{1}{\alpha+1}\frac{1}{2^{\alpha-1}}\frac{(1-2V_t}{(1-V_T)^\alpha} \quad (9)$$

Where $V_T = V_{TH}/V_{DD}$

C. Dynamic power dissipation

$D_{ynamic} = \alpha c_L V_{DD}^2 f$ Where α is switching activity factor of gate.

4. SIMULATION RESULT AND DISCUSSION

Simulation is performed in Cadence tool using Virtuoso analog design environment (ADE), for 45nm technology. This paper emphasize on delay, leakage power and average of CMOS inverter for 45nm technology. Simulation results are obtained from technology by taking input signal pulse having rise time (t_r) = lns, initial delay (t_d) = 0ns, pulse width= 10ns, time period= 20ns, wp = win = 2wn with this consideration, we compare our result by varying supply voltage for 45nm CMOS inverter thus it can be observed that the delay time decreases with increase in width of PMOS in 45nm technology. The table drawn below, shows how the average power, delay and leakage power changes, with the variation in supply voltages, in both 45nm technology CMOS inverter.

From, the table 1 it can be observed that the delay time decreases with the increase in supply voltage and as the delay decreases. In case of average power and leakage power as the supply voltage increases, then the average power and leakage power increases. As the technology shrinks, the leakage power increases and average power decreases

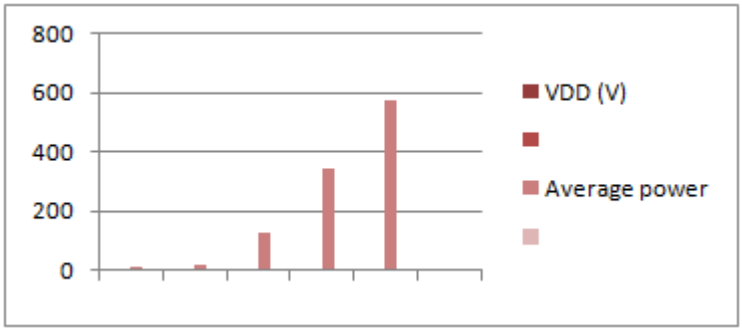

Figure 2: Average power with the variation of supply voltage

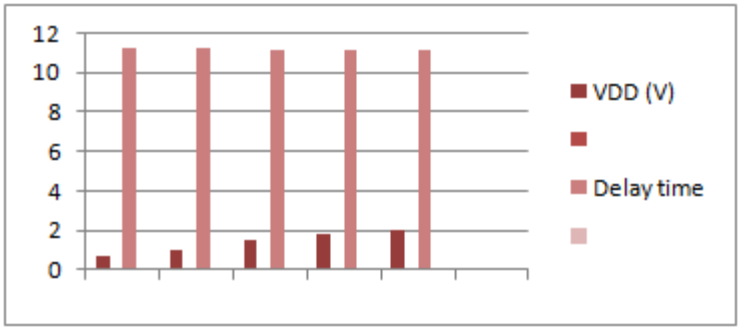

Figure 3: Delay time with the variation of supply voltage

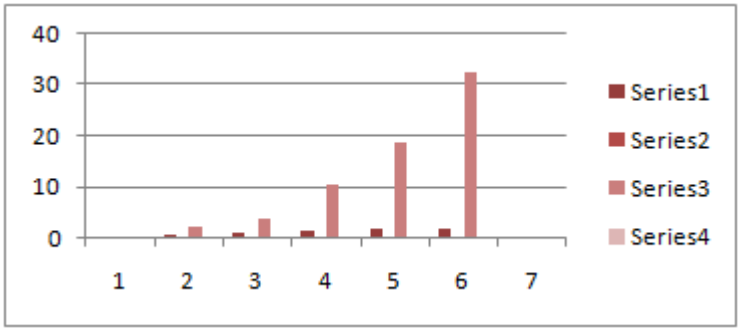

Figure 4: Leakage power with variation of supply voltage

The table drawn below, shows how the average power, delay and leakage power changes, with the variation in supply voltages, in 45nm technology CMOS inverter.

Table 1: Average power, Leakage power and Delay time relate with supply voltage.

VDD (V)	Average power (P_{avg} in nw)	Delay Time ($t_{in\ ns}$)	Leakage Power (P_{IKg} in pw)
0.7	10.55	11.28	2.31
1	23.06	11.20	3.92
1.5	126.4	11.18	10.58
1.8	345.0	11.17	18.69
2	573.9	11.15	32.50

5. CONCLUSION

This paper includes UDSM technology in terms of delay, leakage power and average power using CMOS inverter and analyzes how load capacitance, width of transistor and supply voltage effect on average power and delay in 45nm technology. It has been noticed from simulation result that, in 45nm technology, the average power and delay reduces. So, it has been observed that when the channel length less than or equal to 10nm then output waveform are not appeared because the channel length in this range size is below atomic width, which puts the limitation in nano range.

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