# DYNAMIC FLOATING OUTPUT STAGE FOR LOW POWER BUFFER AMPLIFIER FOR LCD APPLICATION

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***ABSTRACT***

*This topic proposes low-power buffer means low quiescent current buffer amplifier. A dynamic floating current node is used at the output of two-stage amplifier to increase the charging and discharging of output capacitor as well as settling time of buffer. It is designed for 10 bit digital analog converter to support for LCD column driver it is implemented in 180 nm CMOS technology with the quiescent current of 5 μA for 30 pF capacitance, the settling time calculated as 4.5μs, the slew rate obtained as 5V/μs and area on chip is* $30\times72\mu m^2$.

***KEYWORDS***

*Liquid crystal display (LCD) ,column driver, row driver, gamma correction, class AB output stage*

## 1. INTRODUCTION

With increasing demand of low-power portable LCD panel there was hard-core research to develop it as with the low-power means we have to decrease the static loss of the component or the blocks used in the driving scheme of the LCD panel, the driving scheme of LCD panel is shown in figure 1, which consists of source driver circuits (column driver), gate driver circuits(row driver), the reference voltages, timing controller's, gamma correction circuits, column driver is used to drive a pixel with required colored information and row driver used to refresh a pixel which required refreshing rate.[1,2] The column driver as shown in fig.2 contains input registers, shift registers, level shifters, digital to analog converter and buffer amplifiers. The column driver which is important to achieve the high resolution, high-speed, and low power dissipation among these output buffers is the key to determine the speed, resolution, and power consumption each pixel is derived by a buffer amplifier which is either positive polarity or negative polarity to drive the alternate pixel.

DOI : 10.5121/vlsic.2015.6102 

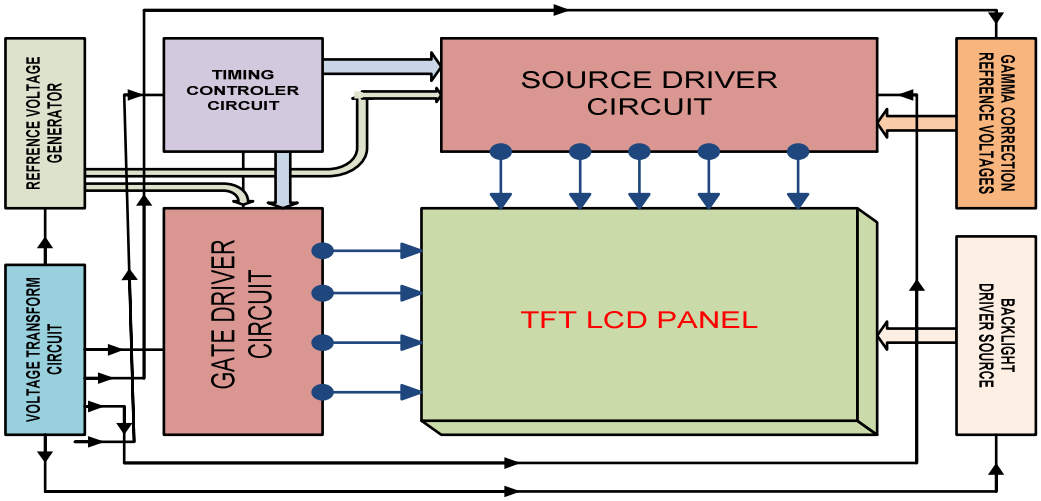


Fig 1.Block diagram of LCD panel

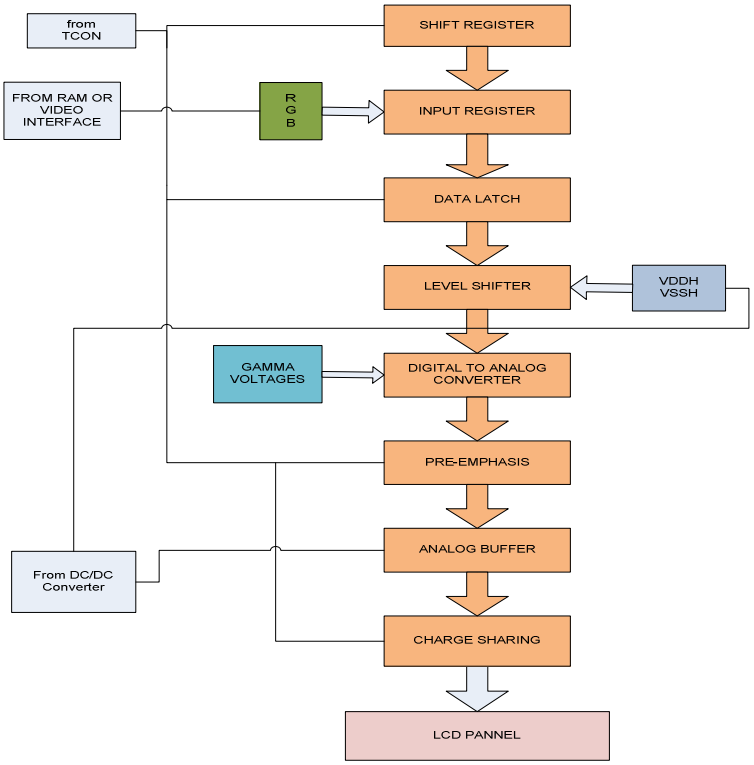


Fig 2.Column driver architecture of LCD

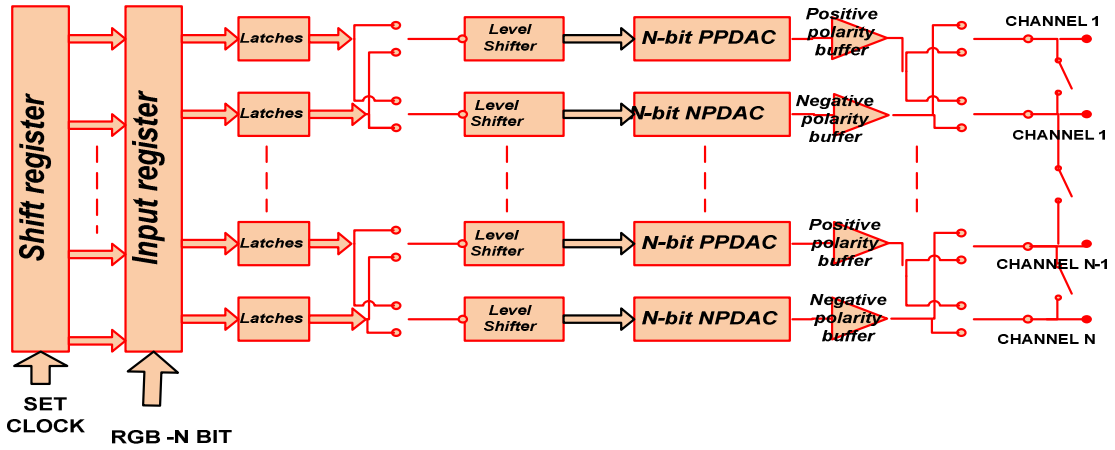


Fig 3.Architecture of an R_DAC based column

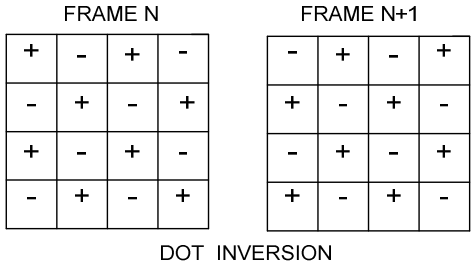


Fig 4. Dot inversion method to drive

There are four driving schemes for LCD panels these are row inversion, column inversion, frame inversion and dot inversion method, dot inversion method is best to drive a particular pixel to remove cross talk figure.4 shows its driving scheme adjacent pixel is driven by either a positive polarity buffer or by negative polarity buffer with due respect to common voltage, this will improve the lifetime of the liquid crystal.[3],[4],[5].The figure.4 shows a driving method of column driver to drive a pixel each adjacent pixels are driven by positive and negative polarity buffer [8-11].

In proposed buffer amplifier a single buffer which contain NMOS & PMOS differential pair, PMOS buffer has large discharge capability and NMOS has large charge capability are used to drive the adjacent pixel to follow the dot inversion technique. A floating output stage is used to control the biasing current of output stage using aspect ratio of MOS used in output stage.

## 2. FREQUENCY ANALYSIS OF TWO STAGE BUFFER

To drive high capacitive and resistive load of the pixel a class AB output stage is best suited for the column driver line. For low offset voltage we need high open loop gain of buffer amplifier, two-stage amplifier are generally used to drive the pixel, amplifier requires compensation capacitor for the stability as the phase margin of the operation amplifier depend upon the compensation capacitor, the slew rate is also depends on compensation capacitor. As some buffers adopt output node to get the stability without using Miller capacitance, some uses charge

conservation technique to reduce the dynamic power loss without Miller capacitance. These buffer suffers from charge storage problem as during scanning off time of row driver's the columns lines are for a small duration of time is isolated from the pixels to refresh formation at buffer quickly, so we need a capacitor which is fulfilled by compensation capacitor so those buffers which are without compensation capacitors have a problem that they can't refresh there information within the refresh time. As the proposed buffer has two-stage with the Miller capacitor for the compensation is used in design. The figures.5 shows the equivalent circuit of two stage operational amplifier with output load resistance and capacitance.

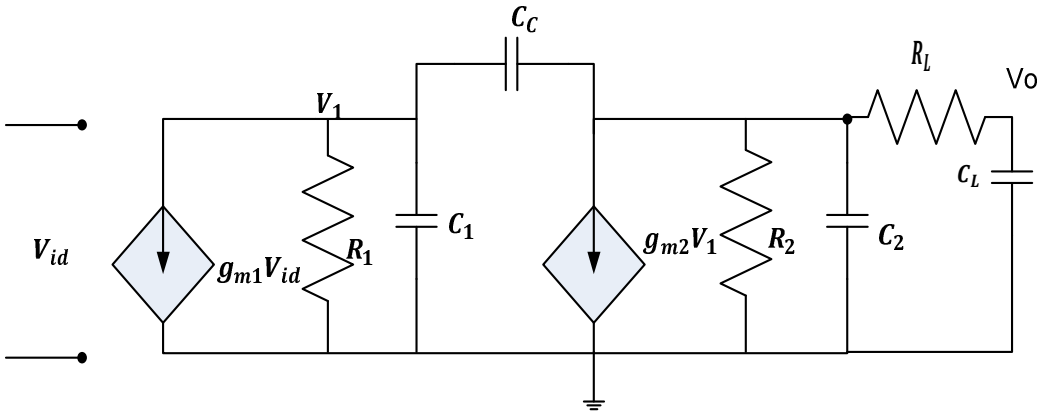


Fig 5. Small signal model of proposed buffer amplifier

Figure 5 shows small signal equivalent diagram of proposed amplifier for two stage under open loop, $g_{m1}$ & $g_{m2}$ are the transconductance, $R_1$ & $R_2$ are the output resistance, $C_1$ & $C_2$ are the open loop parasitic capacitance of the first and second stages, $C_c$ is the miller capacitance for phase compensation and $R_L$& $C_L$are the resistive and capacitive load.

The transfer function of the amplifier is calculated using current equation:-

using current equation at input node:

$$g_{m1}V_{id} + \frac{V_1}{R_1} + SC_1V_1 + (V_1 - V_0)SC_C = 0$$

$$V_1\left[\tfrac{1}{R_1} + S(C_1 + C_C)\right] = SV_0C_C - g_{m1}V_{id} \qquad (1)$$

using current equation at output node:

$$g_{m2}V_1 + \frac{V_0}{R_2} + SC_2V_0 + (V_0 - V_1)SC_C + \frac{V_0}{\left(R_L + \frac{1}{SC_L}\right)} = 0$$

$$V_0\left[\frac{1}{R_2} + S(C_1 + C_C) + \frac{SC_L}{1 + SR_LC_L}\right] = V_1(SC_C - g_{m2}) \qquad (2)$$

Put value of $V_1$from equation 1 to equation 2 we get,

$$\frac{V_0}{V_{id}} = \frac{g_{m1}g_{m2}R_1R_2\left(1-\frac{SC_C}{g_{m2}}\right)(1+SR_LC_L)}{1+A_1S+A_2S^2+A_3S^3} \qquad (3)$$

$$A_1 = R_1(C_1+C_C)+R_LC_L+R_2(C_2+C_C)+C_LR_2+R_1R_2g_{m2}C_C$$

$$A_2 = R_1R_LC_L(C_1+C_C)+R_1R_2(C_1+C_C)(C_2+C_C)+R_1R_2C_L(C_1+C_C)+C_LR_LR_2(C_2+C_C) + R_1R_2C_C[C_C-(C_1+C_C)g_{m2}R_1]$$

$$A_3 = R_1R_2R_LC_L(C_1+C_C)(C_2+C_C)+{R_1}^2R_2{C_C}^2(C_1+C_C)$$

As from equation 3 it show 3rd order transfer function

$$A_0(S) = \frac{A_{dc}\left(1+\frac{S}{\omega_{Z1}}\right)\left(1+\frac{S}{\omega_{Z2}}\right)}{\left(1+\frac{S}{\omega_{P1}}\right)\left(1+\frac{S}{\omega_{P2}}\right)\left(1+\frac{S}{\omega_{P3}}\right)}$$

to solve the 3rd order transfer function using dominant pole concept, the characteristic equation is written as:

$$1+A_1S+A_2S^2+A_3S^3=0$$

$$\approx A_1S+A_2S^2+A_3S^3=0$$

$$\approx A_1S\left(1+\frac{A_2}{A_1}S+\frac{A_3}{A_1}S^2\right)=0$$

$$\omega_{P1} \cong -\frac{1}{A_1}$$

$$\omega_{P2} \cong \frac{A_1}{A_2}$$

$$\omega_{P3} = \frac{1}{P_2}\frac{A_1}{A_2}$$

$$A_{dc} = g_{m1}g_{m2}R_1R_2$$

$$\omega_{P1} \cong \frac{1}{R_1R_2g_{m2}C_C+C_LR_2}$$

$$\omega_{P2} \cong \frac{1}{[(C_1+C_C)R_L]}$$

$$\omega_{P3} \cong \frac{g_{m2}C_C + {C_L}/{R_1}}{C_C C_L}$$

$$\omega_{Z1} = \frac{-g_{m2}}{C_C} \text{ and } \omega_{Z2} = \frac{1}{R_L C_L}$$

the unity gain frequency($\omega_t$)= $A_{dc}\,\omega_{P1}$

$$\omega_t = \frac{g_{m1}g_{m2}}{C_C g_{m2} + {C_L}/{R_1}}$$

taking 3rd pole very far away from unity gain bandwidth so it does not affect the phase margin so $\omega_{Z2}$ will compensate for $\omega_{P3}$ so the transfer function act like 2nd order transfer function,

$$A_0(S) = \frac{A_{dc}\left(1 + \frac{S}{\omega'_{Z1}}\right)}{\left(1 + \frac{S}{\omega'_{P1}}\right)\left(1 + \frac{S}{\omega'_{P2}}\right)}$$

where $\omega'_{Z1} = \frac{-g_{m2}}{C_C}$

$$\omega'_{P1} \cong \frac{1}{R_1 R_2 g_{m2} C_C}$$

$$\omega_{P2} \cong \frac{g_{m2}}{[C_2]}$$

Phase margin of the amplifier is as:

$$< A_0(S) = tan^{-1}\left(\frac{\omega}{\omega'_{Z1}}\right) - tan^{-1}\left(\frac{\omega}{\omega'_{P1}}\right) - tan^{-1}\left(\frac{\omega}{\omega'_{P2}}\right)$$

as ω=GBW(taken this as a frequency range)

$$< A_0(S) = -tan^{-1}\left(\frac{\text{GBW}}{\omega'_{Z1}}\right) - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{P1}}\right) - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{P2}}\right)$$

under condition $\omega'_{Z1} \geq 10GBW$

$$< A_0(S) = tan^{-1}\left(\frac{\text{GBW}}{\omega'_{Z1}}\right) - tan^{-1}(A_{dc}) - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{P2}}\right)$$

as $A_{dc}$ is very higher value so $tan^{-1}(A_{dc})$=$90^0$

$$< -180^0 - PM = tan^{-1}\left(\frac{1}{10}\right) - 90^0 - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{P2}}\right)$$

PM=$90^0$-$tan^{-1}\left(\frac{\text{GBW}}{\omega'_{P2}}\right) - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{Z1}}\right)$

For phase margin of $60^0$and $\omega'_{Z1} = 10GBW$

$$\omega'_{P2} = 2.2\ GBW \qquad \omega'_{P2} = 2.2\ GBW$$

$$C_C = .22C_L \text{ and } g_{m2} = 10g_{m1}$$

As seen that with higher value $g_{m2}$ the value of $C_C$ we will get become smaller but it leads to large current flow in output stage and hence more static power loss occurs in amplifier as with large value of $C_C$ it accurse large area on chip, if we chose load resistance and capacitance too large than open loop zero come in picture and then,

PM=$90^0 - tan^{-1}\left(\frac{\text{GBW}}{\omega'_{Z1}}\right)$ then $\frac{g_{m2}}{g_{m1}} = \frac{1}{\tan(90^0 - PM)}$

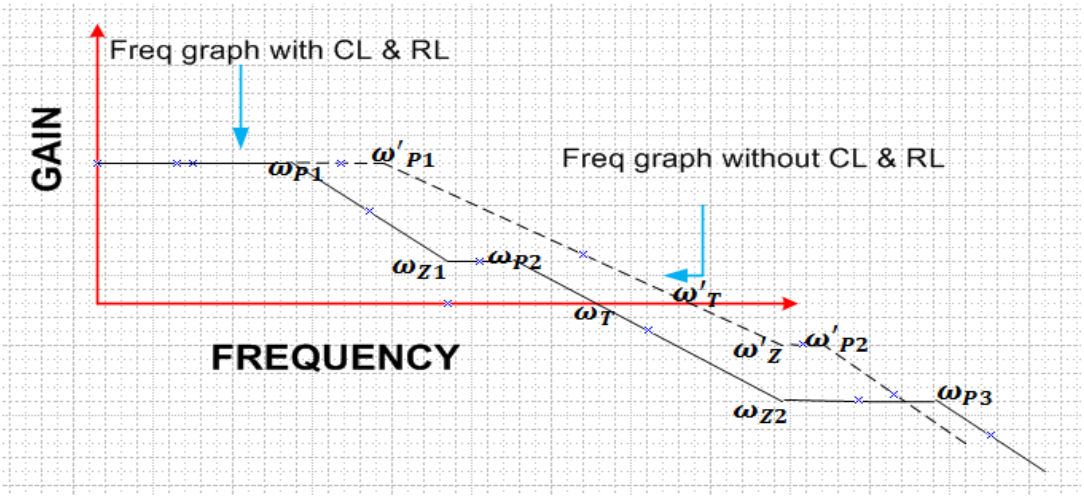


Fig 6. Open loop frequency response of two-stage opam with & without load capacitance and resistance

## 3. PROPOSED BUFFER AMPLIFIER WITH DYNAMIC FLOATING

To reduce the static power loss we combined N- type and P-type differential pair with dynamic floating concept to reduce the current flowing at the output stage, two floating bias current ln1 and ln2 are used to charge and discharge the output node in combination with lb1 and lb2, during transition phase from low to high Mp-bias will provide extra current to charge the capacitive load and during high to low Mn-bias will sink the extra current to discharge the capacitive load quickly this is the methodology for which we quickly charge and discharge the output load without increasing the static current that flows through the complementary common source

amplifier M01 and M02. The two output are isolated by the combination of 6 transistors as shown in the figure.7 Mn-bias, Mn-bias,MDN1, MDN2, MDP1 and MDP2 for same rising and falling time ln1=ln2,lb1=lb2

$$lb1 = lb2 = ln1\left[\, 1 + \frac{(W/L)_{MDN2}}{(W/L)_{MDN1}} + \frac{(W/L)_{MDP2}}{(W/L)_{MDP1}} \,\right]$$

The schematic of the proposed buffer is shown in the figure. 8,M1-M5 shows NMOS differential pair,M6-M10 shows PMOS differential pair,C1-C4 shows miller capacitance, the biasing current of NMOS and PMOS pair is Ib as M01 and M02 are mirrored from M5 and M10 which is Ib/2 current that will flow, as seen the output stage biased by dynamic floating and 2 single-stage differential pair, the circuit will suffer from output DC offset voltage which is removed by proper sizing as

$$\frac{(W/L)_{M01}}{(W/L)_4} = \frac{(W/L)_{M02}}{(W/L)_9} = ln1\left[1 + \frac{(W/L)_{MDN2}}{(W/L)_{MDN1}} + \frac{(W/L)_{MDP2}}{(W/L)_{MDP1}}\right]$$

To design operational amplifier for LCD the following requirement should meet according to number of bits or resolution of DAC used in LCD panel[23],The open loop gain will be estimated as

$$A_{OLDC} \geq 2^{N+1}$$

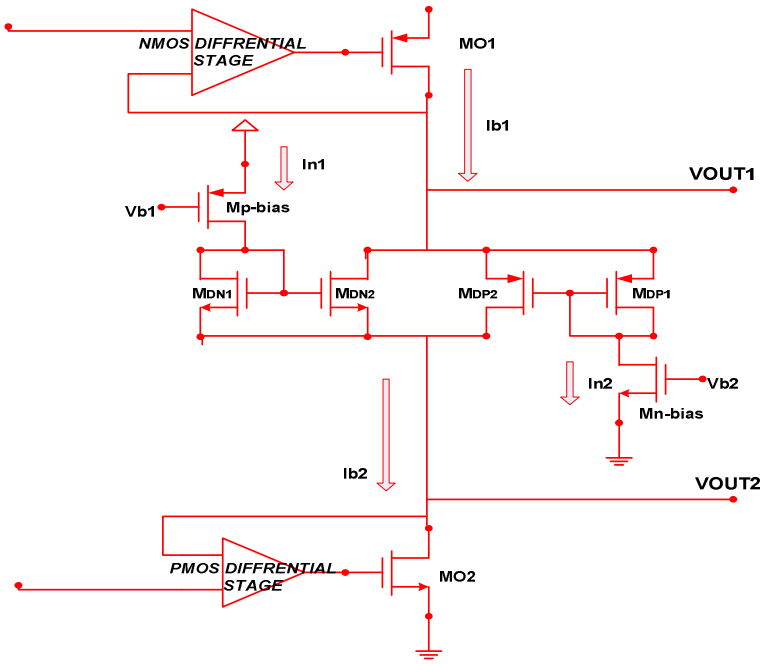


Fig 7. Architecture of proposed dynamic floating buffer amplifier

Let open loop gain will be 1000 then gain error will be

$$\text{gain error} = \frac{1}{.5\times 1000} = .0002 \leq \frac{V_{ref}}{2^{N+1}}$$

so min value of VDD=512× .002 = 1.02 $volt$ and with specific settling time which should be less than scanning time let it will be 1µs,the gain bandwidth

$$GBW \geq \frac{ln2^{N+1}}{2\pi t_s}$$

for 8 bit the frequency does not exceed 1Mhz. So the design specification for buffer amplifier is DC gain ≥ 1000=60db, VDD=3.3 volt , GBW=1Mhz PM=60$^o$ ,CMOS technology 180nm, load capacitance= 30pf and load resistance of 30kΩ.

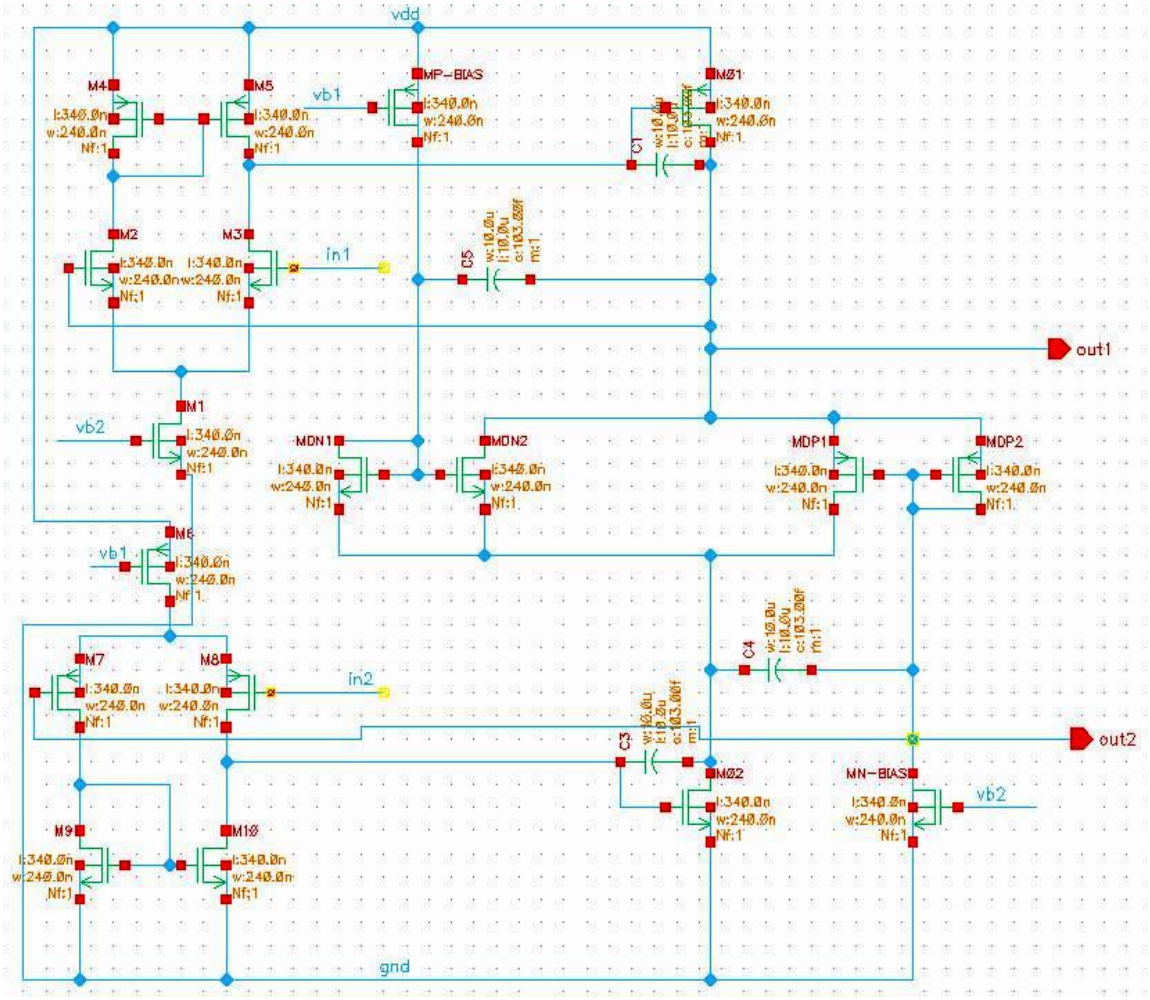


Fig 8. Schematic of proposed dynamic floating buffer amplifier

| | | | | | |
|---|---|---|---|---|---|
| M1 | $^{1.5}/_{1}$ | M9 | $^{5}/_{1}$ | M01 | $^{28}/_{1}$ |
| M2 | $^{1.9}/_{1}$ | M10 | $^{5}/_{1}$ | M02 | $^{28}/_{1}$ |
| M3 | $^{1.9}/_{1}$ | MPBIAS | $^{4.5}/_{1}$ | C1 | 1p |
| M4 | $^{5}/_{1}$ | MNBIAS | $^{4}/_{1}$ | C2 | 6p |
| M5 | $^{5}/_{1}$ | MDN1 | $^{4.5}/_{1}$ | C3 | 1p |
| M6 | $^{2}/_{1}$ | MDN2 | $^{9}/_{1}$ | C4 | 6p |
| M7 | $^{25}/_{1}$ | MDP1 | $^{8}/_{1}$ | CL | 30P |
| M8 | $^{25}/_{1}$ | MDP2 | $^{4}/_{1}$ | RL | 30Ω |

## 4. EXPERIMENTAL RESULT

The proposed buffer amplifier is fabricated using a 180nm CMOS technology. The chip area occupied by the buffer is 30×72 $\mu m^2$, fig 9 shows the output with 50kz input square wave with load capacitance of 30pF and 30kΩ resistance, fig 10 shows triangular response of proposed buffer, the slew rate obtained is 4.8v/μs with setting time of 4.5 μs and 4.2 μs for up and down stream of square wave, the biasing current per channel is 5μA. And power consumed by buffer is 72 μw. The simulation results using transient and AC analysis is shown in figure from 9 to15 using cadence spectre simulation tool.

## 5. CONCLUSION

This paper represents a low power buffer amplifier, with low quiescent current with the dynamic floating output node we adjust the output bias current without changing the input differential pair biasing current configuration, according to load capacitance the output current will be varied with the help of floating bias current network. The use-fullness of such type of buffer is, it work as positive and negative type buffer without any switched capacitor network which is used to toggle the differential amplifier in between positive and negative buffer.

COMPARISON TABLE

| | **This work** | **[1]** | **[2]** | **[3]** | **[4]** |
|---|---|---|---|---|---|
| **Process** | 180nm CMOS | .35μmCMOS | .35μmCMOS | .35μm CMOS | .35μm CMOS |
| **VDD** | 3.3 | 5 | 3.3 | 5 | |
| **Bias current** | 5μA/per channel | 2μA | 7.4μA | NA | 5μA |
| **loads** | 30KΩ, 30pF | 10KΩ, 24pF | 600pF | 400pF | 10pF |
| **o/p swing** | 96% | NA | NA | NA | NA |
| **Settling time** | 4.5μs | 2μs | 8μs | 1μs | .5μs |
| **Slew rate** | 5v/ μs | NA | NA | NA | 2v/ μs |
| **Area** | 30×72 $\mu m^2$ | 22×190$\mu m^2$ | 100×45$\mu m^2$ | 86×74 $\mu m^2$ | .04 $mm^2$ |

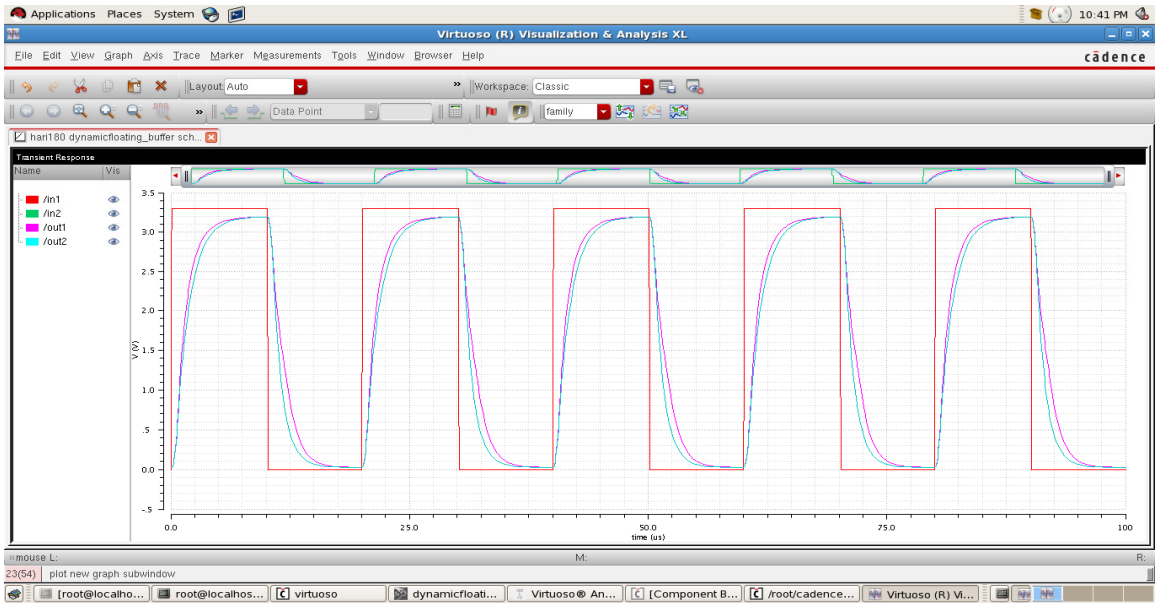


Fig 9. Simulation result with rectangular wave of frequency 50khz with load

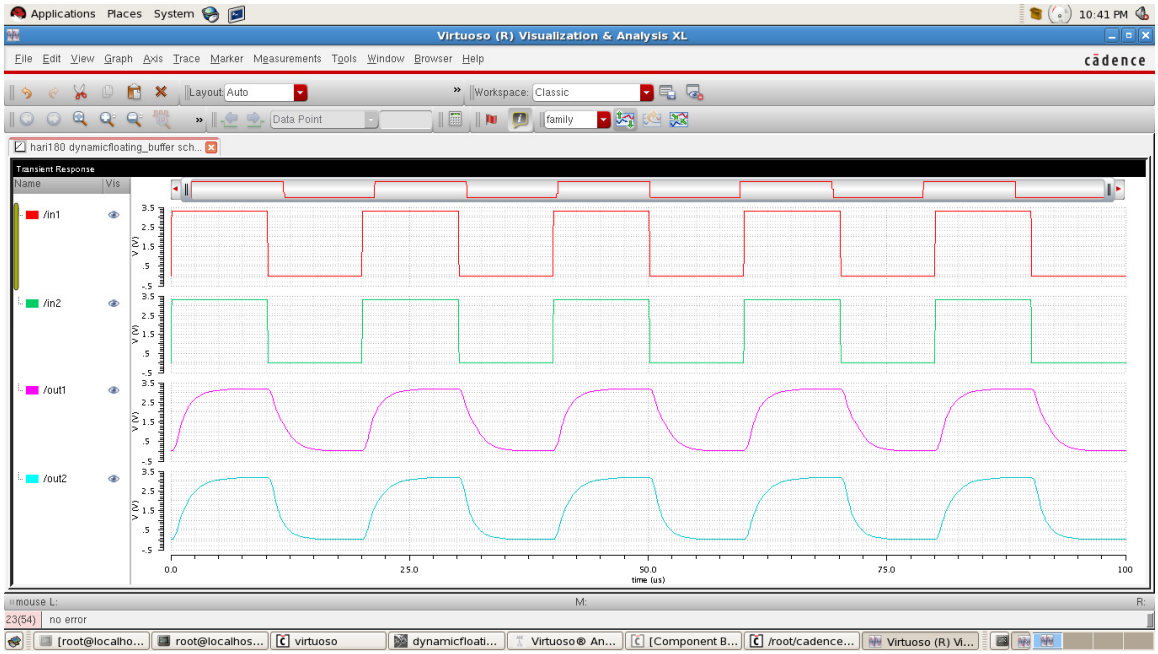


Fig 10. Simulation result with rectangular wave of frequency 50khz with two input output

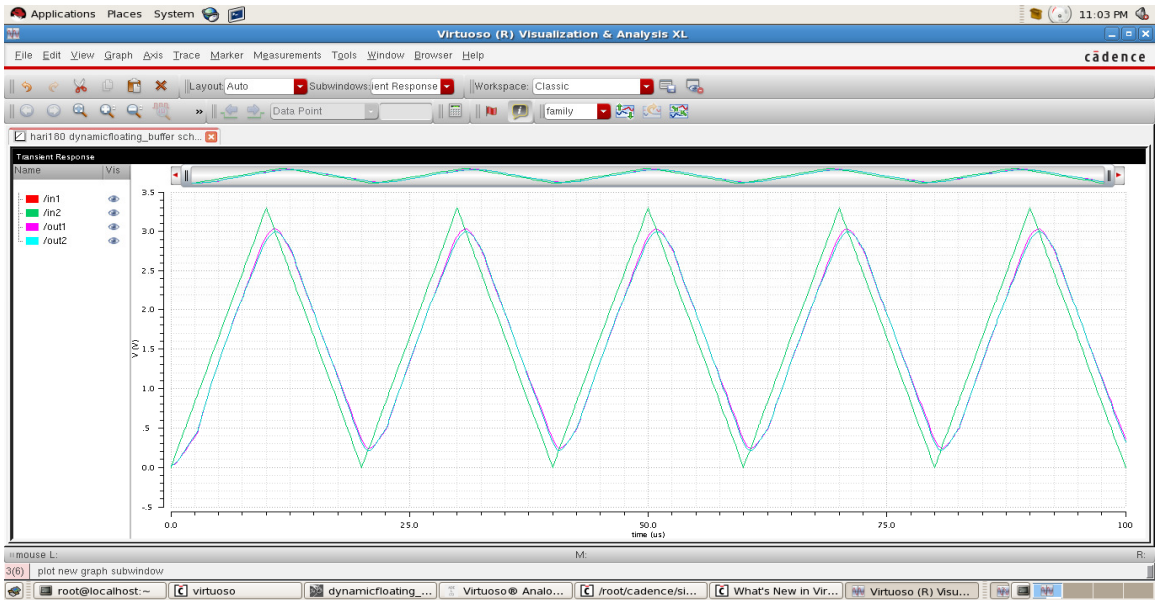


Fig 11. Simulation result with triangular wave of frequency 50khz with load

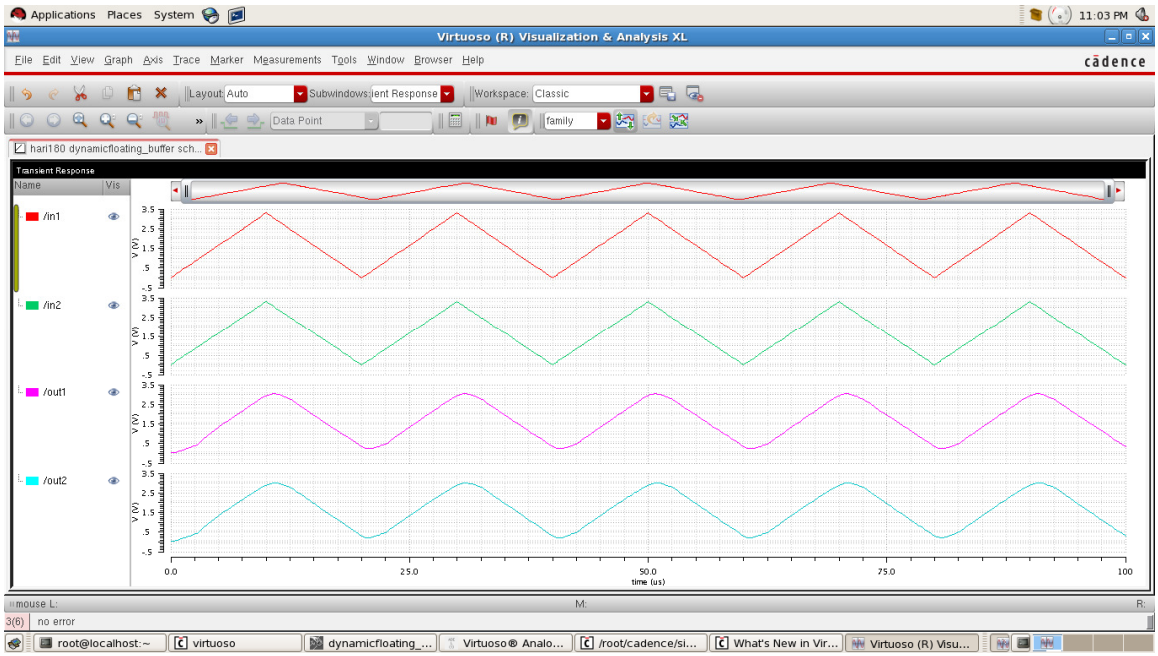


Fig 12. Simulation result with triangular wave of frequency 50khz with two input output

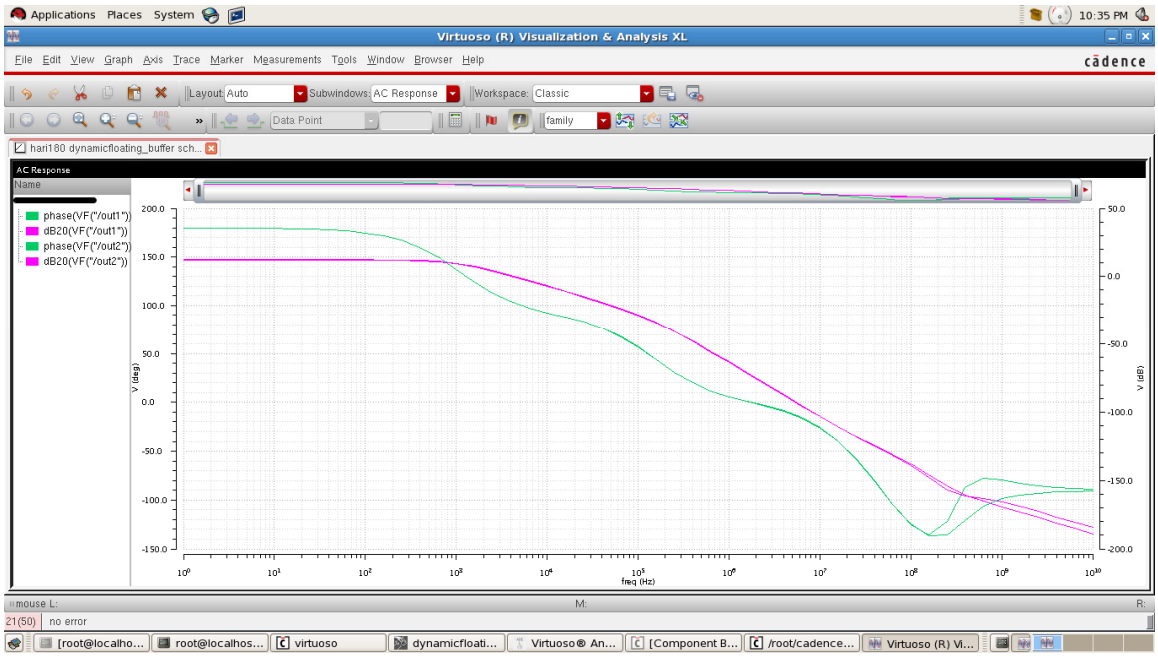


Fig 13. AC response of the proposed floating load output stage

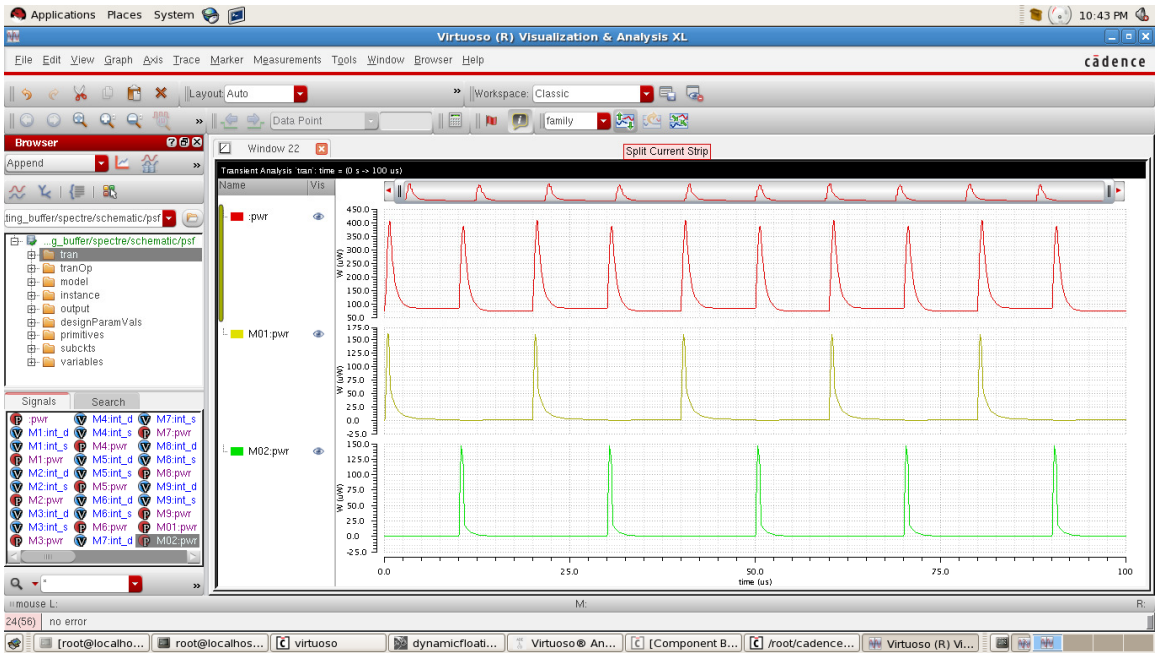


Fig 14. Power diagram with rectangular wave of frequency 50khz with load

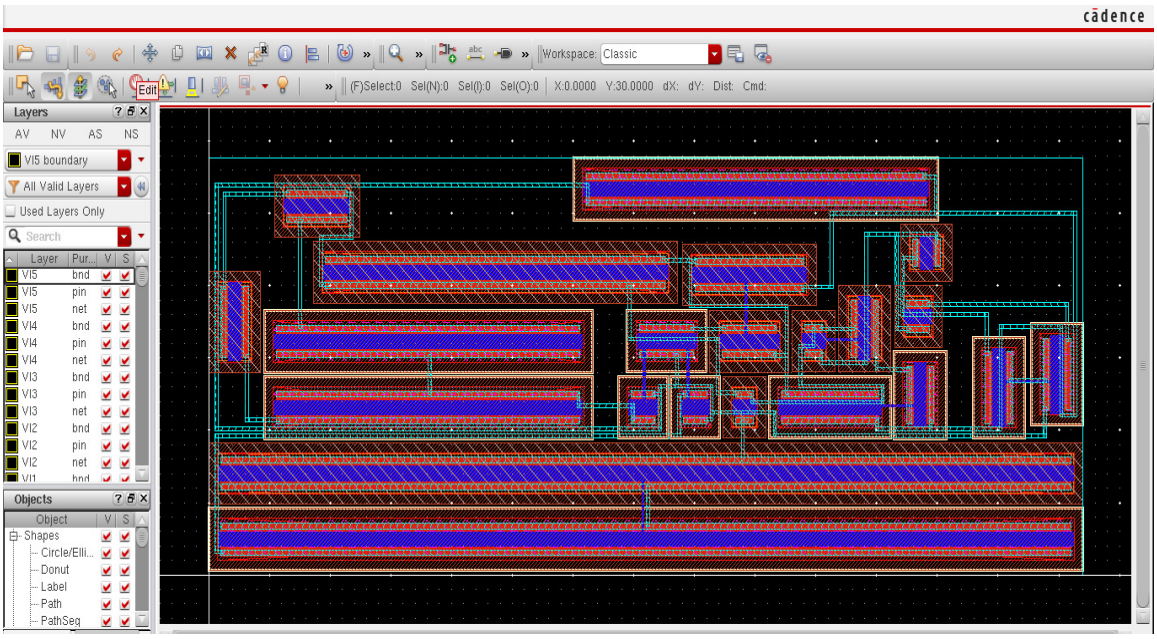


Fig 15. Layout diagram of proposed floating output node of buffer amplifier

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