EVALUATION OF ATM FUNCTIONING USING VHDL AND FPGA

Manali Dhar[1], Debolina Roy[2] and Tamosha Saha[3]

[1]Assistant Professor, Department of Electronics & Communication Engineering, DSCSDEC, Kolkata, India
[2,3]UG Student, Department of Electronics & Communication Engineering, DSCSDEC, Kolkata, India

ABSTRACT

It has been almost four decades that banks and other financial organizations have been gradually computerised, in order to improve service and efficiency and to reduce cost. The birth of Electronic Fund Transfer and Automated Teller Machines has given rise to 24-hour banking and a greater variety of services for the customer. This method uses a computer to transfer debits and credits, with the help of electronic pulses, which are carried through wires either to a magnetic disk or tape. ATM (Automated Teller Machine) has become an important part in our daily lives. People use ATM for various purposes such as money withdrawal, checking balance, changing password etc. Since it mainly deals with people's money, it has to be a secure system on which we can rely. We have taken a step towards increasing this security and integrity by trying to implement the functioning of an ATM using VLSI-based programming, HDL(Hardware Description Language).The conventional coding languages such as C,C++ are replaced by VHDL(Very High Speed Integrated Circuit Hardware Description Language) so that the code cannot be easily hacked or changed. This article consists of an insight into the various functions that can be performed using an ATM, a brief description of the Coding and the obtained simulation results. It also consists of the implementation of the code using FPGA Kit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM (Automated Teller Machine), Security, HDL (Hardware Description Language), FPGA (Field Programmable Gate Array).

1. INTRODUCTION

An Automated Teller Machine (ATM) is a safety as well as complex and real-time system that are highly complicated in design and implementation. ATM transaction is a process that involves any request of money withdrawal or balance check from the user, its approval by the system and completion successfully. The main steps that make up an ATM transaction are-1) Card Insertion, 2) Card Authentication, 3) Password Verification and 4) Transaction Approval. In Card Authentication, the card is inserted by the user in the card slot of the ATM.

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In Card Authentication, the originality and validity of the card entered is checked by the system. In the Password Verification step, the user is asked to enter the preset password to access his/her bank account. This is a vital step which maintains the security of the system. If the password entered is wrong, the user is denied access to the account, otherwise access is granted. In the final step, Transaction Approval, the user is asked to enter the amount of money he/she wishes to withdraw. This amount is then checked against the balance left in the user's account. If balance is sufficient, withdrawal is approved and the transaction procedure ends. These will be discussed in further detail later in this document.

2. SOLVING CONVENTIONAL CODE IMPLEMENTATION USING VHDL

The entire transaction process implying the various ATM functions are implemented using VHDL, as it is a more secure programming language and allows for a better design management. Also, VHDL is technology independent. The ultimate result of the coding is observed by integrating it on the Spartan FPGA Kit.

VHDL is an acronym for VHSIC Hardware Description Language (VHSIC is an acronym for Very High Speed Integrated Circuits). It is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. The digital system can also be described hierarchically. Timing can also be explicitly modelled in the same description. VHDL is a powerful language with numerous languages constructs that re capable of describing very complex behaviour.

Firstly, it allows description of the structure of a design that is how it is decomposed into sub-designs, and how those sub-designs are interconnected. Secondly, it allows the specification of the function of designs using familiar programming language forms. Thirdly, as a result, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping automated teller machines (ATMs) are embedded systems for financial-related services. In the development of Very Large Scale Integration technology, the Field-Programmable Gate Array (FPGA) has been widely used to implement digital systems because of its simplicity, programmability, short design cycle, fast time-to-market, low power consumption, and high density. An FPGA provides a compromise between an application-specific integrated circuit (ASIC) and a general purpose processor. Systematically design efficient, portable, and scalable register transfer level (RTL) digital circuits using the VHDL hardware description language and synthesis software. An RTL design can accommodate future simulation, verification, and testing needs, and can be easily incorporated into a larger system or reused.

2.1. VHDL CODE IMPLEMENTATION

VHDL is a language for describing digital electronic systems. VHDL is designed to fill a number of needs in the design process. Here, we have sketched the flowchart according to which we have developed our program using VHDL programming language which is more advantageous than other existing languages.

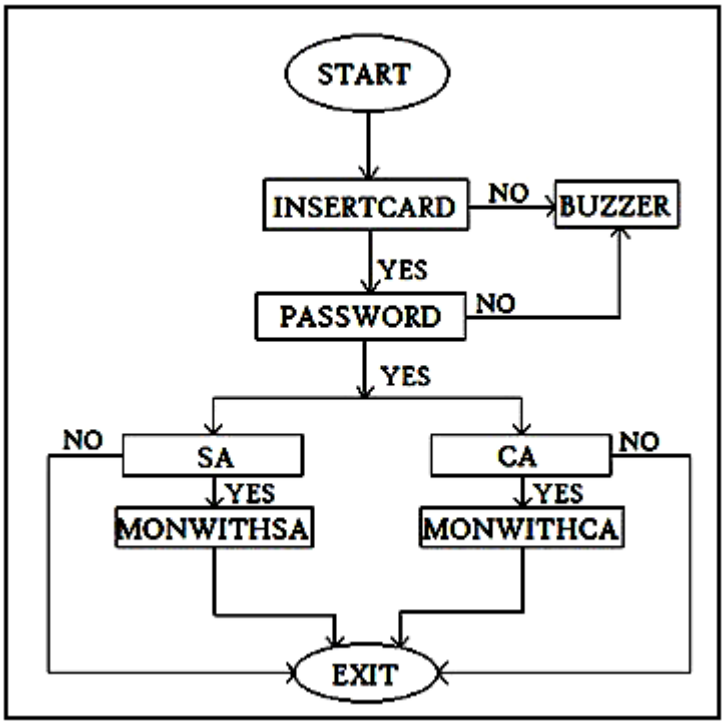

Fig.1 Flowchart of VHDL code of specified ATM functioning

In automated teller machines (ATMs) the method of electronic funds transfer is incorporated which uses a computer to transfer debits and credits with the help of electronic pulses, which are carried through wire either to a magnetic disk or tape. Using an ATM card a customer can access nearly all the facilities available from a counter service. The basic operation according to the given flowchart (Figure 1) can be explained according to the following stages. The whole process can be described as following- STAGE 1: In the first stage, the customer/card holder inserts the card at the slot provided for card insertion in the ATM machine for card authentication. If the card seems to be invalid/not inserted in a proper manner, it is indicated through the buzzer. While, if the card is valid, it automatically proceeds to the next stage. In this stage, it is verified whether the inserted card is valid or not. If it seems to be invalid, then it is indicated though the buzzer. If it is the valid one, then it further proceeds. As the next step it asks for a valid password to be inserted by the card holder. Again, if the entered password is wrong, a next chance is provided to the user to re-insert the correct password. In case of the entered password is correct at the first attempt, the system allows to proceed further. STAGE 2: In this stage, the system asks the card holder to enter a valid password. If the entered password is a wrong one, it is indicated by the buzzer. In case of a correct password, the system proceeds further.

STAGE 3: In the third stage, we have considered two options: a) Savings Account, b) Current Account.

In order to proceed further, the customer have to select any one option from this list :- i) If the Savings Account option is selected, the money withdrawal is done on the Savings Account, ii) If the Current Account is selected, then the money is withdrawn from the Current Account.

2.2. SIMULATION TOOLS

Xilinx ISE 9.2i:

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx company for synthesis the proposed design and analysis of Hardware Description Language(HDL) designs, enabling the developer to compile the designs, examine RTL(Register Transfer Level) diagrams, perform timing analysis(Test Bench Waveform),simulate a design's reaction and configure the target device with the programmer.

ALS-SDA-CPLD/FPGA VHDL Trainer Kit (DAUGHTER BOARD-FPGA – XILINX-XC3S50):

The ALS CPLD/FPGA TRAINER is a powerful tool that allows the user to understand the capabilities of FPGA and CPLD. Configuration is the process by which the bit streams of a design, as generated by the development software are loaded into the internal configuration memory of the FPGA or CPLD. The Spartan-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, Cost-sensitive consumer electronic applications. Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications; including broadband access, home & broad range networking, display/projection and digital television equipment.

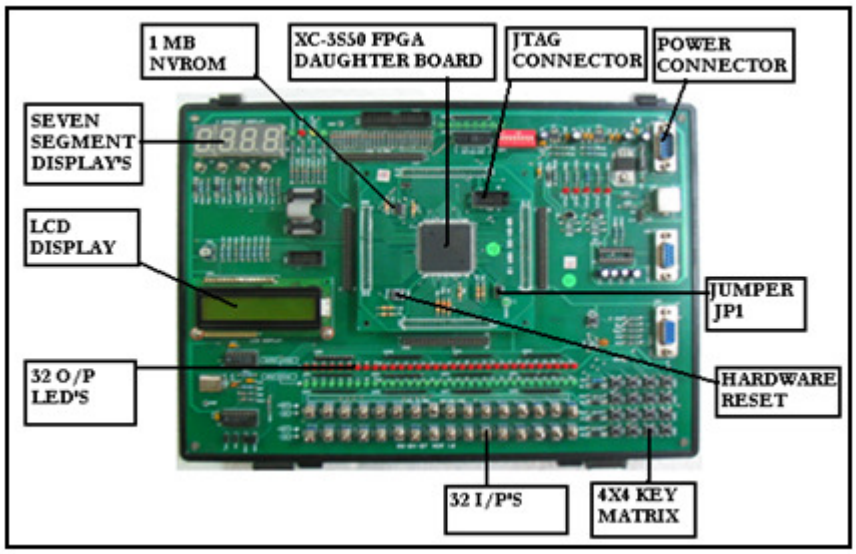

Fig.2 XC-3S50 FPGA VHDL TRAINER KIT

This kit provides some features: Spartan -3 FPGA devices XC3S50-PQ208 of Xilinx, It has 50k System gates, consists of 1,728 logic cells, and it employs 12k Distributed RAM. It also has 72k Block RAM; it is an FPGA IC in a PQFP208 pin package with 124 I/O lines. And the specified Daughter Board has some features: Push button switches PROG to initiate FPGA during master serial mode, Optional PROM, Four sets of 20x2 berg connector for plugging on to the baseboard , Mode selection jumpers (JP1) Power supply +3.3V, 2.5V and 1.2V are provided from the baseboard.

The SPARTAN-3 FPGA of XILINX uses SRAM technology. SPARTAN-3 devices support serial configurations, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Spartan-3 devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode ARTAN
- Boundary-scan mode

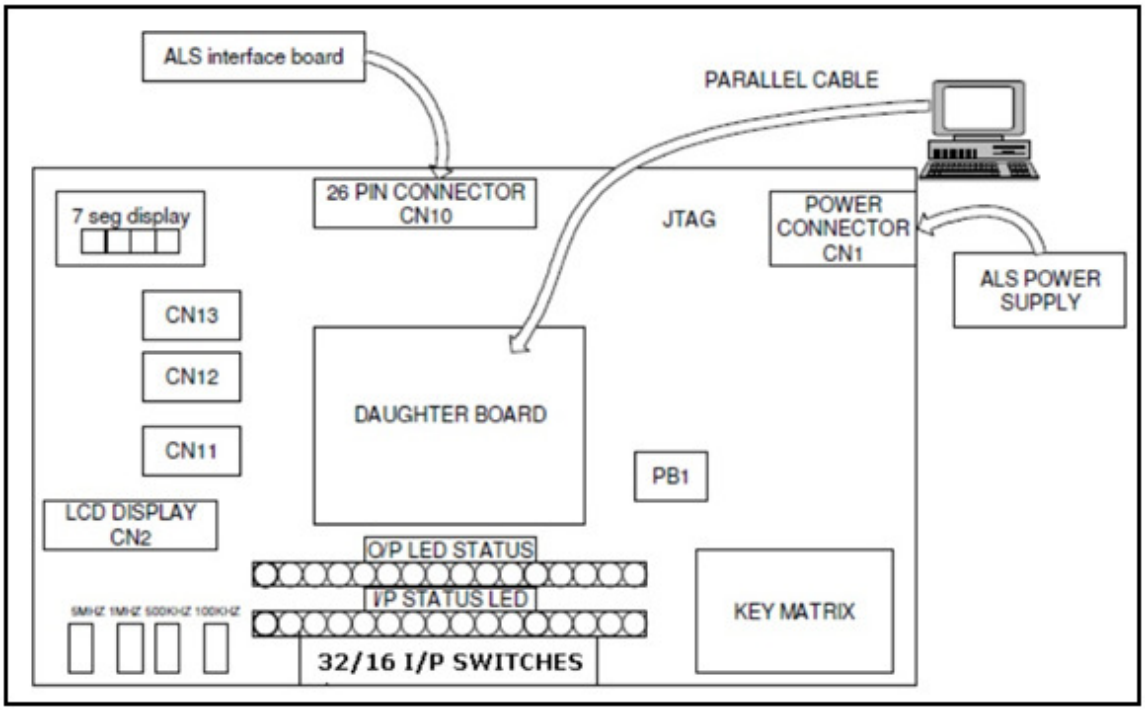

Fig.3 Connection diagram of Base-Board

2.3. SIMULATION PROCEDURE

First the VHDL code is implemented and executed using Xilinx ISE 9.2i and the results are gathered. The corresponding output from Xilinx are synthesize report, RTL schematic, Test Bench Waveform (user-friendly) and Output waveform according to algorithm; after the final execution of coding VHDL code will have to loaded to XC-3S50 FPGA VHDL TRAINER KIT and the corresponding input and output will be shown with the help of O/P & I/P LED Status (mentioned in Fig.3).The corresponding Simulation results are mentioned in the next sections. Here, below table indicates the different port names which allocate the performance of input. Then port type is the performance of input and performance in the given algorithm.

Table1. PORT Depiction

PORT NAME	PORT Significance
INSCRD (*Insert Card*)	ATM Card is properly inserted or not *(I/P PORT)*
PASSWRD (*Password*)	If Card is properly inserted, asks for proper Password insertion *(I/P PORT)*
BUZZER	Indicates the result of Validity Check *(O/P PORT)*
SAVACCT (*Savings Account*)	Asks user for choosing of account type Savings Account *(I/P PORT)*
CURRACT (*Current Account*)	Asks user for choosing of account type Current Account *(I/P PORT)*
MONWITHSA (*Money Withdrawal from Savings Account*)	Depends on account selection, user ready to withdrawal money from concerned account *(O/P PORT)*
MONWITHCA (*Money Withdrawal from Current Account*)	Depends on account selection, user ready to withdrawal money from concerned account *(O/P PORT)*

Using the software, Xilinx 9.2i ISE the implementation of the ATM code is performed practically. The FPGA hardware used is Spartan 3 series on which we have implemented and practically performance of the ATM code is carried out successfully. The simulation results are presented in the next section with the snapshots of the hardware implementation we have carried out.

2.4. SIMULATION RESULTS

RTL Schematic Diagrams are given in Fig.4. & Fig.5, which we have obtained by simulating the VHDL code using Xilinx 9.2i software, is implemented in the software and the corresponding RTL views are obtained.

The RTL schematics are followed by the Test Bench waveform (user friendly input) in Fig.6 and its respective simulation output in Fig.7 which has been obtained by giving certain conditions to the Test Bench waveform as inputs.

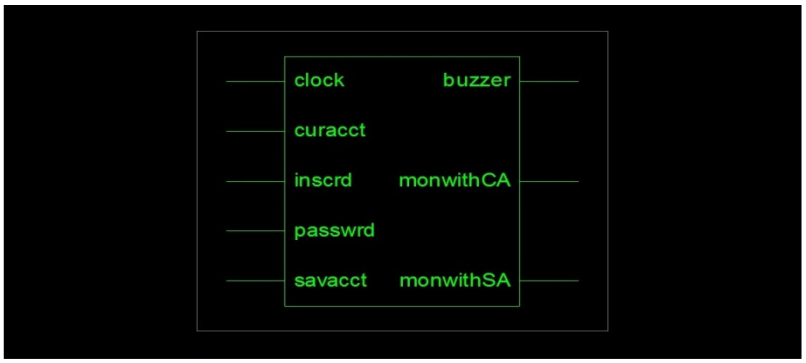

Fig 4.RTL Schematic Diagram of Xilinx 9.2i ISE

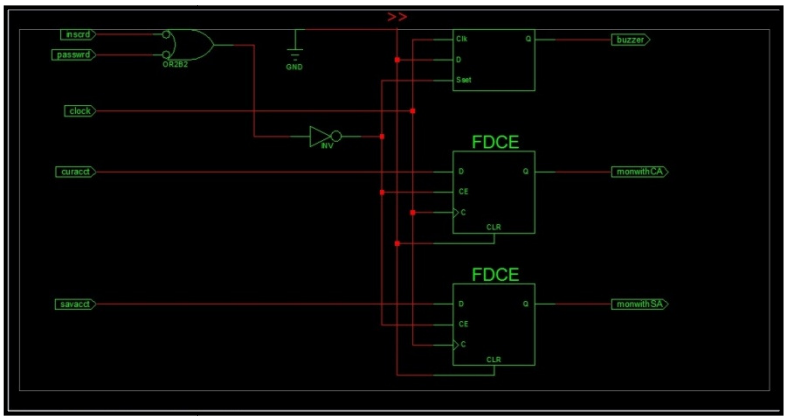

Fig 5.RTL Schematic Diagram-2 of Xilinx 9.2i ISE

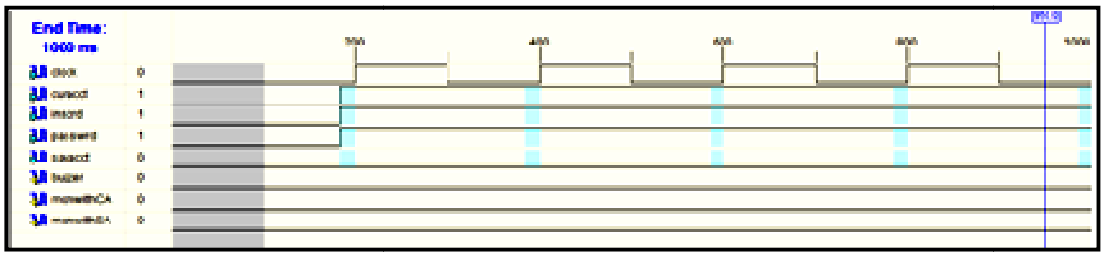

Fig 6.Testbench Waveform generated by Xilinx 9.2i ISE

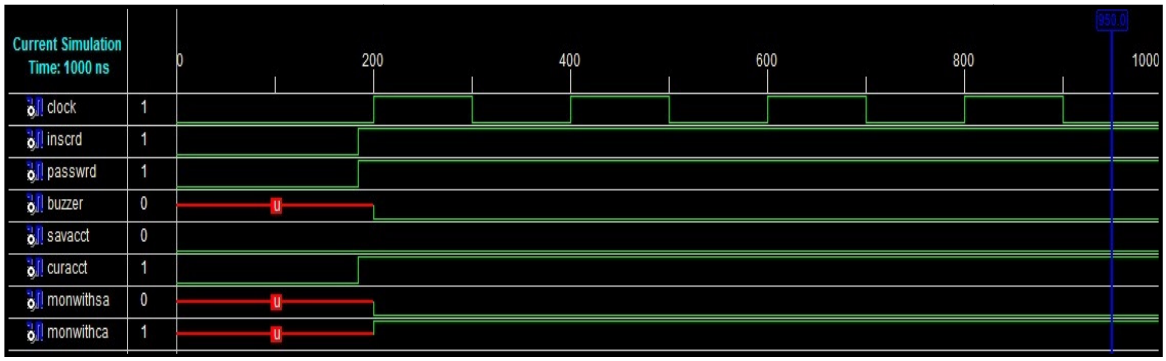

Fig 7. Simulation Output of Xilinx ISE 9.2i

In the test bench waveform, as it is visible from the figure, certain conditions are given as inputs. The CURRACCT, INSCRD, PASSWRD options are entered as 1 which means these options are made true. The simulation output according to the given inputs may be explained according to the following simulation description table.

Table 2. SIMULATION PORT Depiction

SL. NO.	NAME OF PORT	STATUS	TASK DESCRIPTION
1	INSCRD	1	When ATM card is inserted properly consequently this port is high.
2	PASSWRD	1	The correct password has been entered. At the same time as a result this port is also high.
3	BUZZER	0	Since there has been no problem with the card insertion and password authentication, the buzzer remains disabled.
4	SAVACCT	0	As no value is given in the input for this port so the output remains low.
5	CURRACT	1	This port is has been selected so it remains high.
6	MONWITHSA	0	As no value was entered for the savings account, so this port remains low.
7	MONWITHCA	1	As the current account was selected, so the money is withdrawn from the current account and thus it remains high.

Condition 1:- We have considered another condition where the SAVACCT, INSCRD, PASSWRD are selected and the test bench waveforms and simulation outputs are obtained as follows-

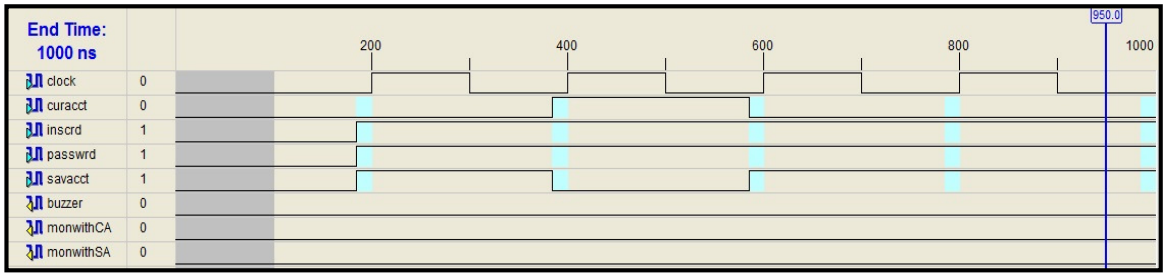

Fig 8. Test bench Waveform generated by Xilinx 9.2i ISE

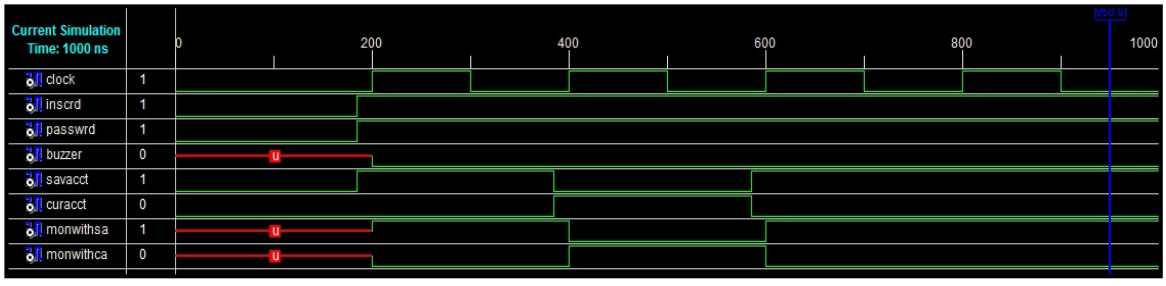

Fig 9. Simulation Output of Xilinx ISE 9.2i

This simulation output may be explained in a similar manner following the previous description table-

Table 3. SIMULATION PORT Depiction (Condition 1)

SL. NO.	NAME OF PORT	STATUS	TASK DESCRIPTION
1	INSCRD	1	As the ATM card is inserted properly so this port is high.
2	PASSWRD	1	The correct password has been entered. As a result this port is also high.
3	BUZZER	0	Since there has been no problem with the card insertion and password verification, the buzzer remains disabled.
4	SAVACCT	1	This port is has been selected so it remains high.
5	CURRACT	0	As no value is given in the input for this port so the output remains low.
6	MONWITHSA	1	As the savings account was selected this time, so the money is withdrawn from the savings account and thus it remains high.
7	MONWITHCA	0	As no value was entered for the current account, so this port remains low.

In the simulation outputs (Fig 7 & Fig 9), for both the cases certain ports are obtained as undefined (U) for a certain clock pulse. This indicates that for that particular clock pulse, the state of the ports could not be determined and hence they remain undefined.

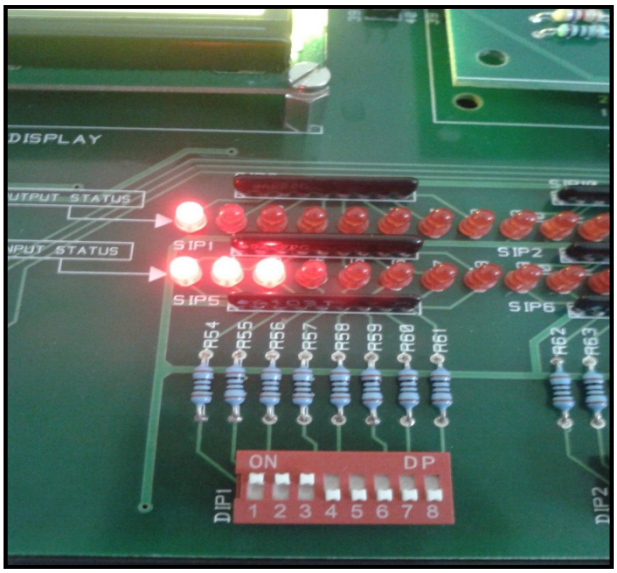

Fig 10. Simulation Output of FPGA VHDL Trainer Kit

In the above figure, the output of the first condition is shown. Here the INSCRD, PASSWRD, SAVACCT options as entered as 1 through the switches DIP1-1, 2 and 3 respectively. Hence the three corresponding LEDs of the SIP5 (INPUT LED) series are turned on showing the inputs. While, the first LED of the SIP1 (OUTPUT LED) series shows that the output port or MONWITHSA port is ON as well as working according to programme.

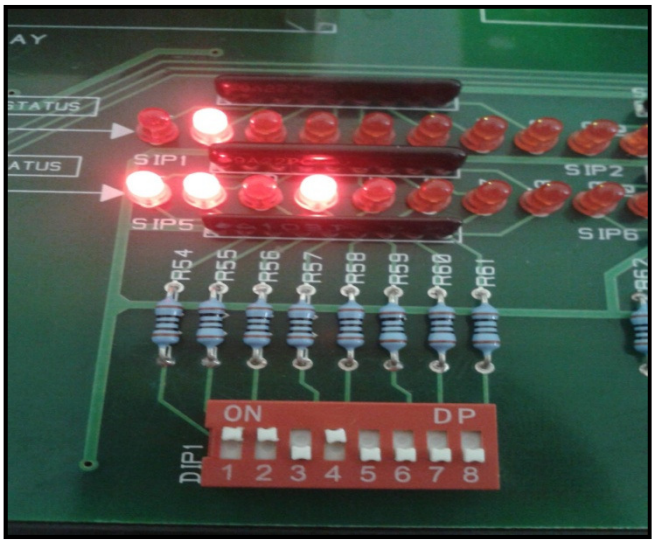

Fig 11. Simulation Output of FPGA VHDL Trainer Kit

In this figure, the INSCRD, PASSWRD AND CURRACCT options are selected through the switches 1,2 and 4 respectively which are shown through the first, second and fourth LEDs of the SIP5 series. The respective output port i.e. the MONWITHCA port is turned high and is thus shown by the second LED of the SIP1 series. Thus the FPGA implementation is accomplished successfully.

3. CONCLUSION

We have taken a step towards improving the security and integrity of an ATM using VHDL, keeping its original functioning intact. This is a new technology which may prove to be highly useful. This idea can gradually grow alongside the existing technologies to provide mankind with a more efficient and secure banking service. Using VHDL can reduce the menace posed by hackers, and many other such illegal activities which is a worldwide problem these days. Further, FPGA is a new and user-friendly technology which has found an important place in modern day research and development. This is flexible and can be combined with various software to yield in-vitro results. Thus, we sincerely hope that in the near future, this implementation will gain popularity and will be a significant contribution to the vast field of electronics technology.

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AUTHORS

[1] First Author – Manali Dhar, M.Tech (Microelectronics & VLSI Design), Dr. Sudhir Chandra Sur Degree Engineering College, Assistant Professor, Dept. of ECE, JIS Group and madhuja4u@gmail.com

[2] Second Author – Debolina Roy, Final Year B.Tech Student (Electronics & Communication Engineering), Dr. Sudhir Chandra Sur Degree Engineering College, JIS Group

[3] Third Author – Tamosha Saha, Final Year B.Tech Student (Electronics & Communication Engineering), Dr. Sudhir Chandra Sur Degree Engineering College, JIS Group