SCHOTTKY TUNNELING SOURCE IMPACT IONIZATION MOSFET (STS-IMOS) WITH ENHANCED DEVICE PERFORMANCE

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ABSTRACT

In this paper, we propose and investigate a schottky tunneling source impact ionization MOSFET (STS-IMOS) with enhanced device performance. STS-IMOS has silicide (NiSi) source to lower the breakdown voltage of conventional impact ionization MOS (IMOS). There is cumulative effect of both impact ionization and source induced tunneling for the current gating mechanism of the device. The silicide source offers immensely low parasitic resistance subsequently there is an increment in voltage drop across intrinsic region. This leads to appreciable lowering of breakdown and threshold voltage for STS-IMOS. Hence, it demonstrates enhanced device performance over conventional IMOS. Besides this for STS-IMOS the location of maximum electric field has shifted towards the source and now it is quite away from gate oxide. Hence, it shows high immunity against Vth fluctuations due to hot electron damage. Consequently, it is found that device reliability is also improved significantly.

KEYWORDS

Impact Ionization, Barrier Tunneling, Subthreshold Slope (SS), Schottky-Contacts

1. INTRODUCTION

In recent research, to overcome the “Boltzmann tyranny” and to realize “green transistors” with super steep subthreshold swing (SS) various charge based beyond CMOS non-conventional MOS devices have been proposed based on alternative charge injection mechanism. Among them IMOS [1]-[3] has evolved as a potential candidate having subthreshold slope (SS) as low as 5mV/dec significantly high I_{ON}/I_{OFF} ratio (approximately 10^7 - 10^8). IMOS has no channel potential barrier, it uses the potential difference between the source and the channel to determine whether breakdown occurs or not. As the carriers of I-MOS devices are injected by avalanche breakdown mechanism instead of thermal injection, the subthreshold swing can be reduced even below its theoretical limit (60 mV/dec) at room temperature. Structurally, IMOS [4], [5] is a gated p-i-n device with gate semi overlapped over the intrinsic region that operates in reverse-bias regime. The conduction mechanism of IMOS is entirely different from the thermally injected drift-diffusion mechanism based conventional MOS. The conduction mechanism in IMOS is governed by the avalanche impact ionization phenomenon [6], [7]. IMOS exhibits super steep

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sub-threshold behavior due to the inherent properties of impact ionization mechanism. As impact ionization has enormously high gain and carriers generated due to impact ionization can be easily removed due to drift in high electric field region. Hence, it can be concluded that IMOS uses the gate controlled modulation of the breakdown voltage to switch from ON state to OFF state and vice-versa. Further as impact ionization mechanism for charge injection in IMOS requires high electric field it results in high breakdown voltage (V_{Br}). It has high parasitic resistance of source region hence IMOS has high breakdown voltage and threshold voltage. To address this problem, a schottky tunneling source impact ionization MOSFET (STS-IMOS) with silicide source is proposed and investigated here. The fabrication process of STS-IMOS is compatible with the CMOS fabrication process flow. There is cumulative effect of impact ionization and source induced barrier tunneling. Simulation results demonstrate lower value of both threshold and breakdown voltages, enhanced I_{ON}/I_{OFF} ratio and steep subthreshold swing (SS) for STS-IMOS. This paper is organized as follows: Section II addresses, device structure and the simulation methodology for studying the device performance parameters. Section III shows the analytical framework for the proposed device followed by Section IV covers simulation results. Finally, Section V draws important conclusions from the simulation study carried out.

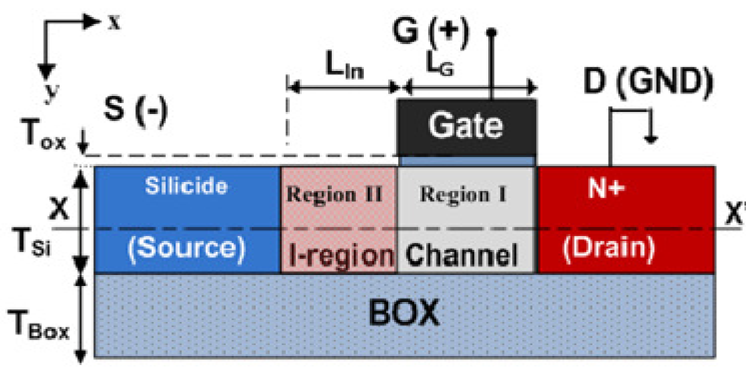

Figure 1. Schematic cross-sectional view of STS-IMOS.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Schematic cross-sectional view of STS-IMOS is shown in Fig. 1. Silicon film thickness (T_{Si}) is 15nm, thickness of gate oxide (T_{ox}) is 3 nm, total channel length (L_{ch}) is 200 nm, gate length (L_G) is 120 nm and intrinsic region length (L_{in}) is 80 nm. For IMOS source doping (N_A) and drain doping (N_D) for both transistors are taken to be 10^{19} cm^{-3}. STS-IMOS is having NiSi source as suggested in [8] - [9] with schottky barrier height φ_B as 0.6 eV. To model the source induced tunneling effect in STS-IMOS non-local tunneling model is incorporated with a non-local distance of 2 nm in Synopsys. STS-IMOS operating principle is based on the impact ionization and source induced tunneling as shown in Fig. 2. Under a high applied V_{SD} with low gate bias V_{GD} there is no inversion in the region under gate, hence the effective channel length is the length of the entire intrinsic region. With increment in V_{GD} there will be formation of inversion layer under the gate hence effective channel length is now reduced to i-region without the gate and electric field is intensified across this region, resulting in larger fraction of V_{SD} drop across it and this initiates avalanche multiplication. Now, in STS-IMOS large V_{GD} is applied modulates the effective φ_B and tunneling distance as well. Hence, there tunneling of electrons from source to drain, consequently there will current amplification. In order to optimize the device performance the parasitic resistances of source and the drain must be as small as possible and the effective voltage drop across the intrinsic channel region must be large to initiate the avalanche multiplication and tunneling simultaneously.

3. MODELING OF STS-IMOS

The net current through STS-IMOS has three components, impact ionization current (I_{ii}) due to high electric field, tunneling current (I_{Tun}) and thermionic current (I_{Therm}) due to silicide source. As impact ionization current and tunneling current will be major components, hence thermionic emission current is neglected.

$$I_{eff} = I_{ii} + I_{Tun} + I_{Therm} \approx I_{ii} + I_{Tun} \quad (1)$$

3.1. Source induced tunneling Current Component (I_{Tun})

To quantify the tunneling current $I_{T\,un}$ in STS-IMOS, the tunnel current barrier is characterized by the transmission function *T(E)* using (WKB) approximation as

$$T(E) = \exp\{-A(\phi_B - E)^{3/2}\} \quad (2)$$

Where, A denotes the Richardson constant given by

$$A = \frac{4\sqrt{2m^*}}{3q\text{h}E_{elect}}$$

Now, the tunneling current can be modeled by solving

$$I_{Tun} = \frac{4e}{h}\int_{\phi_B - qV_{GTun}}^{\phi_B} T(E).f_m.[1 - f_s(E)].dE$$
$$= \frac{4e}{h}\phi_m \int_{\phi_B - qV_{GTun}}^{\phi_B} \exp\{-A(\phi_B - E)^{3/2}\}. \quad (3)$$
$$[1 - \frac{1}{1+\exp\{E/k_B T\}}].dE$$

Using Boltzamann's approximations and expanding the terms by using Taylor series and considering only upto 2nd order terms we get,

$$I_{Tun} = \frac{4e}{h}\phi_m[\xi_1 V_{GTun} - \xi_2 V_{GTun}^2] \quad (4)$$

$$\xi_1 = 2q(\frac{1+\phi_B^{3/2} + A^2\phi_B^3}{k_B T}); \qquad \xi_2 = q^2(\frac{1+\phi_B^{3/2} + A^2\phi_B^3}{k_B T})$$

where, $V_{GT\,un}$ is the effective gate threshold bias appearing in the intrinsic region to initiate the tunneling mechanism and it is linearly dependent on the applied gate bias V_{GD}.

3.2. Impact Ionization Current (I_{ii})

The ionization current is the major current component because of high electric field in the intrinsic region of STS-IMOS. In order to quantify the current contribution due impact ionization process in STS-IMOS we have followed the compact modeling technique developed by Mayer

[10] for IMOS. I_{ii} in STS-IMOS can be modeled by using the initial the electric field in the structure, depending on the applied bias and the device geometry is calculated. This calculated electric field in the region of impact ionization is then incorporated in the ionization integral, M. The two dimensional Poisson's equation in area-I is

$$\frac{\partial^2 \psi_1(x,y)}{\partial x^2}+\frac{\partial^2 \psi_1(x,y)}{\partial y^2}=\frac{qN_i}{\varepsilon_{Si}};0\le x\le L_G;0\le y\le T_{Si} \tag{5}$$

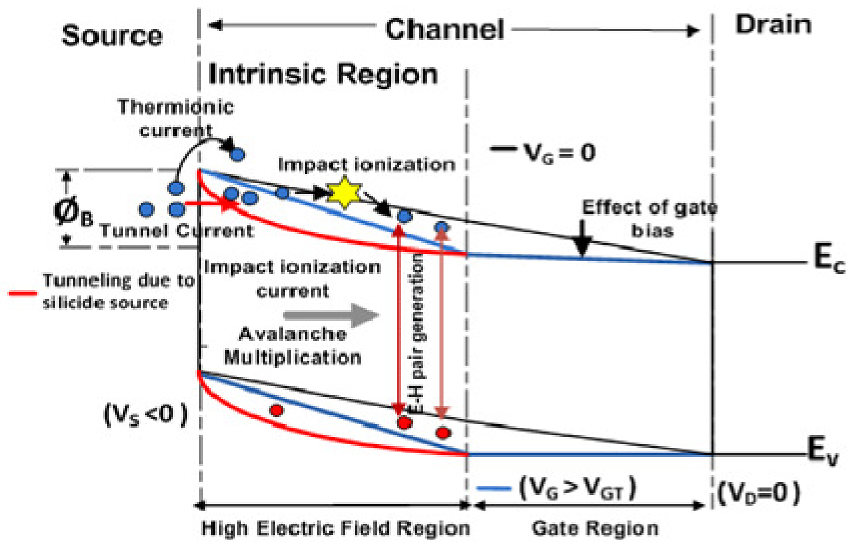

Figure 2. STS-IMOS conduction mechanism

Solution for $\psi_1(x)$ can be obtained by considering the parabolic potential function approximation and imposing following boundary conditions

$$\frac{\partial \psi_1(x,y)}{\partial x}\Big|_{y=0}=-[\frac{\varepsilon_{ox}}{\varepsilon_{Si}}][\frac{V_G-\psi_{0,1}(x)+\Delta\psi_{ms}}{T_{ox}}] \tag{6}$$

$$\frac{\partial \psi_1(x,y)}{\partial x}\Big|_{y=T_{Si}}=0 \tag{7}$$

General solution for the above differential equation will be of the form

$$\psi_1(x)=A^{'}\exp(\sqrt{\gamma}x)+A^{"}\exp(-\sqrt{\gamma}x)-\{\frac{\Im}{\gamma}\} \tag{8}$$

Where,

$$\gamma=[\frac{\varepsilon_{ox}}{\varepsilon_{Si}T_{ox}T_{Si}}];\Im=[\frac{qN_i}{\varepsilon_{Si}}-(\frac{\varepsilon_{ox}}{\varepsilon_{Si}})[\frac{V_G+\Delta\psi_{ms}}{T_{ox}T_{Si}}]] \tag{9}$$

Similarly potential function and electric field in region-II can be given by,

$$\psi_2(x)=[\frac{qN_i}{\varepsilon_{Si}}]x^2+\theta x+\phi;E_2(x)=-[\frac{qN_i}{\varepsilon_{Si}}]x-\theta \tag{10}$$

where, $A^{'}$, $A^{''}$, θ and ϕ are constants whose values can be obtained by imposing the following boundary conditions

$$\psi_1(0) = V_D; \psi_2(L_G + L_{in}) = V_S + V_{bi}; \psi_1(L_G) = \psi_2(L_G) \quad (11)$$

$$\frac{\partial \psi_1(x)}{\partial x}\Big|_{x=L_G} = \frac{\partial \psi_2(x)}{\partial x}\Big|_{x=L_G} \quad (12)$$

Using above mentioned boundary conditions

$$\theta = [\frac{\eta_1}{\chi_1}]V_G + \tau \quad (13)$$

Where,

$$\eta_1 = [(\exp(\sqrt{\gamma}L_G) + \exp(-\sqrt{\gamma}L_G)).(\gamma L_G .\exp(-\sqrt{\gamma}L_G)) + (\frac{2L_G}{\sqrt{\gamma}} - L^2_{in} - 2L_G L_{in})\gamma^{3/2} + 2(\exp(\sqrt{\gamma}L_G) + \exp(-\sqrt{\gamma}L_G)) + 3\gamma - 1] \quad (14)$$

$$\chi_1 = [\sqrt{\gamma}L_{in} + \exp(2\sqrt{\gamma}L_G)] \quad (15)$$

$$\tau = (\frac{1}{\sqrt{\gamma}L_{in} + \exp(2\sqrt{\gamma}L_G)}).[(V_s + V_{bi})\sqrt{\gamma} - 2V_D.\exp(\sqrt{\gamma}L_G) + \exp(-\sqrt{\gamma}L_G)] - [\frac{qN_i}{\varepsilon_{Si}}].(\frac{1}{\gamma} + 3) + \Delta\phi_{ms}\eta_1] \quad (16)$$

Further impact ionization integral M can be used to get I_{ii} expressions.

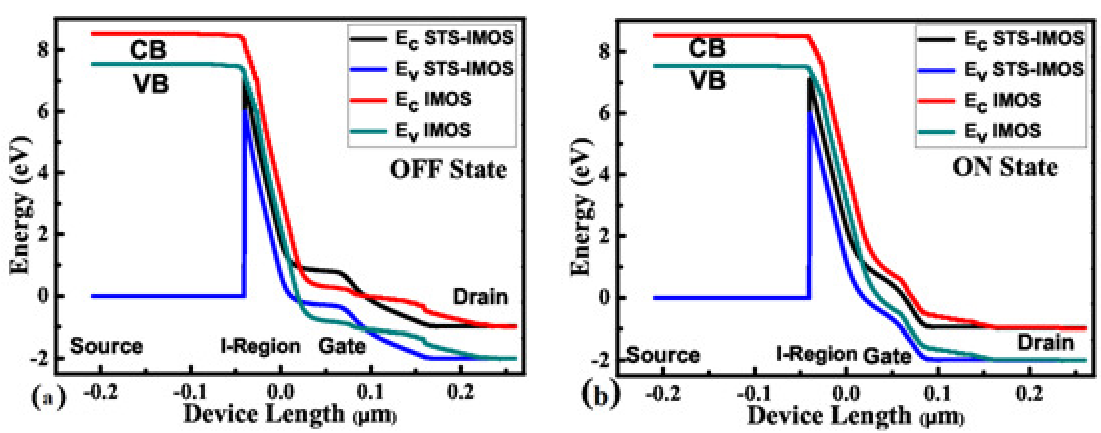

Figure 3. Energy band diagram of STS-IMOS in (a) OFF state, i.e., (V_{GD} = 0 V, V_{SD} < 0 V) (b) ON state, i.e., (V_{GD} > 0 V, V_{SD} < 0 V) along device length with cut-line $X – X'$.

4. SIMULATION RESULTS AND DISCUSSION

Fig. 3(a) depicts energy band diagram along the device length with horizontal cut-line (X-X') at the center of the silicon film for STS-IMOS and conventional IMOS, in OFF state, there is no formation of inversion layer under the gate. Hence, effective channel length is entire i-region. Thus the electric field strength in intrinsic region is not enough to initiate the impact ionization process. This OFF state current is significantly small. A positive gate voltage turns the device ON by creating inversion layer under the gate and now effective channel length is reduced and electric field is intensified under the intrinsic region without the gate. It initiates impact ionization process. ON state energy band diagram along the device length with cut-line (X-X') at the center of the silicon for both devices is shown in Fig. 3 (b). Fig. 4 (a) and (b) exhibit the transfer characteristics ($I_D−V_{GD}$) and breakdown characteristics ($I_D−V_{SD}$) of STS-IMOS and IMOS respectively. TCAD simulations show the threshold voltage of STS-IMOS V_{GT} as 0.25 V and for conventional IMOS it is reported as 0.53 V. Moreover, simulation results observe the breakdown voltage V_{Br} for STS-IMOS as 4.1 V and for conventional IMOS it is 4.9 V. Hence, from simulation results it can be inferred that there is a significant improvement in terms of threshold voltage and breakdown voltage with comparable I_{ON}/I_{OFF} ratio and sub-threshold swing.

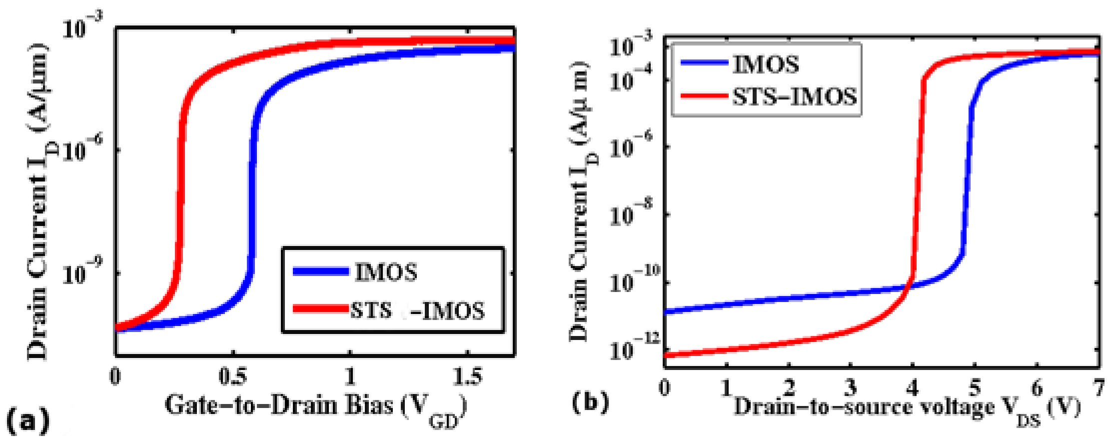

Figure 4.(a) Transfer characteristics ($I_D−V_{GD}$) of STS-IMOS and IMOS, (b) breakdown characteristics ($I_D−V_{DS}$) of STS-IMOS and IMOS.

5. CONCLUSIONS

In this paper, a schottky tunneling source impact ionization MOSFET (STS-IMOS) with silicide source is proposed and investigated to lower the breakdown voltage. It also enhances the performance of conventional impact ionization MOSFET (IMOS). The accumulative effect of impact ionization and asymmetric source induced barrier tunneling is the key feature of STS-IMOS. TCAD simulations validated significant reduction in break down voltage and threshold voltage with comparable SS for STS-IMOS. It shows high immunity against V_{th} fluctuations due to less hot electron damage. Consequently, device reliability is improved significantly.

REFERENCES

[1] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q, in IEEE International Electron Devices Meeting, IEDM Tech. Dig., 2002 pp. 289 –292.

[2] K. Gopalakrishnan, P. B Griffin, and J. D. Plummer, , "Impact Ionization MOS (I-MOS)- Part I: device and circuit simulations," IEEE Transactions on Electron Devices, vol. 52, no. 1, pp. 69 –76, 2005.

[3] K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, Impact Ionization MOS (I-MOS)-part II: experimental results, IEEE Transactions on Electron Devices, vol. 52, no. 1, pp. 77 –84, 2005.

[4] W. Y. Choi, "Applications of impact-ionization metal-oxidesemiconductor (I-MOS) devices to circuit design," Current Applied Physics, vol. 10, no. 2, pp. 444 –451, 2010.

[5] W. Y. Choi, J. Y. Song, J. D. Lee, B.-G. Park, and B.G. Park, "A novel biasing scheme for I-MOS (Impact-Ionization MOS) devices," IEEE Transactions on Nanotechnology, vol. 4, no. 3, pp. 322 –325, 2005.

[6] W. Y. Choi, J. D. Lee,J. Y. Song, Y. J. Park, and B.G. Park, "100-nm n-/p-channel I-MOS using a novel self-aligned structure," IEEE Electron Device Letters, vol. 26, no. 4, pp. 261 –263, 2005.

[7] F. Mayer, C. Le Royer, G. Le Carval, L. Clavelier, and S. Deleonibus, "Static and dynamic TCAD analysis of IMOS performance: From the single device to the circuit," IEEE Transactions on Electron Devices, vol. 53, no. 8, pp. 1852 –1857, 2006.

[8] R. Jhaveri, V. Nagavarapu, and J. C. Woo, "Asymmetric schottky tunneling source SOI MOSFET design for mixed-mode applications," IEEE Transactions on Electron Devices, vol. 56, no. 1, pp. 93 –99, 2009.

[9] Q. Huang, R. Huang, Z. Wang, Z. Zhan, and Y. Wang, "Schottky barrier impact-ionization metal-oxide-semiconductor device with reduced operating voltage," Applied Physics Letters, vol. 99, no. 8, pp. 083507, 2011.

[10] F. Mayer, T. Poiroux, G. Le Carval, L. Clavelier, and S. Deleonibus, "Analytical and compact modelling of the I-MOS (Impact Ionization MOS)," in IEEE 37th European Solid State Device Research Conference, ESSDERC2007, pp. 291 –294.

[11] S. Sentaurus, Release G-2012.06, S-process and S-device simulators, Synopsys, 2012.

[12] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. Wiley, New York, 1981.

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