ARCHITECTURE OF A NOVEL CONFIGURABLE COMMUNICATION PROCESSOR FOR SDR

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ABSTRACT

The design of high performance Digital Signal Processing (DSP) Processors for Software Defined Radio (SDR) with high degree of flexibility and low power consumption has been a major challenge to the scientific community ever since its conception. The basic philosophy of SDR is to implement different modulation or demodulation schemes on the same underlying hardware. Currently available high performance DSP processors, optimized with 'Very Large Instruction Word (VLIW)' architecture and multiply and accumulate (MAC) units, are unable to meet the near real time speed requirements of Software Defined Radios (SDR) due to their inherent sequential execution of compute intensive signal processing algorithms. Moreover, their power dissipation is considerably high. Even though, Application Specific Integrated Circuits (ASIC) exhibit high performance, they are also not suitable because of their lack of flexibility. Various references on FPGA based implementations of reconfigurable architectures for SDRs are also available. However, the Look-up Table (LUT) based implementations of FPGAs are not optimum and therefore, cannot offer highest performance at low silicon cost. Keeping this view, this paper presents the design of a configurable communication processor for Software Defined Radio. The proposed scheme features the performance of an ASIC based design combined with the flexibility of software. Experimental results reveal that the proposed architecture has minimum hardware requirement, improved silicon area utilization and low power dissipation.

KEYWORDS

Field Programming Gate Array (FPGA), Software Defined Radio (SDR), Digital Signal Processing (DSP) Processor, Hardware Description language (HDL), Signal Flow Graph (SFG), Application Specific Integrated Circuit (ASIC), Union of graph, Reconfigurable DSP Processor

1. INTRODUCTION

The communication industry has witnessed substantial changes in digital communication standards. The journey of digital communication commenced with GSM, D-AMPS and PDC systems and gradually, a large portion of digital communication solutions were replaced by WCDMA, HSPA and CDMA 2x standards. Though these 3G standards offer much higher data rate and reliability, customers have now begun leaning towards the services offered by 4G standards with data rates reaching 100 Mbits/s, if not more. To cope up with this ever changing scenario of communication schemes, it is felt that the current developments in communication systems and protocols should not only be of low cost and high efficiency, but also adaptive and reusable. In conventional radio communications, the hardware components used for modulations/ demodulations are fixed for a particular communication scheme. For large varieties of

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applications, particularly for military and cell phone services, radio protocols need to be changed in real time with very high speed. This necessitates the design of a high performance radio system with high degree of flexibility. The "Software Defined Radio(SDR)" [1][2][3][4][5] offers flexible, high performance radio systems where hardware components of modulators/ demodulators are implemented by means of software on different hardware platforms like DSP processors or FPGAs.

Software Defined Radio (SDR) systems [6][7][8][9] are flexible communication systems where components of classical radio systems are replaced by software modules. Implementing different modules (modulators, demodulators, filters etc.) in software has the distinct advantage that SDR systems can be modified on the fly to deploy different communication schemes [10][11] without changing the hardware. Though the concept of SDR has been in existence for more than a decade, introduction of latest Digital Signal processing Processors [12][13] and FPGAs have made newer types of design of SDR possible. The block diagram of a SDR system is presented in Fig.1.

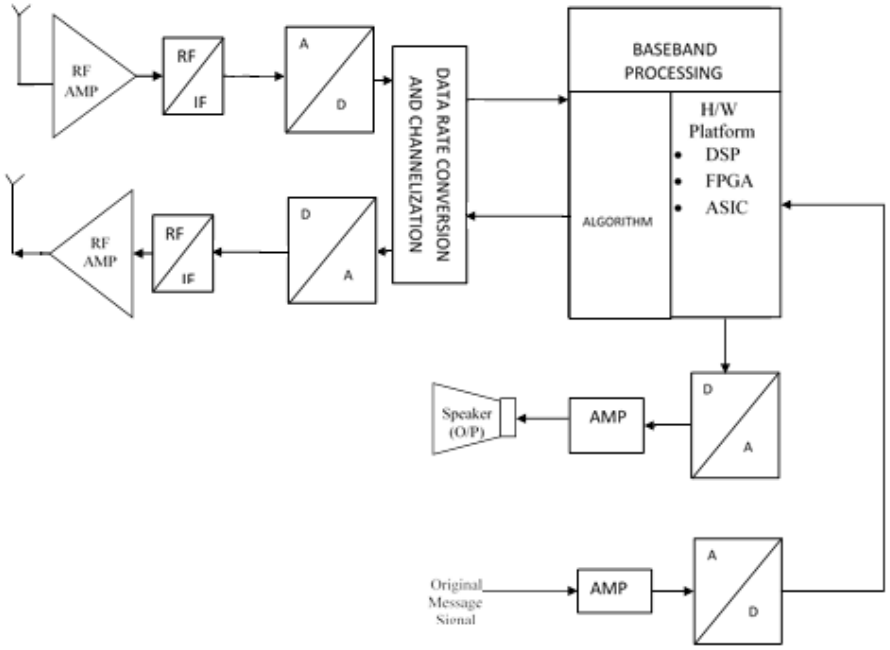

Figure 1. Block Diagram of SDR

Evaluation history and literature survey of SDR reveals that there are various types SDR systems, projects and platforms. Joe Mitola[14] proposed software radio which was a software-based transceiver. He used GSM base station- combination of Ferdensi's digital receiver and E-Systems Melpar's. E-Systems Melpar sold the software radio idea to the US Air Force and Melpar built a prototype commanders' tactical terminal in 1990-91 that employed Texas Instruments TMS320C30 Processors. SPEAKEASY [15] is an open architecture and proves the concept of multi-band, multi-mode software programmable radio operating from 2 MHz to 2 GHz. Tactical radio systems as well as voice and data communications to aircraft and onto battlefield has been used as Military applications and civilian applications. Academic projects, the CHARIOT and SpectrumWare, were funded by DARPA. GNU Radios as well as some European projects has also attracted a large number of SDR developers.

Flexible radio systems are generally implemented on programmable platforms like Digital Signal processing Processors and FPGAs. In the case of DSP based implementation [16][17], programs for the proposed architecture are executed on the DSP processor. Flexibility can be achieved as the programs are easily modifiable. The major problem is that the power consumption in this case is considerably high. Moreover the efficiency of the design will also be limited by the efficiency of the instruction set of that particular digital signal processor. On the other hand FPGA [18][19][20][21][22][23][24] is configured for a particular design by downloading the corresponding bit streams onto FPGA. These bit streams are generated after synthesis of the description of the circuit in some Hardware Description Language (HDL)[25][26] like VHDL, Verilog etc. Changes in these HDL programs will thus be reflected in the final configuration of the FPGA, thereby offering flexibility. However the drawback of FPGA based design lie within the issues of un-optimized Look Up Table (LUT) based implementation, large silicon area usage, high power dissipation, communication delay and considerable configuration latency. On the contrary, Application Specific Integrated Circuits (ASICs) [27] provide lower power dissipation, minimum latency time and higher silicon area utilization factor. The major issue with this type of VLSI [28] based design is lack of flexibility in the architecture.

Considerable effort has been given by designers and researchers to implement software define radio (SDR) system in various platforms, including recent works related to FPGA based implementation[20][21][23][29] of SDR. These designs, though aim to leverage flexibility of FPGAs, are not also free from the drawbacks discussed above. Jignesh Oza et.al;[29] in their work have combine different modulation schemes into a single circuit and have implemented on FPGA but no efforts were made to minimize the hardware requirement. Only selection lines were used for choosing available schemes at a particular instant of time. On the other hand Tadayuki Kamisaka, et. al; [30] proposed modulators where different modulation schemes can be chosen by simply changing the ROM contents. Although it is useful for various data transmission speeds but the operating speed was bottlenecked due to use of non-optimized LUT-based ROMs. FPGA based design of composite of modulation schemes either by selection line or by union method [23](graph theory method) is free from the inherent drawback like high latency time, un-optimized LUT (i.e. poor silicon utilization factor) and high power consumption. On the other hand ASIC based design is highly optimized, low power and high speed without or little flexibility. Hence in this paper, ASIC design of composite modulators and their various level of hardware optimization using graph theory methods (nomenclature, labelling, precedence relationship and union of graph) have been presented in details. This design was also converted into Verilog codes (HDL) and was synthesized by ASIC synthesis tool Synopsis tool sets-Design Vision/design Compiler.

Keeping these issues in view, this paper aims to present a new reconfigurable architecture for an ASIC based SDR architecture which offers high performance at the same time adding flexibility features to overcome the drawback of legacy ASIC based systems.

2. PROPOSED ARCHITECTURE OF RECONFIGURABLE MODULATORS

2.1. Architecture of Reconfigurable Modulators

In the proposed architecture, for case study, a number of different modulation schemes [10] [11] [31] [32] like amplitude shift keying(ASK), frequency shift keying (FSK), binary phase shift keying (BPSK), Quadrature phase shift keying (QPSK) have been considered and the architecture can be configured to work according to any one of the schemes at a given time. The main intention is to perform all these above mentioned modulation operations using the same underlying hardware platform while the software above the hardware layer controls the configuration. The different modulation/demodulation schemes can be visualized as interconnected building blocks where such building blocks are Adder, Multiplier, Comparator,

Multiplexor etc. These building blocks primitives have to be chosen in such a fashion that they are basic enough so that a particular modulation scheme can be made by connecting these primitives in appropriate order. Obviously a number of switches are required to maintain the interconnections among the primitives for implementing a scheme. So, the architecture consists of:

1. A number of primitive building blocks for performing the signal processing functions for different modulation schemes. These blocks include Adder, Multiplier, Comparator, Multiplexor etc.
2. A number of switches for implementing different routing functions, so that by interconnecting different building blocks different modulation schemes can be implemented. These switches can be implemented using Multiplexers.
3. A control unit or Logical unit is required to generate the control signals for configuring these switches. This unit consists of a number of hardware switches and a Decoder. For a particular modulation scheme to be implemented one particular hardware switch is to be on which sends some particular bit fashion to the input of the decoder. The decoder in turn generates the corresponding configuration bit stream for the routing switches to configure that particular modulation scheme.

The main advantage of such architecture is that it can be configured to any one of the large number of modulation schemes by generating different control signals to the Multiplexers / switches resulting the speed of the hardware with the flexibility of the software.

The efficiency of such a scheme depends on the trade-off among three important factors. They are: 1) minimum number of basic building blocks required for configuring to a desired modulation scheme, 2) minimum number of switches required establishing a given modulation scheme, 3) Minimum Routing delay.

Keeping these factors in focus, a graph theoretic approach for hardware optimization has been considered in this paper.

2.2. Graph theoretic approach for minimization of hardware in composite architecture

At first four the modulation schemes were visualized as a connection of primitive building blocks. The same blocks existing in different modulations schemes are then identified and marked with identical names. With these primitive blocks different Signal Flow Graphs (SFG) are drawn for different modulation schemes. By combining the SFGs common blocks are eliminated and hence there will be sufficient hardware reduction in composite circuit. Such practices are discussed in the following subsection.

2.2.1 Nomenclature of primitive building blocks

Same functionality primitive building blocks have given same nomenclatures are as follows: Random Number Generator (S1), comparator (B1), Multiplier (B2), Constant1 (B3), Cosine Generator (S2), Constant2 (B4), Switch1 (B5), Gain(-1) (B6), Switch2 (B7), Adder (B8), Sine wave generator (S3), Switch3 (B9). Using these primitive blocks as nodes and connecting them accordingly, Signal Flow Graph (SFG)s of four modulation schemes have been drawn.

2.2.2 Signal Flow Graph

The Signal Flow Graphs (SFG) of four modulation schemes and their labelling are shown in the following subsection.

2.2.2.a Labelling of SFGs

The labelling procedure has been so adapted that the nodes performing the same function has been labelled by the same symbol in all the signal flow graphs. Further, the same nomenclatures across the all SFGs are also used for the directed branches joining the same pair of nodes. This avoids duplication of nodes and branches. The labels are listed in Table 1.

Table 1. Labels of directed branches in SFGs

Source Node	Destination Node	Label of the directed branch
S1	B1	e1
S1	B8	e2
S2	B2	e3
S2	B5	e4
S2	B6	e5
S2	B7	e6
S2	B9	e7
S3	B6	e8
S3	B7	e9
S3	B9	e10
B1	B2	e11
B1	B5	e12
B1	B9	e13
B3	B1	e14
B4	B8	e15
B6	B5	e16
B6	B7	e17
B8	B7	e18

2.2.2.b SFG representation of four individual modulation schemes

SFG of four individual modulation Schemes following the convention discussed above are shown in Fig. 2, Fig. 3, Fig. 4 and Fig. 5.

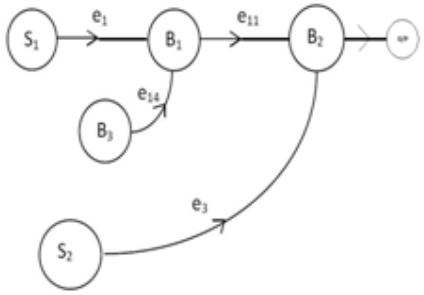

Figure 2. Graph-I (SFG of ASK modulation)

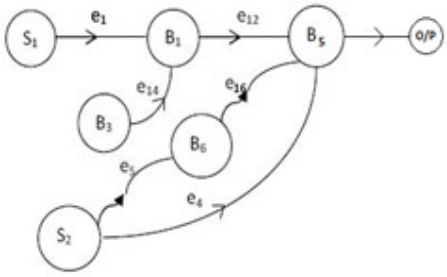

Figure 3. Graph-II (SFG of BPSK modulation)

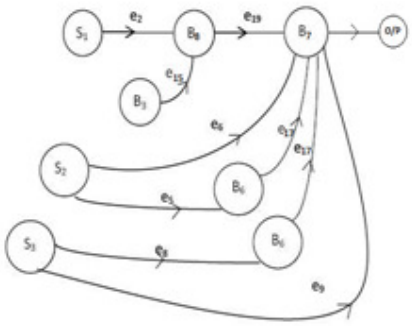

Figure 4. Graph-III (SFG of QPSK modulation)

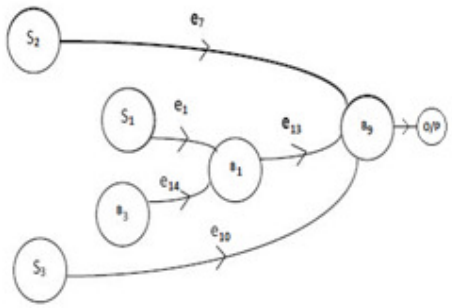

Figure 5. Graph-IV (SFG of FSK modulation)

2.2.3 Construction of a Combined Architecture from the SFGs

In the previous section, the four SFGs for four modulation schemes have been presented. Now using these SFGs and applying the graph theoretic operations [33] like "precedence relationship" and "union of graph" to these SFGs, a new SFG can be developed for proposed architecture. Union of graph property is used to eliminate the common portion of the different graphs. However a combined signal flow graph resulting merely from union of graph would produce erroneous results unless the order of data processing i.e. signal dependency in individual SFGs remains preserved in the combined SFG.

2.2.3.a Precedence Relationship

In constructing network diagrams which represents any project comprising of several activities, preserving precedence relationship is important so that the order of activities be properly represented. In this work two standard operation research methods i.e. PERT and CPM methods are used. Assuming that the time required by the signal to flow across all the branches are same the weight of all branches are considered as 1. Now the precedence relationship for the four modulation schemes is as follows:

For ASK (Graph-I): e1<e11, e14<e11 i.e. e1, e14<e11;

For BPSK (Graph-II): e1, e14<e12, e5<e16;

For QPSK (Graph-III): e2, e15<e18, e5, e8<e17;

For FSK (Graph-IV): e1, e14< e13;

2.2.3.b Union of Graphs

In graph theory, the union of two graph is defined as follows: IF G1 is a graph with vertex set v1 & edge set E1 and G2 be another graph with vertex set V2 & edge set E2 then their union denoted by G1 U G2 is a graph with vertex set is V1 U V2 & edge set is E1U E2. Since the union operation excludes duplicate entry of set elements, the union of two signal flow graphs union will provide the minimum possible number of vertex and edges without affecting the desired functionality of the combined network or combined system provided the precedence of operations are not disrupted. Fig.6 and Fig.7 depicts the two individual directed graphs G1 and G2. Fig. 8 represents the union of two graphs G1 and G2. Now the pair of nodes (V1, V2) and their connecting branch (e1) is same in both G1 and G2. But the resultant graph from the union operation of G1 and G2 will have no duplication of nodes or branches.

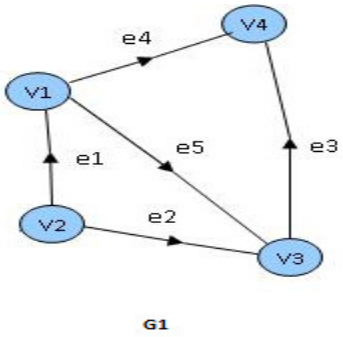

Figure 6. Directed Graph G1

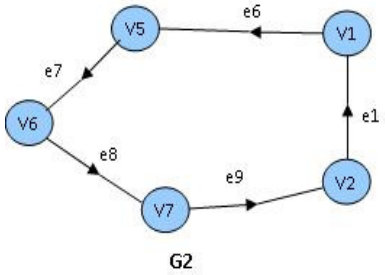

Figure 7. Directed Graph G2

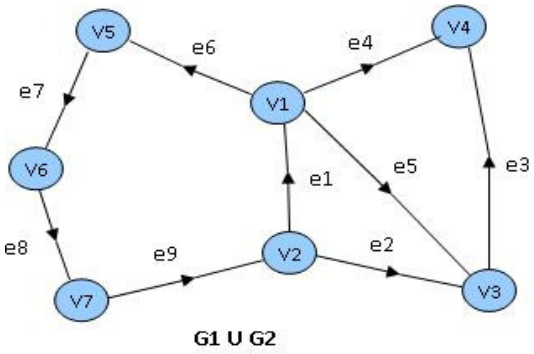

Figure 8. Result of Union Operation G1U G2

In first step of union operation to construct the combined architecture, Graph-I and Graph-II are combined using the Union and preserving the precedence relationship. The nodes S1, B1, S2 and B3 are the common nodes in the both graph. These common nodes are combined strictly adhering to the precedence relationship. The principle being the same pair of nodes and their connecting branches having same directed path are merged. The node pair (S1, B1) and connecting branch e1 being present in both the graphs (Graph-I and Graph-II). The same thing is applicable for the node pair (B3, B1) and connecting branch e14. The resultant graph from the union of graph operation is shown in Fig.9.

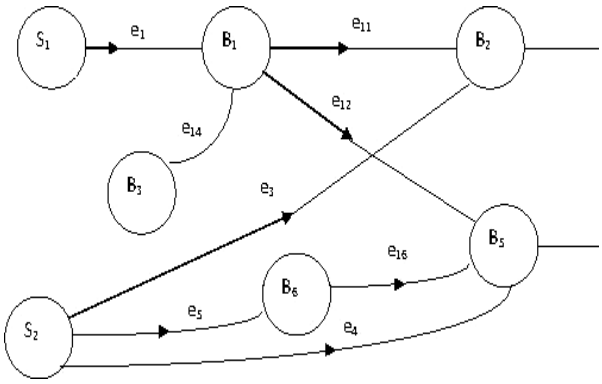

Figure 9. Graph Showing Graph-I U Graph-II

In this work the union of graph operation has been applied in the following fashion to obtain the combined SFG:

Step 1: (Graph-I) U (Graph-II)

Step 2: (Graph-I) U (Graph-II) U (Graph-III)

Step 3: (Graph-I) U (Graph-II) U (Graph-III) U (Graph-IV)

During the operation the following points were observed. In the above case (B1, B1, B1), (B6, B6, B6) are the repeated internal nodes. B1 follows the same pair of branches e1, e14 in all the three graphs I, II & IV. Hence the sum of the incoming signals is same in the all three graphs. The outgoing signals, although different, do not affect the output of the combined system. Hence node B1 will appear once. The repeated node B6 is represented in the Fig.10. The precedence relationship of this repeated node are e16>e5, e17>e5, e17>e8 i.e. e16>e5, e17>e5, e8. Hence the combined digraph will need a "Dummy branch" shown in dotted lines depicted in Fig. 12. The final combined SFG is shown in Fig. 13 which is the union of all four graphs.

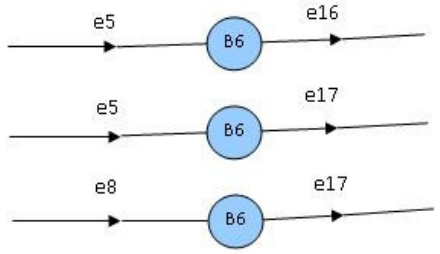

Figure 10. Same node B6 but with different input-output branches

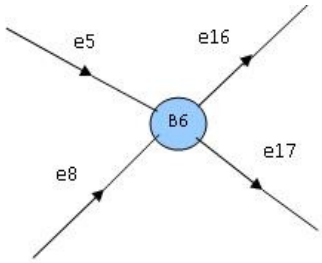

Figure 11. Graph for Precedence Relationship e16 > e5, e17> e5,e8

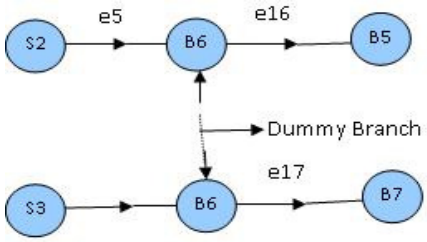

Figure 12. Graph for dummy branch (Shown in dotted line)

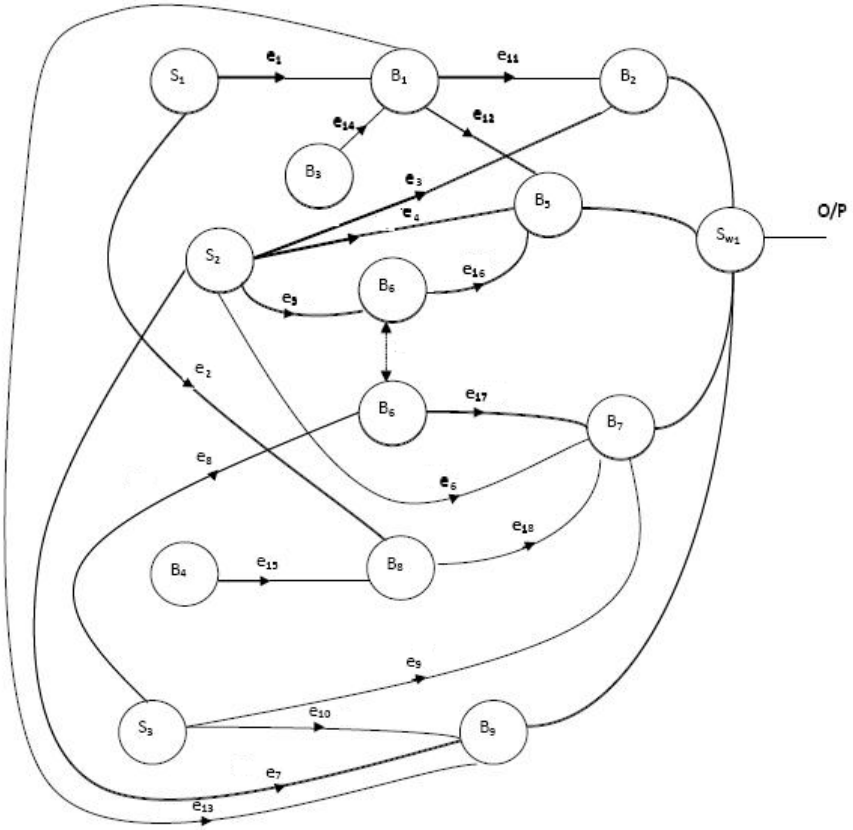

Figure 13. The Composite Graph

3. ASIC IMPLEMENTATION OF COMPOSITE MODULATORS

3.1. Synthesis results for ASIC implementation of individual modulation schemes

The Synthesis report of VERILOG codes of four individual modulation schemes and combined modulation scheme using Design Vision / Design Compiler [34]–a Synopsys tool has been presented and also graphically represented in Fig. 14, Fig. 15 Fig. 16, Fig. 17 and Fig. 18.

Library(s) Used for both Area and Power calculation:
vtvt_tsmc180(File:home/ue/my_cadence_directory/vtvt_tsmc180_release/Synopsys_Libraries/libs/vtvt_tsmc180.db)
Power calculation parameters:
Operating Conditions: nom_pvt
Wire Load Model Mode: top
Global Operating Voltage = 1.8
Power-specific unit information:
Voltage Units = 1V , Capacitance Units = 1.000000ff
Time Units = 1ps , Dynamic Power Units = 1mW (derived from V, C, T units), Leakage Power Units = 1mW

HDL Synthesis Reports of all four Individual Modulation Schemes:
Area Report:

ASK:
Number of ports: 40
Number of nets: 77
Number of cells: 45
Total cell area: 1965.675575

FSK:
Number of ports: 40
Number of nets: 47
Number of cells: 15
Total cell area: 946.096199

QPSK:
Number of ports: 40
Number of nets: 131
Number of cells: 99
Total cell area: 4465.853958

BPSK:
Number of ports: 40
Number of nets: 91
Number of cells: 59
Total cell area: 2758.317297

Power Report:

ASK:
Cell Internal Power = 84.2933 mW (64%)
Net Switching Power = 47.8766 mW (36%)
Total Dynamic Power = 132.1700 mW (100%)
Cell Leakage Power = 986.6118 pW

FSK:
Cell Internal Power = 71.1495 mW (80%)
Net Switching Power = 18.1995 mW (20%)
Total Dynamic Power = 89.3489 mW (100%)
Cell Leakage Power = 591.1196 pW

QPSK:
Cell Internal Power = 121.3645 mW (73%)
Net Switching Power = 44.8811 mW (27%)
Total Dynamic Power = 166.2456 mW (100%)
Cell Leakage Power = 2.4679 nW

BPSK:
Cell Internal Power = 132.3196 mW (67%)
Net Switching Power = 66.1420 mW (33%)
Total Dynamic Power = 198.4616 mW (100%)
Cell Leakage Power = 1.5080 nW

HDL Synthesis Reports of the Proposed Configurable Combined Architecture:

Area:

Number of ports: 56
Number of nets: 181
Number of cells: 133
Number of buf/inv: 17
Total cell area: 5845.632261

Power:
Cell Internal Power = 168.4776 mW (66%)
Net Switching Power = 88.5400 mW (34%)
Total Dynamic Power = 257.0177 mW (100%)
Cell Leakage Power = 3.0346 nW

3.2. Analysis of the Synthesis Report

References are available in literature featuring different modulation/demodulation schemes in a single architecture. However in the reported works combined circuits where implemented mainly aggregating the individual circuits and the selection lines to choose a particular modulation /demodulation scheme at any particular instance. On the contrary here in this work, the ASIC based design, the hardware requirements of the combined circuits have been minimized using union of graphs and ASIC synthesis tool –Synopsis tool like Design Vision/ Design Compiler. Although FPGA implementation of different modulation schemes using union of graph shown in literature but due to inherent drawback of FPGA like configuration latency, un-optimized LUT and high power consumption this paper suggest ASIC implementation of four composited modulation scheme with optimal union of graph. Various Graphs have been plotted form the ASIC synthesis results. From the graphical analysis of the cell area usage experimental data shown in Fig. 14, it can be clearly derived that the total cell area required to implement the combined architecture is significantly less than the sum total of the all individual implementation. The power analysis shown in Fig. 15 also reveals that the combined scheme requires substantially less power compared to the total power requirement to implement the modulation schemes individually. The port, net and cell analysis, switching and dynamic power analysis as well as cell leakage power analysis depicted in Fig. 16, Fig. 17 and Fig. 18 also show that the implementation of the modulation schemes in the combined architecture is better than implementing the modulation schemes individually.

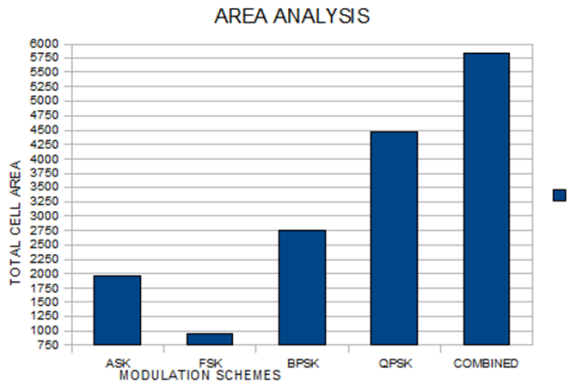

Figure 14. Area Analysis of individual and combined schemes

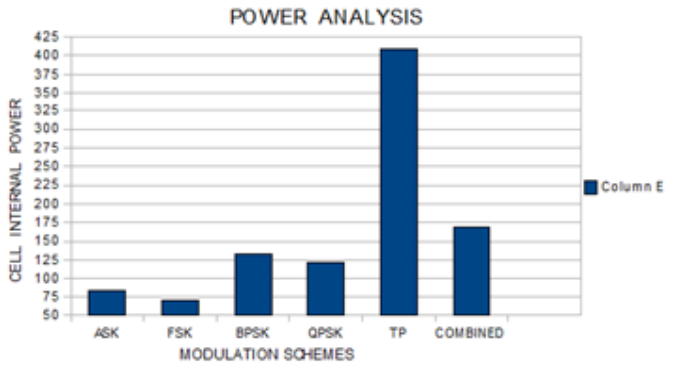

Figure 15. Cell Internal Power of individual and Combined Schemes

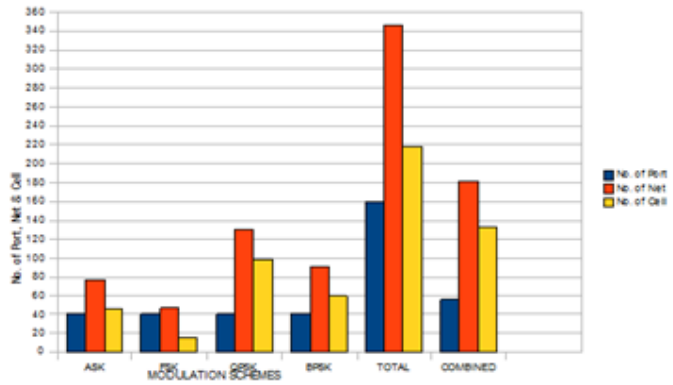

Figure 16. Number of Ports, Nets and Cells Versus individual and Combined Schemes

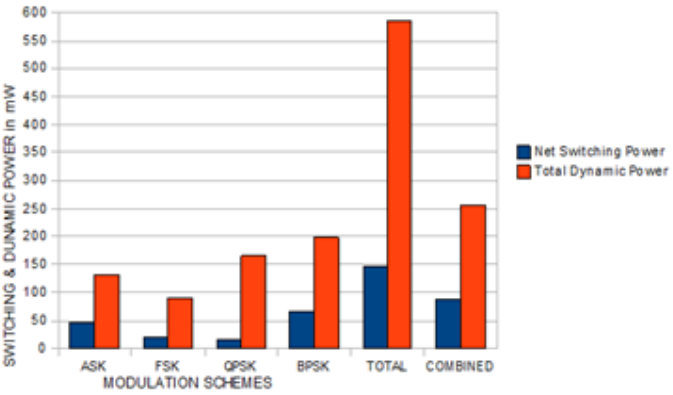

Figure 17. Switching and dynamic power analysis of individual and Combined Schemes

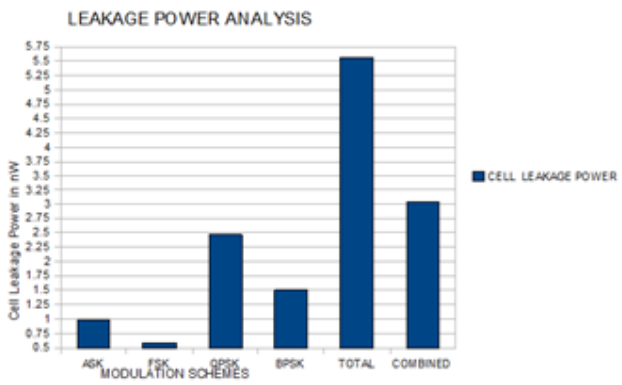

Figure 18. Cell Leakage Power Analysis of Individual and Combined Schemes

4. CONCLUSIONS

In this paper feasibility of ASIC implementation of a novel architecture of Reconfigurable DSP Processor for Different Modulation Schemes with optimum hardware requirements has been explored. The synthesis reports derived from the Synopsis tool have also been presented. It can be concluded from the synthesis results that the ASIC implementation has substantially reduced area and power requirements. The architecture is flexible because run time configuration for any particular modulation scheme can be achieved by activating few switches only. Thus the proposed architecture provides high performance of while retaining flexibility reduced power requirements and improved silicon utilization factor.

To achieve enhanced performance, unions of the set of building blocks for different modulation / demodulation schemes have been combined. Since the performance of most of the building blocks depend on the speed of adders ,multipliers , exploring the possibilities of implementing these arithmetic units using non-binary systems can be thought of . The choice of number system can influence the execution speed of the arithmetic computation to a great extent. Recent studies in computer arithmetic have unleashed that use of number systems like Double Base number System[35], Ternary Number System[36], Logarithmic Number system [37], Single Digit Triple Base Number System[38] etc. can improve the performance of digital signal processing to a great extent. Thus, the performance of the proposed configurable communication Processor for SDR may further be improved by leveraging the advantages of the non-conventional number systems. This study is a potential future research issue related to the current work.

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