A NOVEL ARCHITECTURE OF RNS BASED LIFTING INTEGER WAVELET TRANSFORM (IWT) AND COMPARATIVE STUDY WITH OTHER BINARY AND NON-BINARY DWT

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ABSTRACT

In this paper, a novel architecture of RNS based 1D Lifting Integer Wavelet Transform (IWT) has been introduced. Advantage of Residue Number System (RNS) based Lifting Scheme over RNS based Filter Bank and non-binary IWT has been discussed. The performance of traditional predicts and updates stage of binary Lifting Scheme (LS) for Discrete Wavelet Transform (DWT) generates huge carry propagation delay, power and complexity. As a result non binary number system is becoming popular in the field of Digital Signal Processing (DSP) due to its efficient performance. In this paper also a new fixed number ROM based RNS division circuit has been proposed. The proposed architecture has been validated on Xilinx Vertex5 FPGA platform and the corresponding result and reports are shown in here.

KEYWORDS

Discrete Wavelet Transform (DWT), Integer Wavelet Transform (IWT), Residue Number System (RNS), modulo RNS division, Lifting Scheme (LS), Digital Signal Processing (DSP), Filter Bank (FB).

1. INTRODUCTION

Nowadays, the Discrete Wavelet Transform (DWT) [10, 8] has become very powerful and widely used tool in our advance DSP and Image processing filed due to its excellent locality in time frequency domain. For the last two decade the wavelet theory has been studied by many researchers [1-3] to answer the demand of better and more appropriate functions to represent the signals than the one offered by the Fourier analysis. Defining DWT by Mallat [1] discussed the possibility of its digitally hardware and software implementation [1]. The FIR filter and subsampling used to implement the classical DWT. To develop many research algorithms which has been applied to reduce the computational complexity [2]. The first lifting scheme for DWT had established by Sweldems in 1996, which is very simple and easily developed by hardware [3]. The main concept of the lifting scheme is to break the high pass and low pass filter and convert it into sequence of triangular matrix [4]. The Lifting scheme often requires fewer computations compared to the convolution based DWT [3, 4] and offers many other advantages.
The main motive to use Residue Number System because it helps to reduce the large integer number to smaller integer numbers, so that computation may be performed more efficiently. It based on the Chinese remainder theorem of modular arithmetic for its operation, a mathematical idea from Sun Tsu Suan-Ching (Master Sun's Arithmetic Manual) in the 4th century AD. Due to absent of carry propagation in RNS domain the realization of high-speed, low-power and efficient system can be achieved and it is helpful in signal and image processing. RNS is very useful for

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high speed applications such as digital signal processing, communications, image processing, speech processing, and transforms, all of which are extremely important in computing today.

This paper has been introduced the development of novel architecture for Lifting based 1D RNS IWT for FPGA. There are two reasons behind the motive of this novel architecture. First, wavelet transform is widely used in various high speed applications. And secondly, the advance VLSI technology needs to reduce the cost of building of practical DSP systems and its applications. The advantages are to reduce the arithmetic to a set of concurrent operations that we get from RNS. In this paper we also nullified the problem to implement the fixed number RNS divider circuit by replacing special ROM based approach.

In this paper we are going to discuss the theoretical background of Residue Number System, discrete wavelet transform, lifting scheme, RNS based modulo adder and divider circuit in section 2. Section 3 provides the novel RNS based architectures. Experimental results are reported in section 4. Conclusion and references are drawn in section 5 and section 6.

2. THEORETICAL BACKGROUND

2.1. Residue Number System

Today stringent performance, area, power and time-to-market are the basic challenge and requirements for any kind of DSP and Embedded processors. Sequential carry propagation, power and complexity are main limitation of binary number system. The Residue Number System is the only non-binary system which has an ability to overcome this above limitations and also provide parallel architecture simultaneously.

An RNS is defined by a set of N integer constants is called the moduli. The moduli-set is denoted as {m1, m2 …mn} where 'mi' is the ith modulus. Each integer X can be represented as a set of smaller integers called the residues. The residue-set is denoted as {r1, r2… rn} where 'ri' is the ith residue. The residue 'ri' is defined as the least positive remainder when X is divided by the modulus mi. This relation between them is shown below

$$X \bmod m_i = r_i \quad \text{(1)}$$

The same expression can be written as:

$$\left| X \right| m_i = r_i \quad \text{(2)}$$

The two notations will be used throughout this paper. All integer X can be represented uniquely by using RNS if the X lie within the dynamic range. The dynamic range is determined by the moduli-set {m1, m2 …mn} and denoted as M where:

$$M = \prod_{i=1}^{n} m_i \quad \text{(3)}$$

All integers in the range between 0 and M-1 can be uniquely represented by RNS. If the integer X is greater than M-1, the RNS representation repeats itself. Therefore, more than one integer might have the same residue representation.

2.2. Discrete Wavelet Transform (DWT)

By using high pass and low pass filter banks, the DWT can be implemented and each filter of the filter bank is directly connected with downsampler by two [7, 8, 9].X is the input signal of 1-D

DWT which has been connected with two parallel high pass and low pass filter. The output of the two filters are downsampled by two and produce "d" and "s as shown in Figure1. The *parallel filters (h* and g) represent the analysis filter *bank* [8]. The output signals *of the two filters* are expressed as follows*:*

$$y_L(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + ... + h_N z^{-N} \quad \text{..... (4)}$$

$$y_H(z) = g_0 + g_1 z^{-1} + g_2 z^{-2} + ... + g_M z^{-M} \quad \text{..... (5)}$$

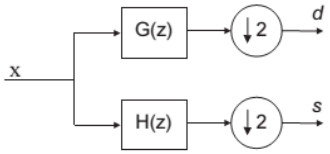

Fig1. Filter Bank Block Diagram

2.3. Lifting scheme (LS)

The basic structure of Lifting scheme for biorthogonal wavelet has been discussed below (see fig:-2) [3].

Split: In this stage, the input signal has divided into two even and odd parts. The even and odd samples are $x_e[n] = x[2n]$ and $x_0[n] = x[2n+1]$. This stage is called lazy wavelets because without splitting we don't require any arithmetic or logical operation.

Predict: The Predict block generates the wavelet coefficient d[n] and easily predict odd samples from even samples using predicts operator 'P':

$$d[n] = x_0[n] - P(x_e[n]) \text{.....(6)}$$

Update: Here we recombine $x_0[n]$ and d[n] and generate the scaling coefficients c[n]. This is skilled by applying an update operator U to the wavelet coefficient and adding to even samples:

$$c[n] = x_e[n] + U(d[n]) \text{ .....(7)}$$

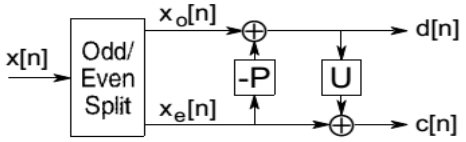

Fig: 2 Lifting stages: split, predict and update

These are the three basic stages of lifting scheme [14]. We calculated equations (6) and (7) for prediction and update block respectively. In general for various type wavelet the number and arrangement of P and U blocks in the lifting structure are different [14].

Now we can write matrix equations for P and U blocks respectively as following

$$\begin{bmatrix} x_{even}(z) \\ d(z) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ t(z) & 1 \end{bmatrix} \begin{bmatrix} x_{even}(z) \\ x_{odd}(z) \end{bmatrix}$$

$$\begin{bmatrix} c(z) \\ d(z) \end{bmatrix} = \begin{bmatrix} 1 & c(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_{even}(z) \\ d(z) \end{bmatrix}$$

Where $p = \begin{bmatrix} 1 & 0 \\ t(z) & 1 \end{bmatrix}$ and $U = \begin{bmatrix} 1 & c(z) \\ 0 & 1 \end{bmatrix}$

Generally, if we have more than one lifting step, the matrix equation is (3).

$$\begin{bmatrix} c(z) \\ d(z) \end{bmatrix} = \begin{bmatrix} k & 0 \\ 0 & 1/k \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \text{ …….. (8)}$$

In equation (8) k and 1/k are normalization factor and t (z) and s (z) are related to filter coefficient in filter bank structure. The relation between FB coefficient and LS equation is (3):

$$E(z) = \begin{bmatrix} h_e(z) & h_0(z) \\ g_e(z) & g_0(z) \end{bmatrix} = \begin{bmatrix} k & 0 \\ 0 & 1/k \end{bmatrix} \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix}$$

Where E (z) is called the Polyphase matrix.The inverse of the lifting scheme is exactly same and easily calculated, even if P and U are nonlinear. Rearranging equation (6) and (7), we get

$$x_e[n] = c[n] - u(d[n]) \text{ …….. (9)}$$

$$x_0[n] = d[n] + P(x_e[n]) \text{ …. …… (10)}$$

2.4. Modulo adder

In this subsection modular adders have been described. The modulo adder is one of the basic important arithmetic units in RNS operation [16]. The basic idea of modulo addition of any two numbers X and Y with respect to modulus m is

$$\begin{aligned} |X+Y|_m &= X+Y && \text{:X+Y<m…… (11)} \\ &= \text{X+Y-m} && \text{: X+Y} \geq \text{m} \\ & && \text{Where } 0 \leq \text{X, Y< m.} \end{aligned}$$

The basic implementation of equation (11) is shown in fig: 3. After first addition the output 'S' is directly connected to the first input of the MUX and again the output 'S' is also connected to the input of the 2nd conventional adder whose another input is complement of m ($\overline{m}$). The output of the 2nd adder 'S-m' is connected to the next input of the previous MUX and carry out of the 2nd adder is directly connected to the select line of this MUX. The whole idea is that if $\mathbf{c_{out}}$ is 0 means X+Y< m and if $\mathbf{c_{out}}$ is 1 means X+Y ≥ m.

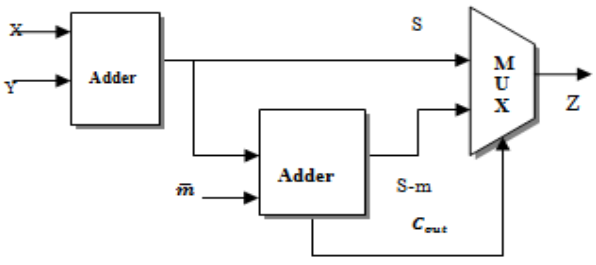

Fig: 3 basic modulo adder circuit

2.5. Modulo divider

Derive and implementation of RNS division is really difficult and this is also the drawback of RNS. If the number divides with a fixed integer number and the result is also an integer number then it is little bit easier to implement by using ROM. ROM based approach we can only use when any kind of architecture is difficult to implement by using conventional method and FPGA is a best platform where ROM is very easy to use.

The main logic behind this architecture is that we consider a number 'r' (in RNS domain it is r_1, r_2 and r_3) which divides by an integer number 'n' and its result is also an integer number 'y'. Again output y splits into y_1, y_2, y3 in RNS domain. The input address of the ROM is the number 'r' which is divided by 'n' and the output of each corresponding address is the result of RNS division. The figure-4 shown the modulo divider circuit.

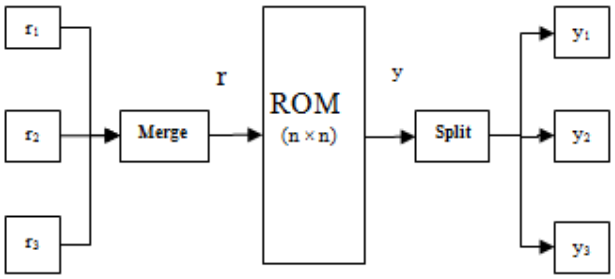

Fig: 4 RNS divider circuit

3. PROPOSED ARCHITECTURE

3.1. ROM based RNS 1D IWT using lifting scheme

In this section, we will first propose a novel ROM based RNS architecture for 1D 5/3 IWT using lifting scheme. In this architecture, three basic building blocks which will repeat for each and every level of decomposition [16]. In these three blocks, the split block is very simple and easy to implement. The job of this block is to separate the input samples into two parts: one is even and another is odd. The diagram of the split block is shown in fig 5. But implement the other two blocks (predict and update) are more critical than first one. A new implemented architecture is designed by pipeline technique.

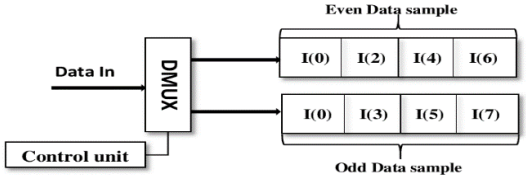

Fig 5: implemented split blockReview Process and Submission

3.2. Implemented structure of 1-level 1-D RNS based predict block:

The Predict block of Integer Wavelet Transform coefficient as the error in predicting the odd samples from even samples based on given four formulas:

$$D_1 = D_1 - \left[\frac{1}{2}(S_1 + S_{2)} + \frac{1}{2}\right] \ldots\ldots\ldots\ldots (10)$$

$$D_2 = D_2 - \left[\frac{1}{2}(S_2 + S_{3)} + \frac{1}{2}\right] \text{..... (11)}$$

$$D_3 = D_3 - \left[\frac{1}{2}(S_3 + S_{4)} + \frac{1}{2}\right] \text{..... (12)}$$

$$D_4 = D_4 - \left[\frac{1}{2}(S_4 + 0) + \frac{1}{2}\right] \text{..... (13)}$$

Where D_1, D_2, D_3, D_4 are odd samples and S_1, S_2, S_3, S_4 are even samples. To implement the hardware of these formulas, we have used three shift registers to store S_1, S_2, S_3, S_4 for three different modules and used another three shift registers to store the value of D_1, D_2, D_3, D_4[16].

Each output of first three shift register is directly connected with modulo adders and the output of each adder is merged. The merged output is also connected with ROM based RNS multiplier. The output of this multiplier again split through RNS splitter circuit and store the output in last three shift registers. The simulated RNS based Predict block is shown in fig-6(a).

3.3. Implemented structure of 1-level 1-D RNS based Update block

The implementation of RNS based update block is exactly same as predict block, but the only difference is that it's accept odd number of samples of the input signal. The four basic formulas which helps to calculate the update coefficient and the hardware is based on this formulas. The implemented and simulated RNS based update block is shown in fig 6(b).

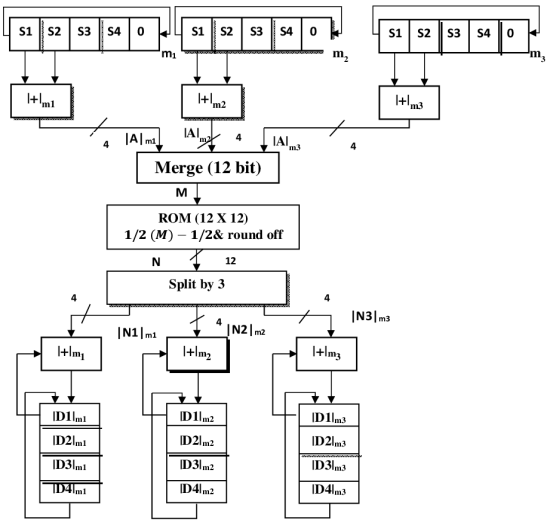

Fig-6(a) RNS based Predict block

Here the first level decomposition is discussed but the 3 level decomposition is exactly same and the hardware usage is reduced from upper level to lower level [16].

Finally the output of the Integer Wavelet Transform is converted by the RNS to binary converter using Chinese Remainder Theorem (CRT) technique.

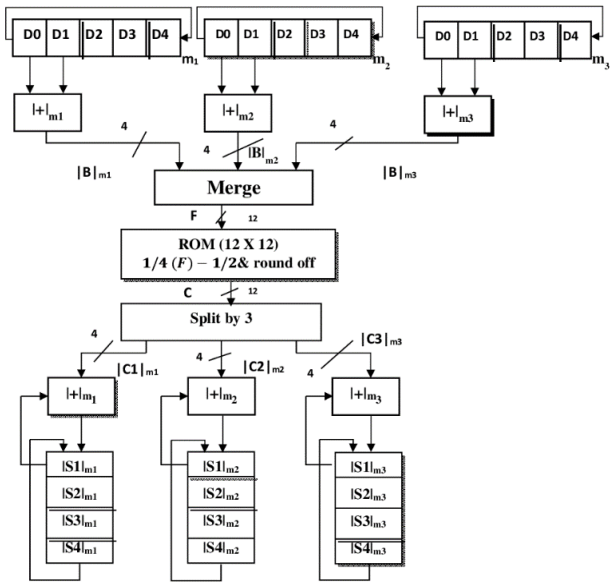

Fig-6(b) RNS based Update block

4. EXPERIMENTAL RESULT

In this section the performance comparison among 1D 1st level novel RNS based Lifting IWT, RNS based filter bank, binary IWT and tipple based IWT has been reported. Here also we have mentioned the time, power, and complexity of our architecture. Each and every module of this novel architecture has utilized 100% hardware. Efficiency of our architecture has been clarified from the table-1 and fig-7 and 8.

TABLE 1: Comparison of resource utilization, power and time summary:

Architecture's list	Adder	Multiplier	Shift register	Delay (ns)	Power (w)
Proposed architecture	6	1	6	4.128	1.332
RNS based DWT	18	24	6	6.332	0.58
Binary DWT	22	24	6	7.814	1.787
Triple based DWT	13	8	6	4.558	1.559

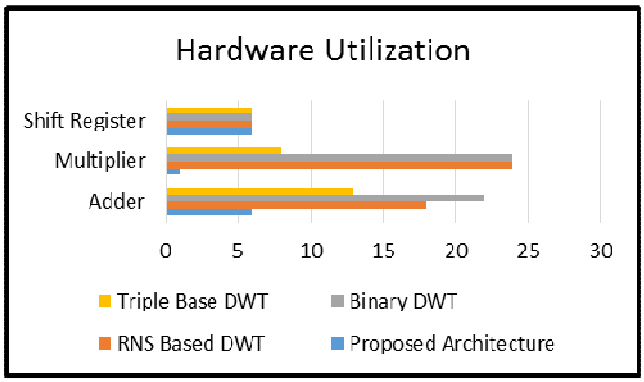

Fig 7 Hardware Utilization

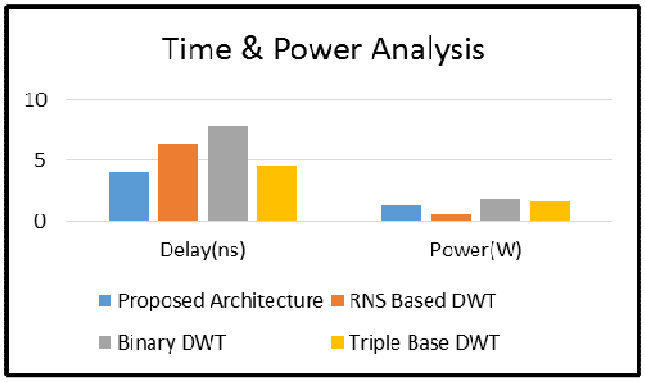

Fig 8 Time & Power Analysis

5. CONCLUSION

In this paper a novel architecture and its related hardware like ROM based RNS multiplier has been designed and simulated.

The major contribution of this architecture is divided into two parts. First of all we have designed an efficient ROM based reconfigurable RNS multiplier which can use for multilevel decomposition. Secondly, we represent a new efficient RNS based Lifting Integer Wavelet Transform.

The simulated and experimented result shows that our architecture is better than other existing architecture in term of complexity, delay and power. In the field of VLSI, DSP and communication this architecture could very effective and perform efficiently.

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