A NOVEL METHODOLOGY OF SIMULATION AND REALIZATION OF VARIOUS OPAMP TOPOLOGIES IN 0.18μm CMOS TECHNOLOGY USING MATLAB

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ABSTRACT

This paper presents a novel methodology of simulation and realization of a various Op-amp topologies, such as two-stage, telescopic and folded cascade are discussed in this paper. The aim of the present work is the development of a tool box which contains the Matlab code to allow automated synthesis of Analog circuits. This tool box is used to find the transistor dimensions (i.e.., width and length) in order to obtain the performance specifications of a two stage op-amp, telescopic op-amp and folded cascode op-amp. In This paper five parameters are considered such as Gain (G), Unity gain frequency (UGF), Phase margin (PM), Slew rate (SR) and Power consumption(P). The designs have been simulated by using 0.18μm CMOS technology with a supply voltage of ±1.8v.Finally, a good agreement is observed between the Matlab based tool box and electrical simulation.

KEYWORDS

CMOS amplifier, two-stage amplifier, telescopic amplifier, folded cascode amplifier, Matlab based Tool box

1. INTRODUCTION

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design[3].op-amps with vastly different levels of complexity are used to realize functions ranging DC bias generation to high-speed amplification or filtering[5]. The present scenario allows the circuit designer only to follow the manual procedure which contains about fifteen steps to get the W/L values of the transistors. For less complex circuits the circuit designer can follow the manual procedure to get the W/L values of the transistors but if the designer makes any mistake in the design procedure then the complete design will be in error in other words the designer will have to repeat the design procedure once again and calculate the W/L values of the transistors. So this shows that even a small and less complex circuit will require a long time to be implemented if the designer makes even a single mistake, then for complex circuits the design will take more time just to get the W/L values of the transistors [6]. This shows that designing of a circuit is time consuming and becomes difficult for complex circuit designs. So there is a need to improve the present scenario of circuit design, which leads to this paper, which is able to calculate the W/L

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values of the transistors without even putting pen on paper. This is achieved by placing the same manual design procedure steps in the form of a code using Matlab. The code while running, ask the user or the circuit designer to enter the desired specifications after, which the code will automatically calculate the W/L values of the transistors and is shown as an output on the command window of Matlab. This output, is nothing but the W/L values of the transistors calculated by the code itself. This output on the command window may not be understandable to the user or the circuit designer, so the Matlab tool named GUI (graphical user interface) is used, which will not only represent the W/L values of the transistors but also the circuit diagram and the specifications used in the design.

This paper is organized into five sections. In section II various op-amp topologies discussed. In section III a developed novel methodology for three op-amp topologies are discussed. In section IV presents the simulation results of three op-amp topologies finally, section V concludes the paper.

2. OPERATIONAL AMPLIFIER TOPOLOGIES

In this section, three types of op-amp topologies will be discussed and their performances will be compared. These topologies comprise two stage, telescopic and folded cascode op-amps. The merits and de-merits of each circuit will be highlighted.

2.1Two-stage op-amp

The two stage op-amp circuit is shown in Fig. 1.This topology consists of eight transistors, with each transistor performing a specific function .Transistor M1 and M2 are the input for the differential amplifier (stage-1), which converts voltage signals into current. Transistors M3,M4,M5 and M8 act as a current mirror, while transistor M6 and M7 form the second stage amplifier .This circuit has the advantage of providing higher gain because the second stage provide higher output voltage swing .The disadvantage of the circuit is that it consumes more power and gives negative power supply(PSR) at higher frequencies[12].

Two-stage Op-Amps are used for their ability to provide more gain and swing. Basically, the second stage provides about 5-15 dB gain, which is not very high. But the higher output swing provided by the second stage is crucial to some applications, especially with lower supply voltages in today's technologies.

So, the second stage is a simple amplifier like a CS stage.

2.2 Telescopic op-amp

The telescopic op-amp circuit is shown in Fig. 2.This circuit is called a Telescopic cascaded op-amp because the transistors are cascades between the power supplies in series and the transistor in the differential pair. This design increases the output impedance and voltage gain due to the cascade transistor and as lower power consumption compared to other topologies. Its output swing is very small and it is not suitable for applications where the input and output need to connect directly since it reduces its linearity range [11].

One of the drawbacks of this implementation is the limited output swing. Each transistor cascaded on top of another one, adds an overdrive voltage to the headroom of output branch which will limit the output swing.

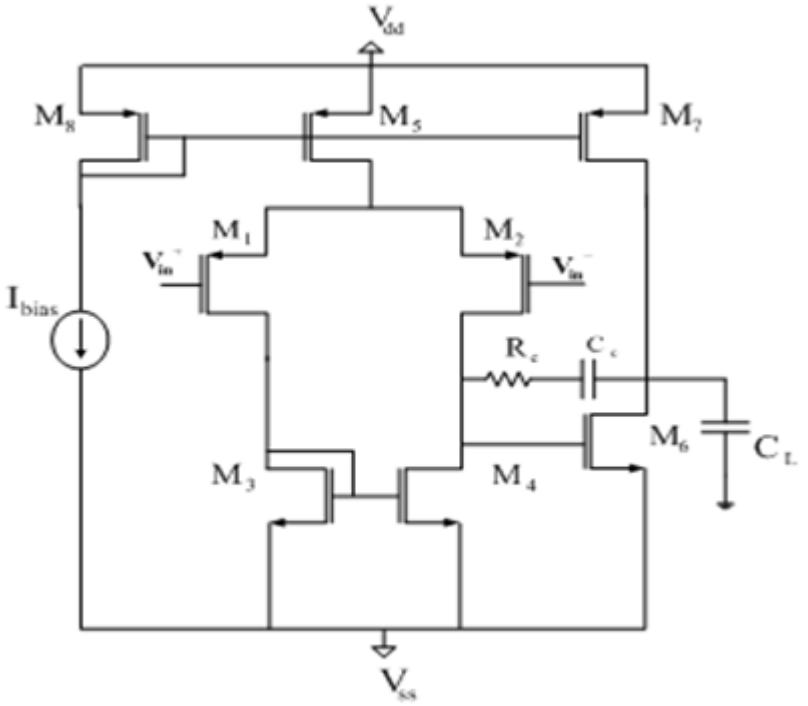

Fig. 1: Two stage Op-amp

Another drawback is that extra poles are added to the small-signal transfer function of the Op-Amp, exacerbating stability issue.

To achieve fully differential configuration current-source loads are used which at the same time will help with high gain requirement as well. It is informative to mention that diode-connected loads are used in single-ended output Operational Amplifiers' implementations and they exhibit a mirror pole introduced to the transfer function.

2.3 Folded cascode op-amp

The Folded cascode op-amp is shown in Fig. 3.This topology consists of an input differential pair, two cascades and one current mirror. It utilizes the high swing and gain can be achieved because cascode at the output are used. However, the current consumption is twice of the telescopic stage due to additional current mirror. The main advantage of folded cascode is that the input transistors can operate with their gate behind the supply lines .The common mode input voltage range can include one of the supply rails and hence this can be used for single-supply systems [13-14].

We saw that telescopic cascode Op-Amps suffer from limited output swing. Folded-cascode Op-Amps allow more swing at the output. Although, this topology consumes more power than telescopic topology due to its need for another current source (M3 and M4 act as a current

source). This topology can be implemented either employing PMOS input devices or NMOS input devices.

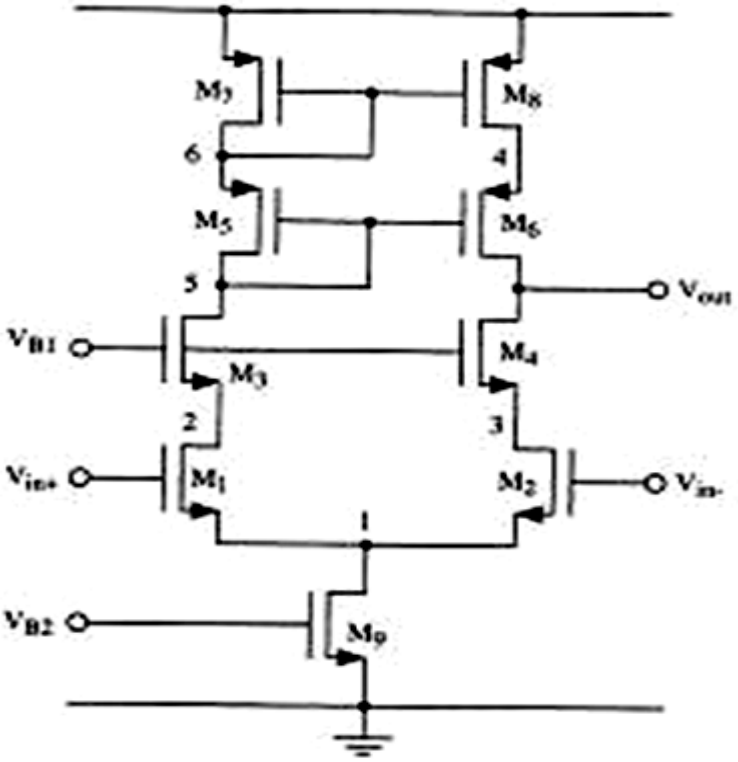

Fig. 2: Telescopic Op-amp

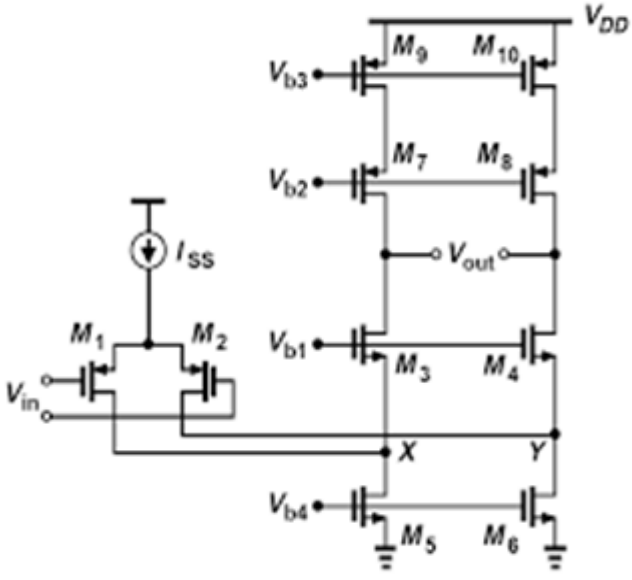

Fig. 3: Folded cascode Op-amp

3. METHODOLOGY

This section discusses the design of three op-amp topologies. Firstly the design of a two stage op-amp will be discussed. This is followed by the description of telescopic op-amp and folded cascode op-amp. In this work the circuit is designed using 0.18µm CMOS technology, with process parameters as shown in Table I., The code run in Matlab and simulations were performed using the Cadence Virtuoso Analog design environment [8-15].

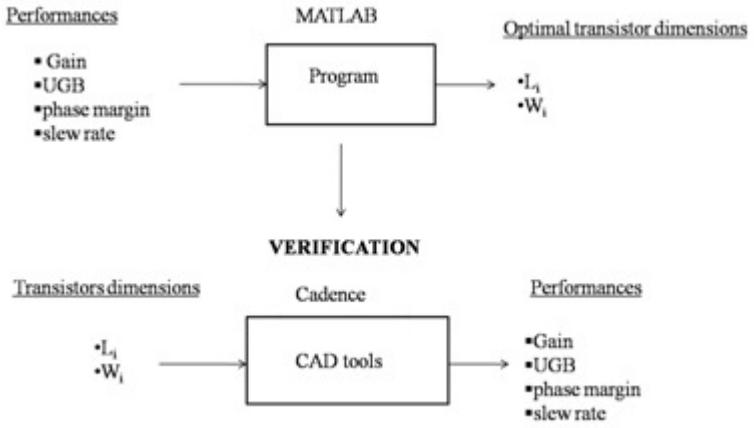

Fig. 4: Op-amp design flow

Table I: Process parameters for Op-amp topologies design

Parameter	Value
Vdd & Vss	±1.8V
kn^1	345 uA/V^2
kp^1	55 uA/V^2
Vt_n	0.48V
Vt_p	0.43V

3.1 Design Equations to be used

Open-Loop Dc Gain: The open –loop voltage gain is given by

$$A_V = \frac{g_{m1}}{g_{ds2} + g_{ds4}} . \frac{g_{m6}}{g_{ds7} + g_{ds6}}$$

Unity-Gain Bandwidth: The Unity gain bandwidth is given by the expression

$$GBW = \frac{g_{m1}}{C_c}$$

Where C_c is compensation capacitor

Phase Margin: The phase margin is given by the equation

$$PM = \pm 180 - \tan^{-1}(\frac{GBW}{P1}) - \tan^{-1}(\frac{GBW}{P2}) - \tan^{-1}(\frac{GBW}{z})$$

Slew Rate: The slew rate is given by

$$SR = \frac{I_5}{C_c}$$

Power Consumption: The power consumption is given by

$$P = (V_{DD} - V_{ss})(I_5 + 2I_7)$$

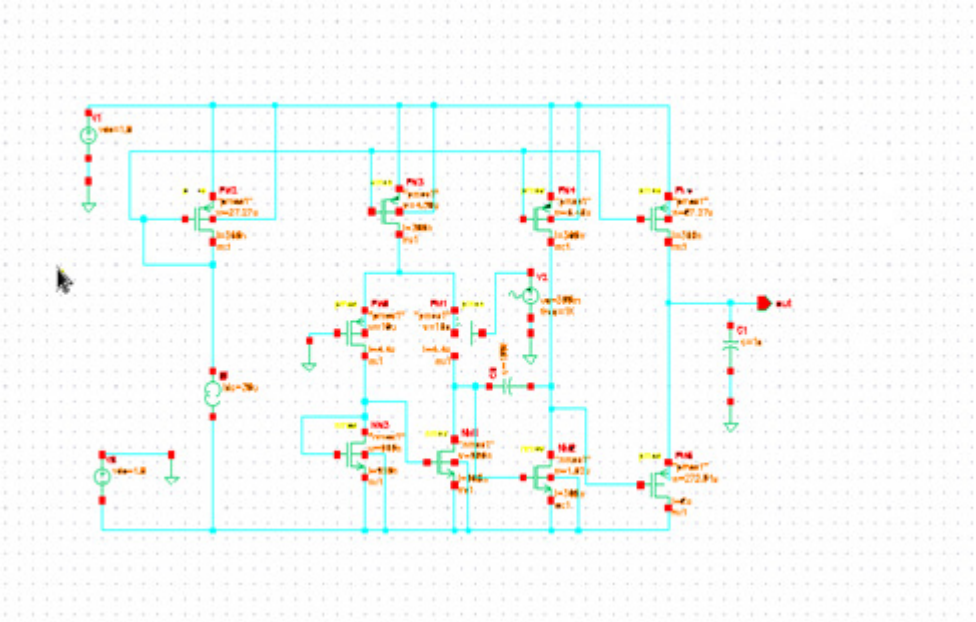

Fig. 5: Op-amp topologies:Two stage

Table II: Simulation results of each transistor dimension for the two stage amp

Transistor	W/L
M1	0.74u/0.18u
M2	0.74u/0.18u
M3	1u/0.18u
M4	1u/0.18u
M5	2.3u/0.18u
M6	0.59u/0.18u
M7	3.27u/0.18u
M8	24.6u/0.18u
M9	13.88u/0.18u
M10	13.88u/0.18u

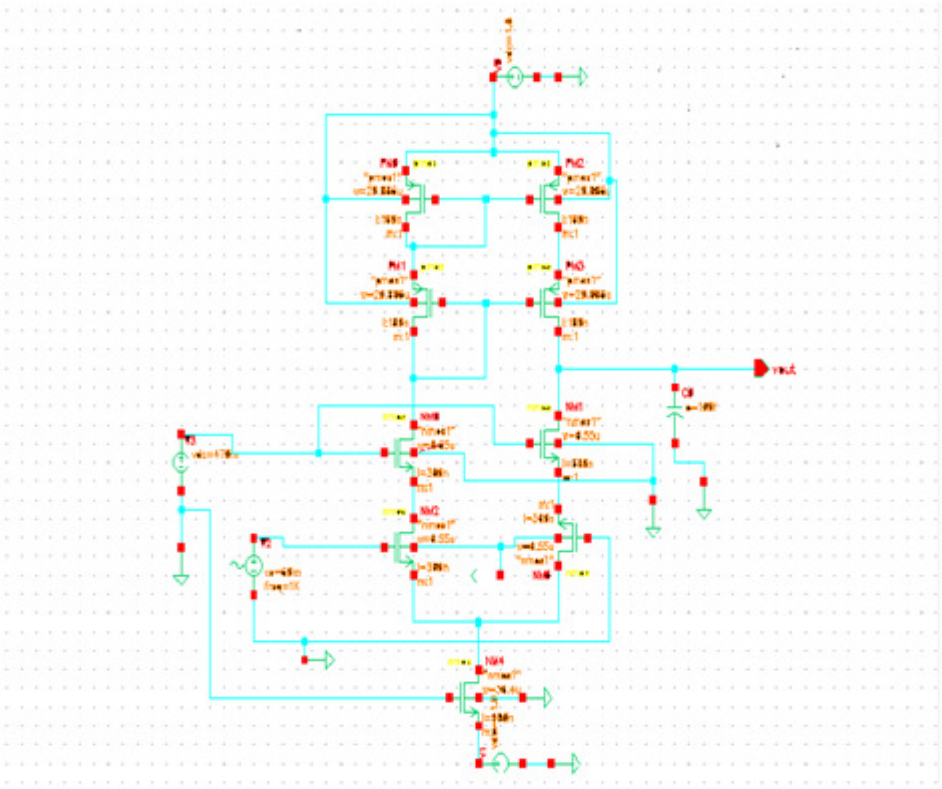

Fig. 6: Op-amp topologies:Telescopic

Table III: Simulation results of each transistor dimension for the telescopic amp

Transistor	W/L
M1	18.19u/0.18u
M2	18.19u/0.18u
M3	18.19u/0.18u
M4	18.19u/0.18u
M5	115.52u/0.18u
M6	115.52u/0.18u
M7	115.52u/0.18u
M8	115.52u/0.18u
M9	36.39u/0.18u

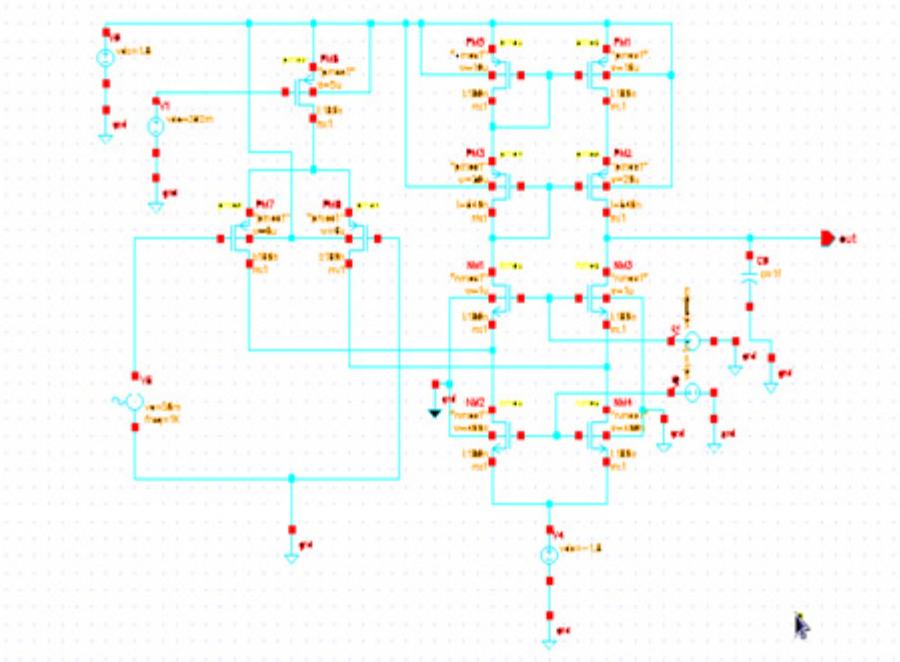

Fig. 7: Op-amp topologies:Folded cascade

Table IV: Simulation results of each transistor dimension for the Folded cascade

Transistor	W/L
M1	5u/0.18u
M2	10u/0.18u
M3	20u/0.18u
M4	1u/0.18u
M5	10u/0.18u
M6	20u/0.18u
M7	1u/0.18u
M8	6u/0.18u
M9	0.4u/0.18u
M10	6u/0.18u
M11	0.4u/0.18u

4. RESULTS AND DISCUSSION

This section examine an automated tool box which calculates the W/L values of the transistors of circuits which includes two-stage op-amp, telescopic amplifier and folded cascode amplifier. Thus decreasing the time spend on designing the circuit, as the designer gets the W/L values of the transistors automatically by just running the Matlab code of the above circuits.

The tool box contains the Matlab codes for each of the three mentioned circuits. The Matlab code contains the design procedure steps which gives the W/L values of the circuit.

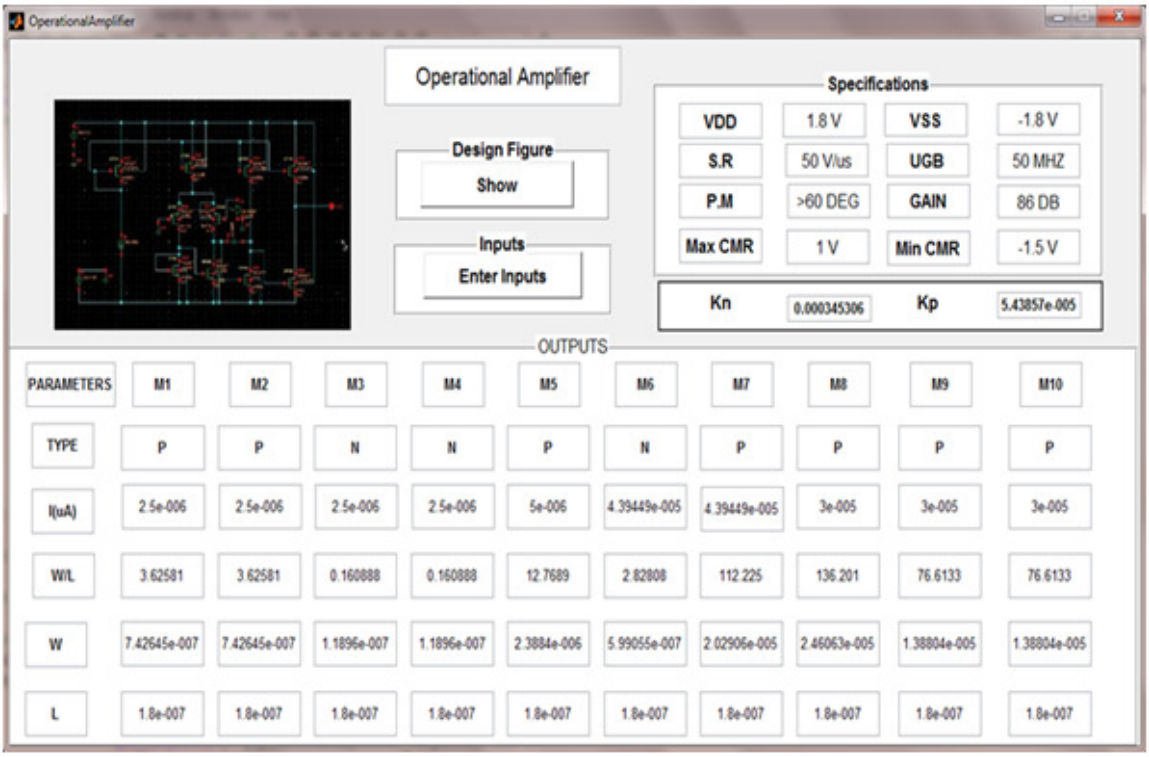

Fig. 8: Two stage op-amp output window with W/L values

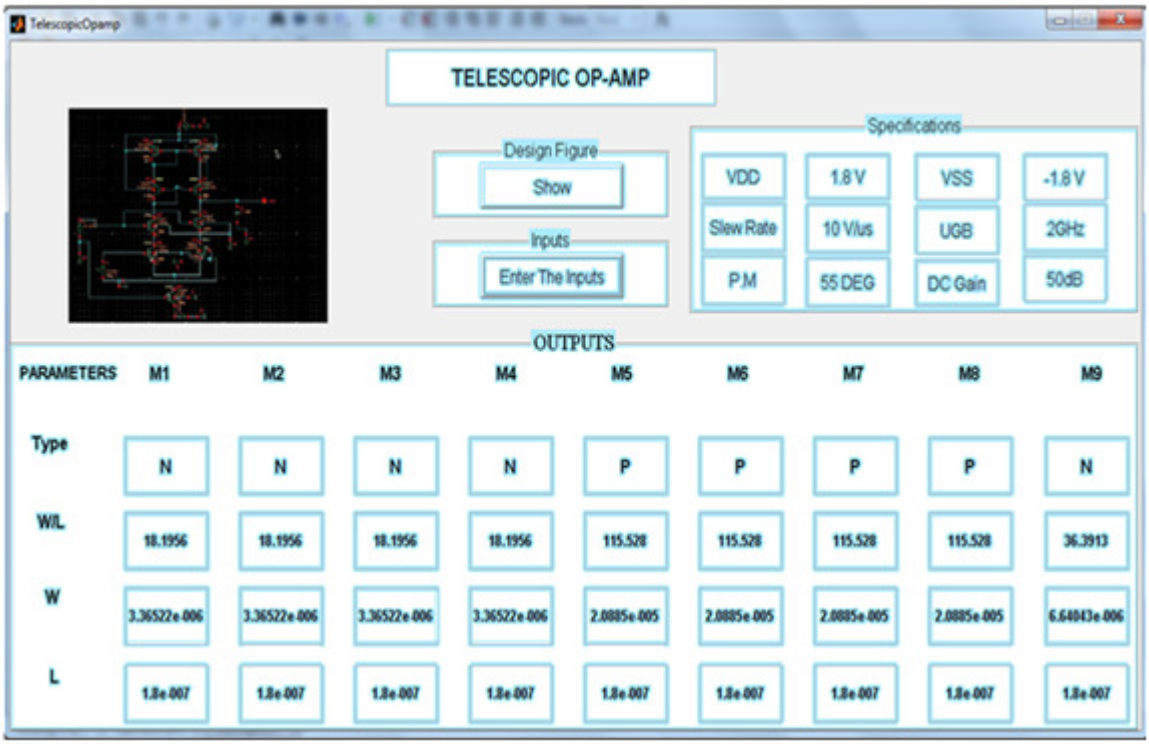

Fig. 9: Telescopic op-amp output window with W/L values

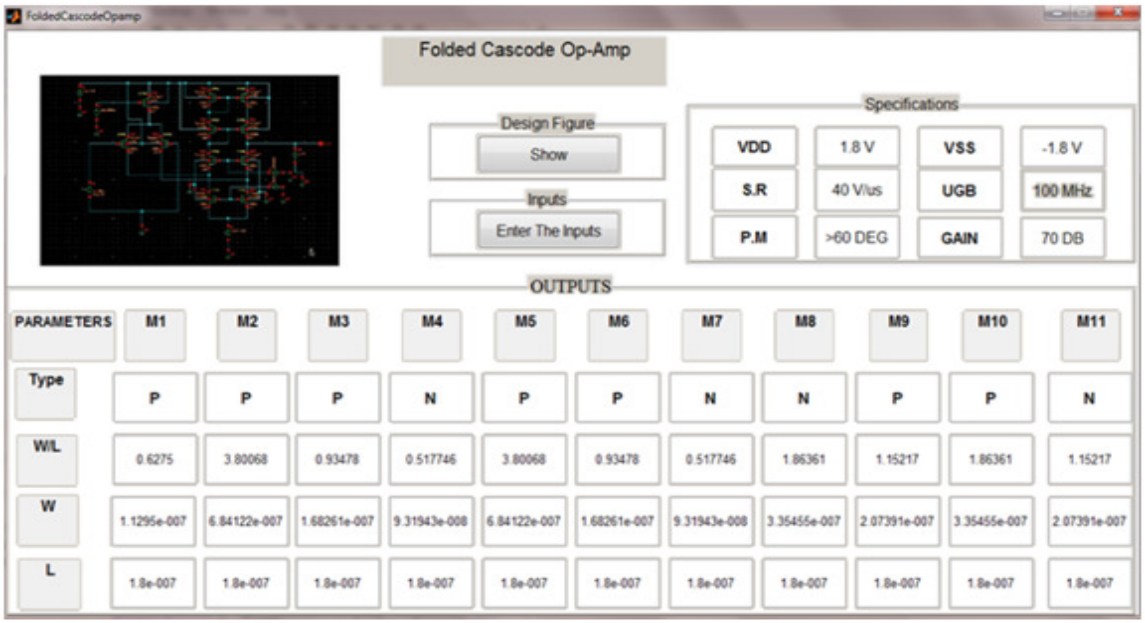

Fig. 10: Folded cascode op-amp output window with W/L values

The simulation results for the two stage op-amp gain are shown in Fig. 11. From the figure, the circuit is able to achieve a maximum gain of 85.14dB with a unity gain frequency of 66.5MHz. Fig. 12 shows the frequency response for the telescopic amplifier. From the figure, the circuit is able to obtain 52.79dB with a unity gain frequency of 2.10GHz. The folded cascode op-amp performance is depicted in Fig. 13.Based on the simulation results a maximum gain of 70.44dB is achieved for the folded cascode with a unity gain frequency of 72.03MHz.

Table V shows the comparison between specifications mentioned in Matlab and simulated results are nearly matched for various op-amp topologies.

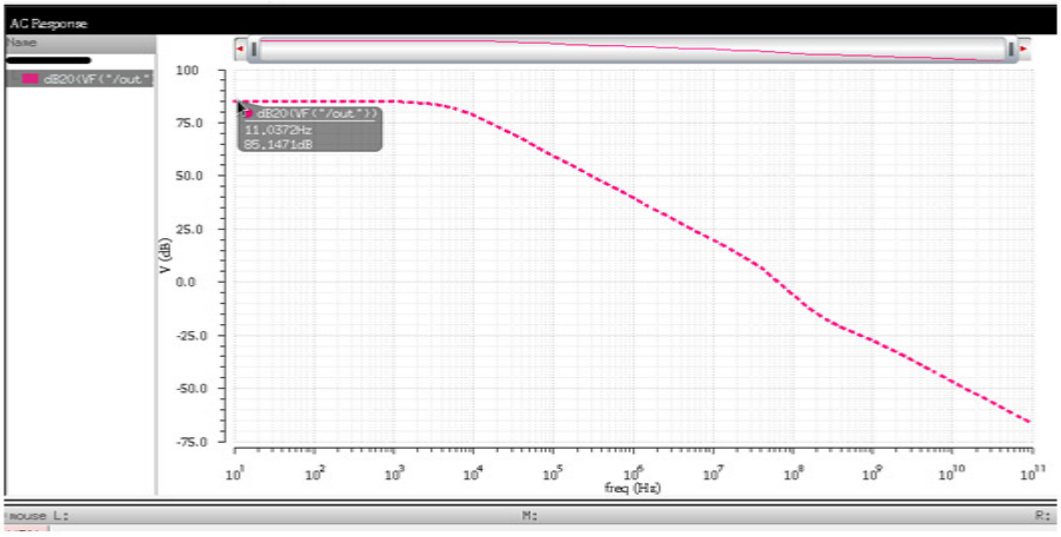

Fig.11: Results of AC analysis for the Two stage Op-amp

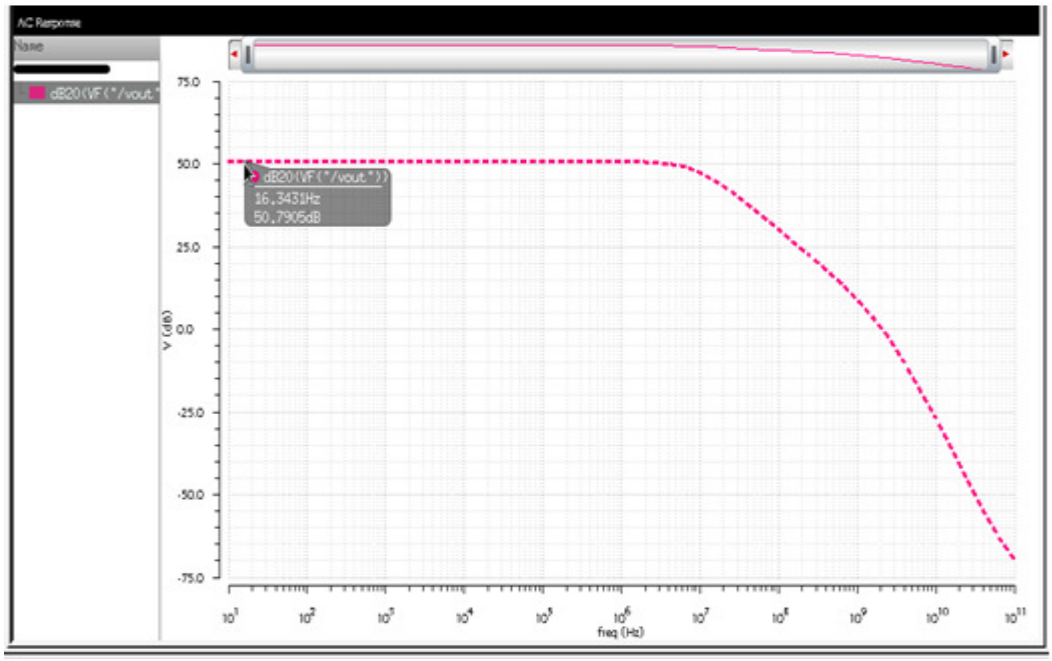

Fig.12: Results of AC analysis for the Telescopic Op-amp

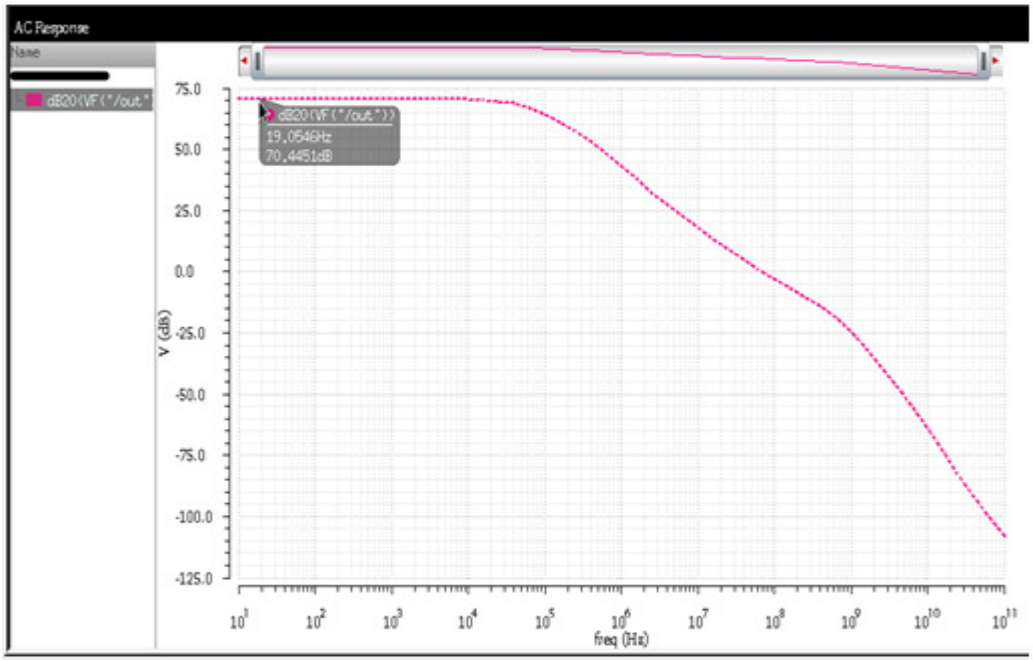

Fig. 13: Results of AC analysis for the folded cascode Op-amp

Table V: Comparision of different parameters of various Op-amp topologies

OPAMP TOLOPOGY	Two-stage Op-amp		Telescopic Op-amp		Folded cascode Op-amp	
Parameter	Specifications entered in MATLAB	Simulated value from Cadence	Specifications entered in MATLAB	Simulated value from Cadence	Specifications entered in MATLAB	Simulated value from Cadence
Gain	86dB	85.15dB	50dB	50.79dB	70dB	70.44dB
Unity gain (in Hz)	50MHz	66.5MHz	2GHz	2.10GHz	100MHz	72.03MHz
Phase margin (in deg)	60	54	55	50	60	87
Slew rate	50v/us	48v/us	10v/us	9v/us	40v/us	36v/us
Power consumption	NA	186.46uA	NA	11.89uA	NA	81.03uA

5. CONCLUSION

In This paper ,a Matlab based tool box has been developed for analog integrated circuits design.the Mat lab based tool box and equation-based optimization are combined to produce an accurate tool in order to determine the device sizes in an analog circuits. a matlab based approach is proposed to optimize the various op-amp topologies.

The results prove the effectiveness of the approach in the analog design where the design space is too complicated to be done with the classical methods within a short time. It can be concluded that the proposed mat lab based tool box approach is efficient and gives promising results for analog integrated circuit design, for the next phase of this work will be optimization of various analog circuits and mixed signal systems.

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