DESIGN AND PERFORMANCE ANALYSIS OF VARIOUS ADDERS AND MULTIPLIERS USING GDI TECHNIQUE

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ABSTRACT

With the active development of portable electronic devices, the need for low power dissipation, high speed and compact implementation, give rise to several research intentions. There are several design techniques used for the circuit configuration in VLSI systems but there are very few design techniques that gives the required extensibility. This paper describes the implementation of various adders and multipliers. The design approach proposed in the article is based on the GDI (Gate Diffusion Input) technique. The paper also includes a comparative analysis of this low power method over CMOS design style with respect to power consumption, area complexity and delay. In this paper, a new GDI based cell designs are projected and are found to be efficient in terms of power consumption and area in comparison with existing CMOS based cell functionality. Power and delay has been calculated using Cadence Virtuoso tool at 45nm CMOS technology. The results obtained show better power and delay performance of the proposed designs at 1.3V supply voltage.

KEYWORDS

CMOS, GDI, Adders, Low Power, Digital Design

1. INTRODUCTION

In today's period, the demands of portable electronic devices are increasing day by day. But issues like power consumption, size and capability still exist and need to be overcome in the existing designs. Power consumption is the most important issue in VLSI design. As per the recent trends in technology, the number of transistors is continuously increasing on a chip that increases the complexity and power consumption of a chip. The increased power consumption leads to increase in the temperature of the chips, which affects the circuit performance. Thus, it is very vital to deal with these issues. Adders and multipliers are well known to be the most basic and fundamental unit in each and every digital circuit used for performing vital computations. The recent trend deals with scaling up to nanometre scale. With the rapidly growing trends in scaling up to nanometer scale, the arithmetic circuits need to be implemented with low power, compact size, and less propagation delay. Therefore, arithmetic cells which consume low-power and provide high performance are of great significance. Thus, any adjustment made in the arithmetic unit would affect the arrangement as a sum total. For designing the arithmetic circuits with low power and high speed [6], it requires the in corporation of techniques at the arithmetic level, architecture level, circuit level and system level. There are several low power design techniques such as dynamic voltage scaling, frequency scaling and clock gating [4] but, there are

DOI : 10.5121/vlsic.2015.6504

very few design techniques that gives the required extensibility with low power consumption and low area.

Recently, a new design approach called GDI (Gate-Diffusion Input) [1] is proposed by Morgenshtein et al. which is used for the design of low power circuits. This method helps in reducing the power consumption, area and propagation delay. To fulfill the increasing demand, we propose different types of adders and multipliers using low power GDI technique that reduces the area and power consumption problem compared to the existing CMOS based designs. In the continuing part of this paper, Section 2 explains the related work. Section 3 briefs the function of GDI technique. Section 4 describes the proposed design of adders and multipliers using GDI method. A comparative analysis between both the techniques is also carried out in this section. In section 5, simulations and results are described. Finally, section 6 presents the conclusion of the work.

2. RELATED WORK

Chia-Hao Hsu et al. has discussed a new design technique known as Gate diffusion input (GDI) for dissimilar types of 10 transistors based full adder. For testing the performance of the proposed adders a whole authentication and analysis have carried out in [3]. In this paper, the proposed designs have some benefits like the extensibility, less transistors count etc. Therefore this can be easily actualized using the CMOS logic. The test results indicate that the proposed 10 transistors full adder is better than the pre-existing designs. Hence, this makes a good alternative choice. Padmanabhanuyuy Balasubramanian et al. has discussed about the digital circuit design with low power modified GDI method [5]. Gate Diffusion Input (GDI) technique for the reduction of power of the digital circuit design has been described in this paper. The eminence of this design method with glance to area complexity, power consumption and delay has also been characterized. In this paper, the logic cells were designed using GDI scheme. These cells are found to be energy efficient in distinguish with the cells based on GDI technique. The importance of these designs was realized by the simulations results observed using CMOS technology. Therefore, in the field of VLSI design we need these kinds of optimized circuits in terms of power, delay and surface area.

Israel A.Wagner et al. has examined the Gate Diffusion Input (GDI) approach for the reduction of power consumption in logic circuit design. The prevalence of this design technique over standard CMOS logic style and PTL (pass transistor logic) with glance to power dissipation, area multiplicity and propagation delay has also described [11]. A new approach of digital circuit design with low power has examined. This approach helps in decreasing the propagation delay, area and power consumption which also maintains the low complexity of the circuits. In this paper, operation illustration with standard CMOS process and pass-transistor logic (PTL) design techniques have been described. The different processes have distinguished in terms of area, number of transistors, propagation delay, and power dissipation. The advantages and disadvantages of Gate diffusion input technique compared to other process has also been examined. Numerous logic circuits have been actualized in different design methods.

M. Mohanapriya et al. has examined the delay, area and power dissipation analysis of adder topographies [2]. This paper presented the appropriate option for the selection of the adder topology related with the parameters like power dissipation, delay and area. This paper has evaluated the operational and performance parameters like area, power dissipation and

propagation delay. In this research work, the functions of adders were analyzed for the optimization of power dissipation, delay and area. These adders have been generally used in several applications such as in digital system, control system and digital signal processing.

3. GATE DIFFUSION INPUT TECHNIQUE

The GDI scheme depends on the implementation of an elementary cell as shown in Figure 1. Principally, this GDI cell looks like a CMOS inverter. However, there are a number of dissimilarities. The GDI cell involves three inputs: 1.) Standard gate input of PMOS and NMOS. 2.) P input to the source/drain of PMOS and 3.) N input to the source/drain of NMOS where bulk of PMOS and NMOS are associated to P or N. It is observed that all of the functional operations are not possible in standard CMOS process but they can be strongly actualized in silicon on insulator (SOI) or CMOS technologies [9] [10].

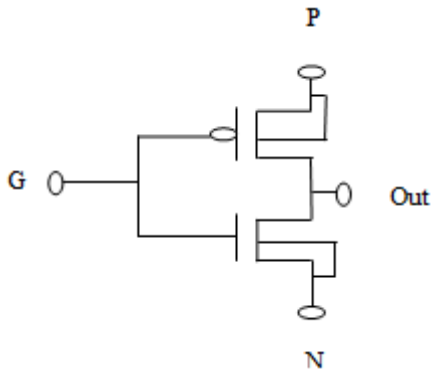

Figure 1. Standard GDI Cell [11]

Table 1.Various Logic Functions [11]

N	P	G	Out	Function
'0'	b	a	a'b	f1
b	'1'	a	a'+b	f2
'1'	b	a	a+b	OR
'b'	'0'	a	ab	AND
'c'	B	a	a'b+ac	MUX
'0'	'1'	a	a'	NOT

Table 1 represents that a small variation in the input line of the elementary GDI cell consistent to different Boolean functions. Generally, these functions are versatile in CMOS as well as in PTL implementations. But these functions are very simple in GDI design method. The GDI method is different from the other design techniques, and it has some valuable characteristics, that allow up gradation in design multiplicity level, power dissipation, and transistor count. Understanding of GDI cell needs a wide functional determination of the elementary cell in several cases and configuration. Firstly we have designed the basic digital gates using GDI technique [5] and then these gates are further used in the implementation of different types of adders and multipliers.

4. PROPOSED ADDERS AND MULTIPLIERS

This section describes the implementation and analysis of various adders and multipliers using GDI technique and CMOS logic scheme. The design of different adders using new low power technique has been proposed and finally optimized adder is selected on the basis of performance and the selected adder is further used in the design of multiplier. Firstly 1 bit full adder [3] is designed using GDI method. This adder is further used to analyze the other complex adders for their better performance. The adders that are implemented using GDI method [2] are ripple carry adder, carry look ahead adder and carry save adder.

4.1 Ripple Carry Adder

The Ripple Carry Adder (RCA) is the simplest adder which is very easy to implement. The basic unit of RCA is a full adder. This can be enlarged to any number by connecting the previous stage carry out of 1 bit full adder to the carry input of the next 1 bit full adder. Ripple carry adder takes in two n-bit inputs where n is a positive integer and it yields (n+1) output bits as n bit sum and a 1 bit carry out. The sum bit needs both input bits and carry input before it can be analyzed. The implementation of Ripple Carry Adder using GDI full adder is shown in figure 2.

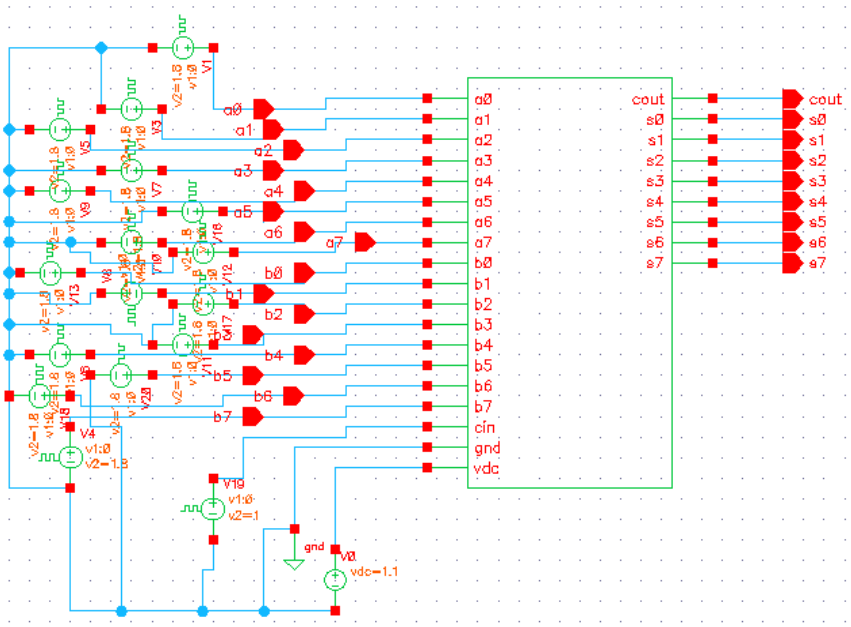

Figure 2. Schematic of GDI based RCA adder

This adder is realized using full adder with low power GDI [8] technique. In this adder, the two 4 bit adders are connected in cascaded form which are designed with the Gate Diffusion Input method.

4.2 Carry Look Ahead Adder

The CLA (Carry Look Ahead) adder calculates the carry signal in advance and this minimizes the propagation delay. This adder possesses very good operation speed. The CLA adder posses carry propagate signal and carry generate a signal which are calculated through the use of the partial full adders. Figure 3 shows the schematic for a Carry Look- Ahead Adder.

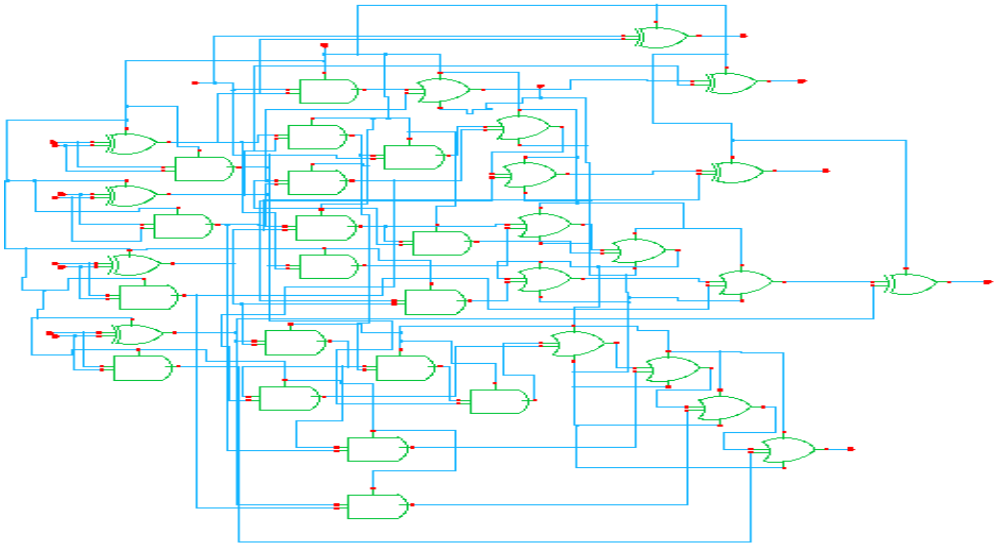

Figure 3. Schematic of GDI based CLA Adder

4.3 Carry Save Adder

Carry save adder implements the synchronous addition of the numerous operands. This is the fundamental need of the multiplication. It is a kind of digital adder which is used in various computer architectures for the computation of the summation of n bit numbers. The schematic of GDI based Carry save adder (CSA) is shown in figure 4.

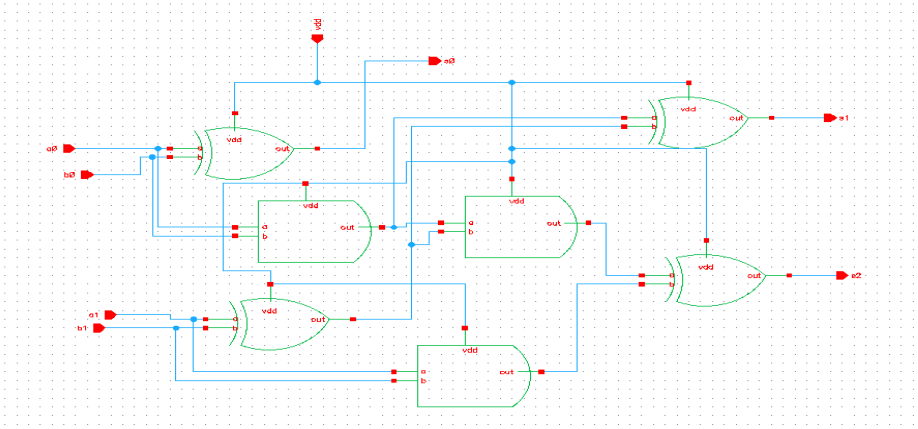

Figure 4. Schematic of GDI based CSA adder

4.3 Multiplier

Multiplication can also be determined as a follow-up of replicated additions. Multiplication is an encapsulated logic of adding a number or integer to itself, for a described number of times. We apply the GDI technique for the implementation of the multiplier that reduces its power and area to greater extent [7]. The schematic of conventional GDI based multiplier is shown in figure 5. To implement the multiplier function, we use the GDI based full adder and GDI based AND gates. We apply the carry look ahead adder (CLA) for the implementation of the modified multiplier. The schematic of modified multiplier which is designed by using GDI based carry look ahead adder is shown in figure 6. GDI based multipliers have minimum power, delay and PDP as compared to CMOS based multipliers. The comparison has been shown in Table 4.

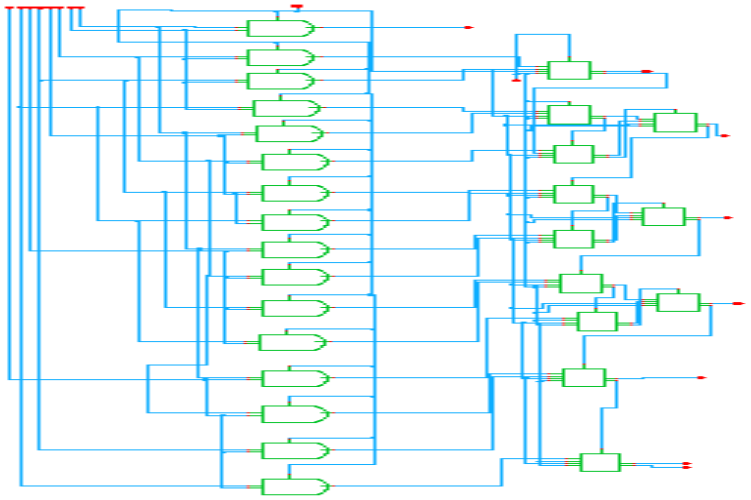

Figure 5. Schematic of conventional GDI based multiplier

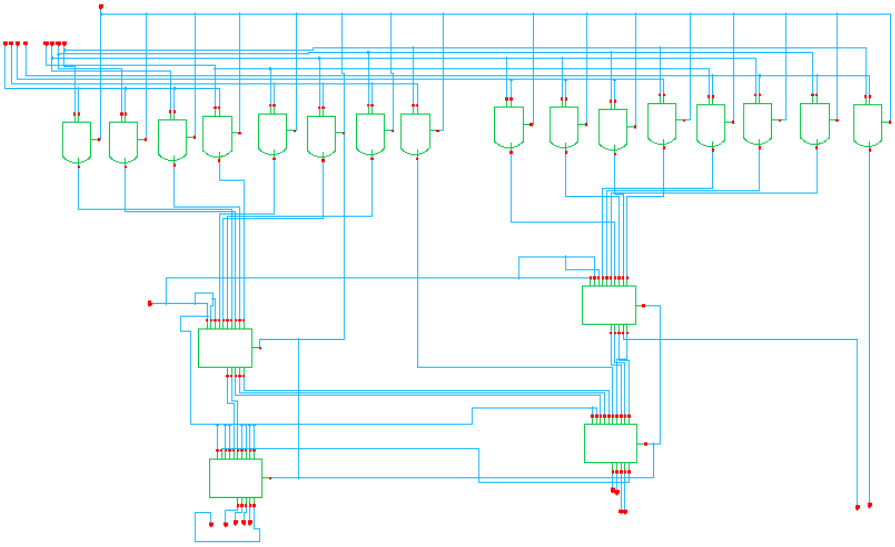

Figure 6. Schematic of GDI based multiplier using CLA

5. SIMULATION RESULTS

In this section, the operational functions of the proposed designs are examined. The analysis is carried out at 45nm technology using Cadence Virtuoso tool. The performance of all the proposed circuit designs is determined in regard of delay, transistors count and power consumption at a biasing voltage ranging from 1 volt to 1.5volts. The comparison of average power, transistors count and delay between the GDI and CMOS based gates, adders and multipliers are shown in Table 2, 3 and 4. It can be seen from the tables that the performance of GDI based circuits are much better than the CMOS based cells in terms of power consumption and reduced area.

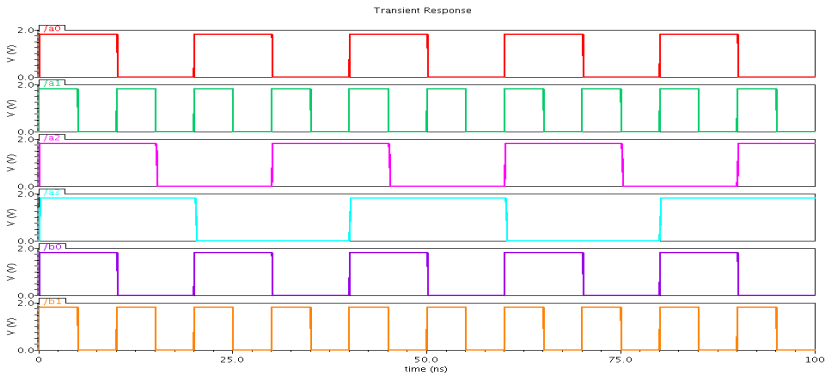

Figure 7. Input waveforms of GDI based CLA Adder.

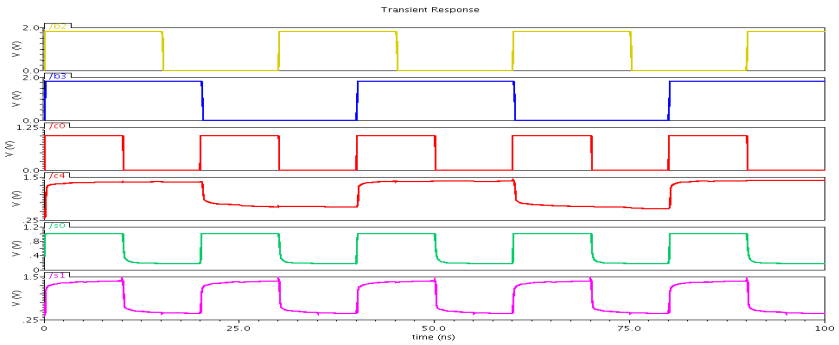

Figure 8. Simulation waveforms of GDI based CLA Adder

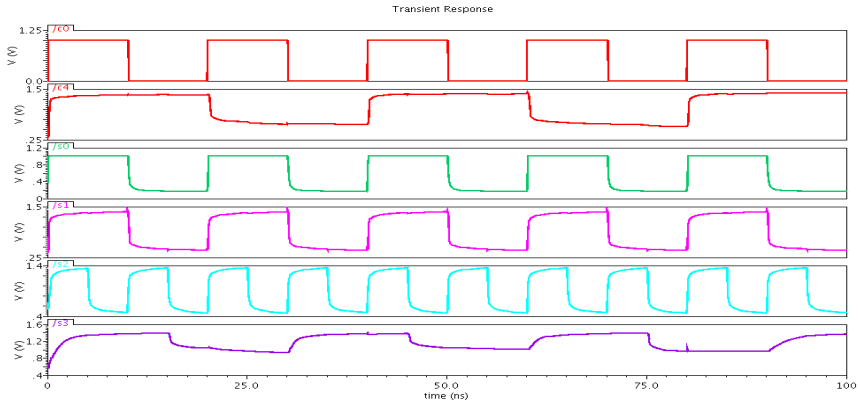

Figure 9. Output waveforms of GDI based CLA Adder

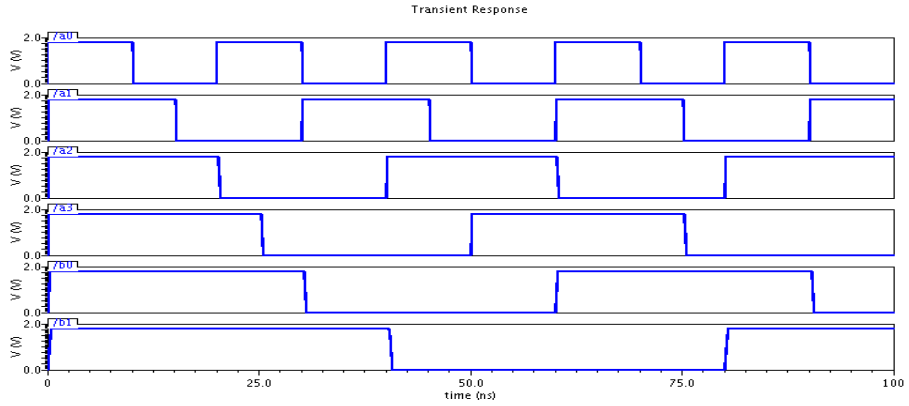

Figure 10. Input waveforms of GDI based multiplier using CLA

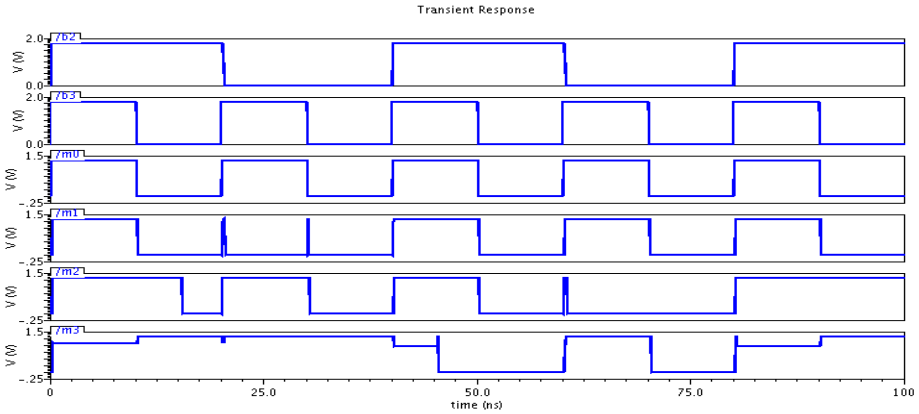

Figure 11. Simulation waveforms of GDI based multiplier using CLA

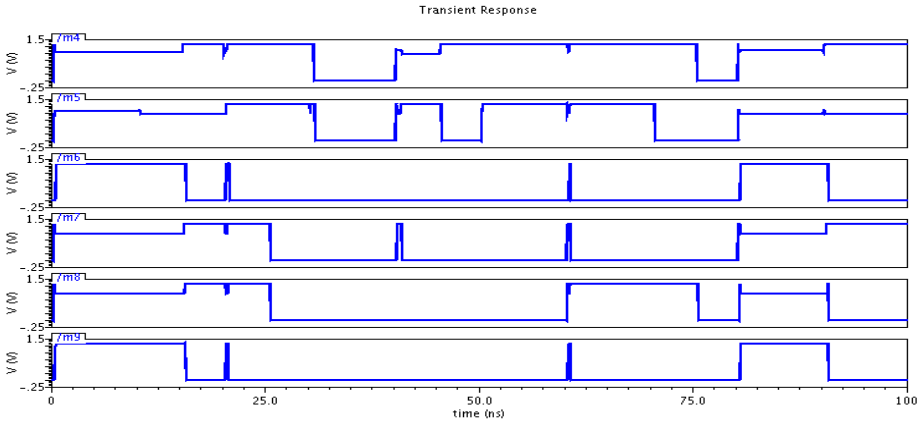

Figure 12. Output waveforms of GDI based multiplier using CLA

The charts illustrated in Figures 13, 14, 15 and 16 describe a comparison of the results obtained for the circuit designs examined in this work. Figure 13 shows the power delay product comparison profile of basic logic gates for the two different implementation styles. Figure 14 shows the PDP obtained for the different adders using two design techniques whereas figure 15

illustrate the PDP (Power Delay Product) obtained for the multipliers using CMOS and GDI technique. Figure 16 shows the comparison of the transistor count of different adders for CMOS design style and GDI design technique.

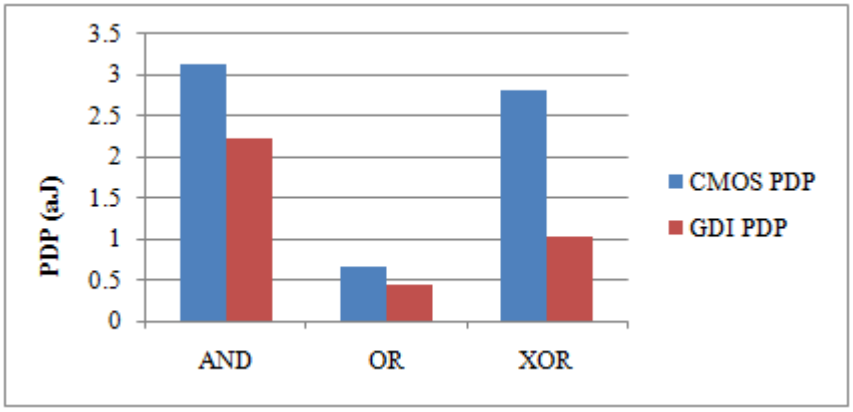

Figure 13. PDP graph of logic Gates

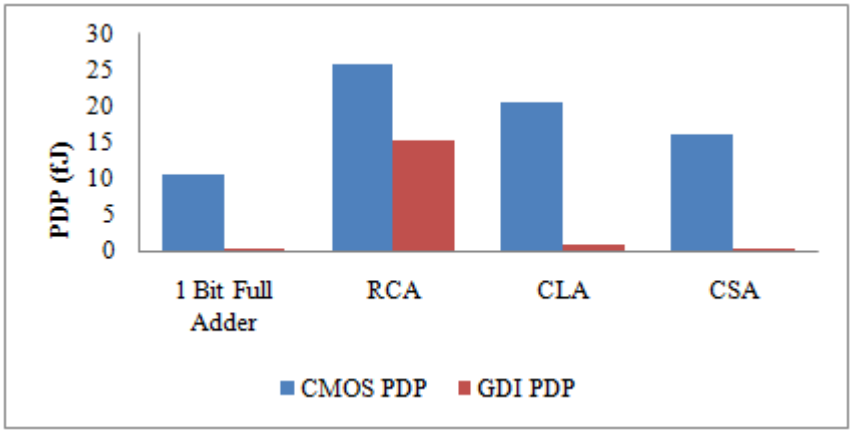

Figure 14. PDP graph of Adders

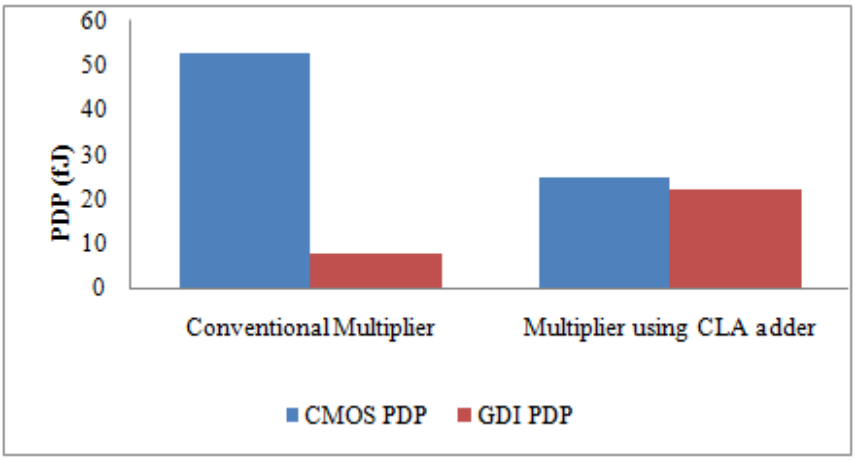

Figure 15. PDP graph of Multipliers

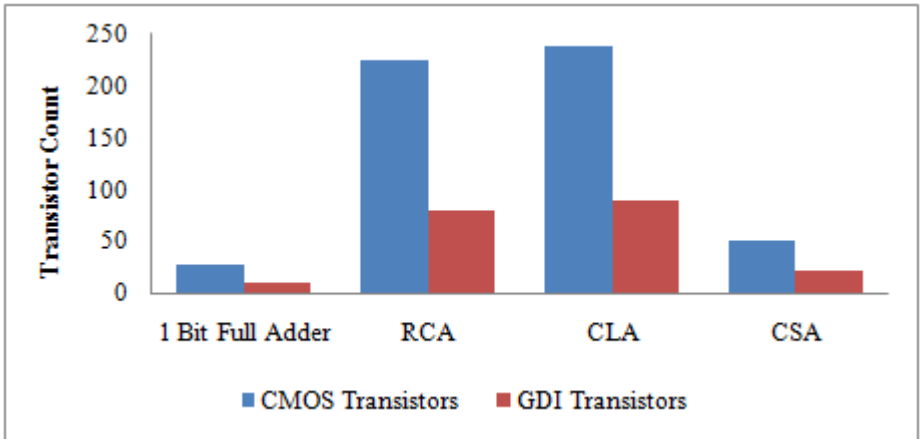

Figure 16. Transistor graph of Adders

Table 2. Performance comparison of CMOS and GDI based Gates

	CMOS				GDI			
Digital Gates	Power (nw)	Delay (ns)	PDP (aJ)	No. of Transistors	Power (nw)	Delay (ns)	PDP (aJ)	No. of Transistors
AND	16.98	0.184	3.1243	6	2.742	0.807	2.2127	2
OR	10	0.065	0.65	6	1.35	0.335	0.4522	2
XOR	21.36	0.132	2.8195	12	4.6	0.224	1.0304	4

Table 3. Performance comparison of CMOS and GDI based Adders

	CMOS				GDI			
Adders	Power (µw)	Delay (ps)	PDP (fJ)	No. of Transistors	Power (µw)	Delay (ps)	PDP (fJ)	No. of Transistors
1 Bit Full Adder	74.99	141.1	10.5810	28	0.0127	194.6	0.002473	10
RCA	144.5	178.2	25.7499	224	2.219	685.8	15.2179	80
CLA	286.5	71.61	20.5162	238	5.293	161.2	0.85532	90
CSA	1.322	1211	16.0094	50	0.4587	112.3	0.05151	22

Table 4. Performance comparison of CMOS and GDI based Multipliers

	CMOS			GDI		
Multipliers	Power (µw)	Delay (ps)	PDP (fJ)	Power (µw)	Delay (ps)	PDP (fJ)
Conventional multiplier	293.9	178.9	52.5787	29.02	267.8	7.7715
Multiplier using CLA adder	267.1	93.42	24.9524	203.0	110.0	22.330

6. CONCLUSION

This paper figure out the advantages of GDI technique over CMOS logic style, as the scaling of devices is regularly increasing. In this paper, we have examined the various adders and multipliers functionality using GDI method Cadence ambiance. Based on transistor level simulations, after applying GDI technique the power reduced in logic gates design, adders and multipliers is 83%, 65.35% and 23.9% respectively. The results of GDI and CMOS based circuits designs are compared in Table 2, 3 and 4. It is found that the circuits using GDI technique are better optimized then the circuits using CMOS logic scheme. Therefore, the proposed designs can be convenient for the use in low power and high speed applications and they become the more suitable substitutes.

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