A NEW TRANSISTOR SIZING APPROACH FOR DIGITAL INTEGRATED CIRCUITS USING FIREFLY ALGORITHM

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ABSTRACT

Due to the fact that, the power consumption and speed of a VLSI circuit are dependent on the transistor sizes, efficient transistor sizing is a new challenge for VLSI circuit designers. However, evolutionary computation can be successfully used for complex VLSI transistor sizing which reduces the time to market and enables the designer to find the optimized solutions for a non-linear and complex circuit design process. In this paper, a new digital integrated circuit design approach is proposed based on the firefly artificial intelligence optimization algorithm. In order to justify the effectiveness of the proposed algorithm in the design of VLSI circuits, an inverter (NOT gate) is designed and optimized by the proposed algorithm. As the simulation results show, the inverter circuit has a very good performance for power and delay parameters.

KEYWORDS

VLSI, firefly algorithm, transistor sizing, power, delay

1. INTRODUCTION

Due to the current rapid advances in the field of portable electronic systems such as: mobile phones, laptop and tablets, the demand for low-power and battery-powered electronic devices is increasing. However, the battery technology did not develop with the rate of microelectronic technology; so, it is required to design low-power electronic circuits and systems. Although, reducing the clock frequency of the system leads to a reduced power value, but, it also reduces the computation speed which is one of the major challenges in the design of integrated circuits. Furthermore, reducing the supply voltage causes a reduction in speed value [1]. So, the main performance parameters such as: delay, power and chip area are in a trade-off with each other. So, choosing a proper value for transistor dimensions (W, L) is the major step in the field of integrated circuit design [2].

However, due to the complex design process of sub-micron integrated circuits, conventional design approaches based on trial and error require a long design time, so, automatic design

DOI : 10.5121/vlsic.2015.6601

algorithms which use optimization algorithms to find the best solutions for design variables (transistor dimensions) are very demanding. However, the optimization constraints should prevent the blind search, while, choosing the transistor dimensions should satisfy the feasibility and fabrication considerations [3]. Furthermore, non-linearity issues are other major problem in optimization based design algorithms [4], which can be solved by meta-heuristic algorithms that try to simulate the social behaviour [5, 6]. In the meta-heuristic approaches the searchable area is considered around the best candidates to solve the design problem. However, a meta-heuristic optimization algorithm called as firefly optimization algorithm is introduced by Yang [7]. The firefly optimization algorithm operates based on flashing characteristics of biological fireflies and has been used more successfully than conventional optimization approaches such as: genetic algorithm (GA), PSO [8, 9].

However, the firefly algorithm is successfully used in applications such as: wireless network design [10], dynamic pricing [11] and mobile agents [12]. As it is discussed in the literature, optimization algorithms such as: Genetic algorithm [13], PSO [3, 14], are successfully used in the design of integrated circuits. As it is discussed in [13], GA is used to optimize the propagation delay of a full adder circuit by selecting optimized values for transistor dimensions. Also, the PSO algorithm is successfully used to optimize the delay of an inverter circuit [3, 14]. However, in both approaches the performance measure of the circuit is formulated as a fitness function in MATLAB and the theoretical values obtained from MATLAB are compared with the circuit simulation results obtained from HSPICE which is a very complex and time consuming task and may face convergence problems especially in sub-micron devices. But, the main idea in this paper is to use directly the HSPICE simulation results in a loop of optimization in MATLAB, where, the firefly optimization algorithm evaluates the fitness value and checks for the termination condition of design algorithm by considering the design problem constraints which leads to an improved accuracy and design time.

This paper is organized as follows: section 2, introduces the firefly optimization algorithm. In section 3, the power and delay equations are presented. In section 4, the proposed design algorithm is discussed in details and the simulation results are presented in section 5. Finally, the conclusions are presented in section 6.

2. THE FIREFLY OPTIMIZATION ALGORITHM

To clarify the performance and operation of the optimization algorithm used in this paper, first we study the behaviour and operation of the firefly optimization algorithm.

The fireflies attract mating partners and potential prey by flashing the light from themselves. The rate, rhythm and the flashing reflection time causes to absorb the fireflies together. Furthermore, different species of fireflies detect each other by imitating optical waves. Generally, fireflies have the following specifications [15]:

- Relaxing from the gender of fireflies, they absorb together.
- Attractiveness is proportional to their brightness, thus, for any two flashing fireflies, the less brighter one will move towards the brighter one. The attractiveness is proportional to the brightness and they both decrease as their distance increases. If there is no brighter one than a particular firefly, it will move randomly;

- The brightness of a firefly is affected or determined by the landscape of the objective function.

The main characteristic of fireflies is the light intensity which is radiated from them and the attraction of each firefly is evaluated using a fitness function in which the fitness value is the value of brightness of each firefly [15].

However, in the simplest form, the light intensity I(r) varies according to the inverse square law:

$$I(r) = \frac{I_S}{r^2} \tag{1}$$

Where, I_s is the intensity at the source. For a given medium with a fixed light absorption coefficient γ, the light intensity I varies with the distance r as follows:

$$I(r) = I_0 \times e^{-\gamma r^2} \tag{2}$$

As it is discussed above, the attractiveness of each firefly is proportional to the light intensity, so, the value of each firefly's attractiveness (β) is obtained as follows:

$$\beta = \beta_0 \times e^{-\gamma r^2} \tag{3}$$

The two dimensional (2D) distance between the two fireflies is calculated based on the eq.(4) and the movement value for i_{th} firefly to the j_{th} firefly is obtained from eq.(5):

$$r_{ij} = \sqrt{\left(x_i - x_j\right)^2 + \left(y_i - y_j\right)^2} \tag{4}$$

$$x_i = x_i + \beta_0 \times e^{-\gamma r i j^2}\left(x_j - x_i\right) + a\varepsilon_i \tag{5}$$

In eq.(5), x, is the initial and final position for i_{th} firefly, while, β part in eq.(5) is the attractiveness of each firefly. Furthermore, the parameter ε is used when no firefly is detected. So, as it is obvious in the above equation, the next position of each firefly is defined based on the attractiveness value of the target's firefly, while, for the cases that no target's firefly exists, the firefly moves randomly [16].

However, the β_0 parameter is usually considered as 1, due to the fact that, the attractiveness value has the highest value at the origin point because each firefly has the highest light intensity (attractiveness value) at it's location, while, the attractiveness value reduces when the distance increases from the origin point [9].

As it is obvious in eq.(5), if β_0=0, then there is no more attractive firefly in the region and the firefly moves randomly. If, $\gamma \to 0$, then, $\beta=\beta_0$ which means that there is no attenuation in light intensity and the firefly's emitted light is detectable everywhere [17]. Also, when $\gamma \to \infty$, all the emitted light is absorbed which causes that the firefly moves randomly again. In theoretical point of view, the γ value may vary between 0 to ∞, while, in practical conditions the γ parameter varies between 0.1 to 10. The semi-code of the firefly algorithm is as follows:

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Objective function f(x), x = (x1, ...,Xd)T
Generate initial population of fireflies Xi (i = 1, 2, ..,n)
Light intensity Ii at xi is determined by f(xi)
Define light absorption coefficient γ
while (t <MaxGeneration)
    for i = 1 : n all n fireflies
        for j = 1 : n all n fireflies (inner loop)
            if (Ii < Ij), Move firefly i towards j; end if
            Vary attractiveness with distance r via exp[−γr]
            Evaluate new solutions and update light intensity
        end for j
    end for i
    Rank the fireflies and find the current global best g *
end while
Postprocess results and visualization
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Fig 1.The semi-code of firefly algorithm [9]

3. POWER-DELAY EQUATIONS AND DISCUSSION

As it is discussed above, there is an inherent conflict between power and delay parameters, but, the delay parameter is proportional to the values of circuit's on-resistance (R_{on}) and capacitance (C) [2]. Furthermore, the circuit's resistance is proportional to the inverse of transistor width (W), so, the larger W leads to a smaller resistance as well as delay values.

Moreover, the power consumption is proportional to the value of circuit's capacitance, so, the larger capacitor causes the higher power consumption value. On the other hand, the capacitance value of an integrated circuit is proportional to the value of the circuit area (W, L), so, increasing the transistor width (W) leads to a higher circuit's capacitance and power consumption.

Giving the above facts, if the value of W is chosen based on a reasonable trade-off between the power and delay parameters, it is possible to design an optimized low-power and high-speed digital integrated circuit.

However, the power-delay product (PDP) parameter, which considers both power and speed of the circuit is used as an effective performance parameter to show the inherent trade-off between power and speed performances of a digital integrated circuit. As a result, minimizing the PDP parameter guaranties the optimized values for both the power consumption and speed parameters of the circuit.

However, as it is discussed in [2], the switching behaviour of the inverter can be generalized by examining the parasitic capacitances and resistances associated with the inverter circuit which is modelled in Fig. 2.

Although the model is shown with both switches open, in practice one of the switches is closed, keeping the output connected to VDD or ground. The effective input capacitance of the inverter is [2]:

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2}) = C_{inn} + C_{inp} \quad (6)$$

The effective output capacitance of the inverter is simply:

$$C_{out} = (C_{ox1} + C_{ox2}) = C_{outn} + C_{outp} \tag{7}$$

The intrinsic propagation delays of the inverter are:

$$T_{PLH/PHL} = 0.7 \times R_{p2/n1} \times C_{tot} \tag{8}$$

In which the C_{tot} is the total capacitance seen at the output node which is as follows:

$$C_{tot} = C_{oxp} \times C_{oxn} + \frac{3}{2}(C_{oxp} + C_{oxn}) = \frac{5}{2}(C_{oxp} + C_{oxn}) \tag{9}$$

Where, the C_{OX} is:

$$C_{oxn/oxp} = C_{ox}^{/} + W_{p/n} \tag{10}$$

The propagation delay of the circuit is as follows:

$$\tau_p = \frac{T_{PLH} + T_{PHL}}{2} = 0.7(R_n + R_p)C_{tot} \tag{11}$$

On the other hand, the average power is as follows:

$$P_{avg} = VDD \times I_{avg} = \frac{C_{tot} \times VDD^2}{T} = C_{tot} \times VDD^2 \times f_{clk} \tag{12}$$

So, the power-delay product (PDP) which is considered as the main optimization objective of this paper is as follows:

$$PDP = Pavg \times \tau_p \tag{13}$$

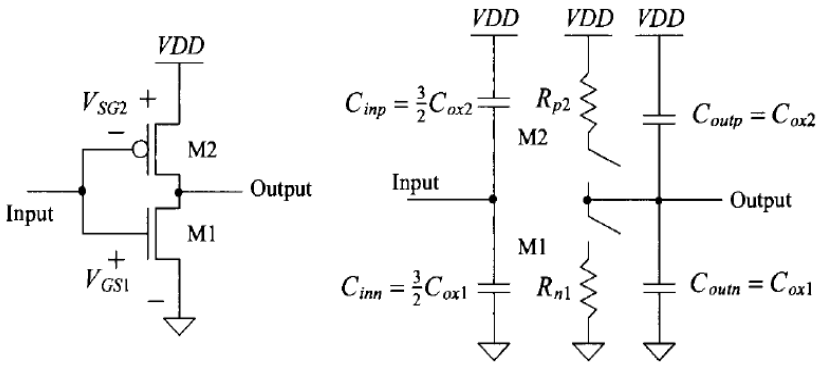

Fig 2. The CMOS inverter switching characteristics using the digital model [2]

4. THE PROPOSED ALGORITHM

As it is mentioned before, the conventional equation-based design method of VLSI circuits, based on manual calculations of transistor sizes, is a very time consuming and complex task which has a large amount of errors between the theoretical results and the results obtained from circuit simulations in HSPICE due to the non-linear and second-order effects which appear in the transistor behaviour. So, the artificial intelligence based design methodologies are successfully used for design and optimization of VLSI circuits [3, 13, 14]. In these methods a fitness function is considered for optimization and the design algorithm tries to minimize the fitness function (power consumption or propagation delay) to find the best solutions for design variables (W, L). However, there is always an error value between the theoretical results which are obtained from design equations and simulation values which are obtained from circuit simulations in HSPICE due to the fact that, theoretical calculations do not consider the higher-order effects which appear in the transistor behaviour, while, circuit simulations consider such effects and use complex transistor models. So, in this paper, as fig. 3 shows, a SPICE-Netlist file is generated for each circuit and the values for design performance measures such as: delay, power, PDP are calculated in HSPICE and the simulation results are transferred to MATLAB to be optimized by the firefly algorithm. In the proposed design algorithm, the firefly optimization algorithm varies the value of W and the main circuit performance parameter which is PDP is evaluated by the circuit simulator HSPICE and the process continues until the termination condition satisfied which is based on the termination of the number generations or achieving a desired value of PDP parameter. Finally, the minimum value of the PDP parameter as well as the corresponding transistor dimensions (W, L) are obtained from the optimization algorithm.

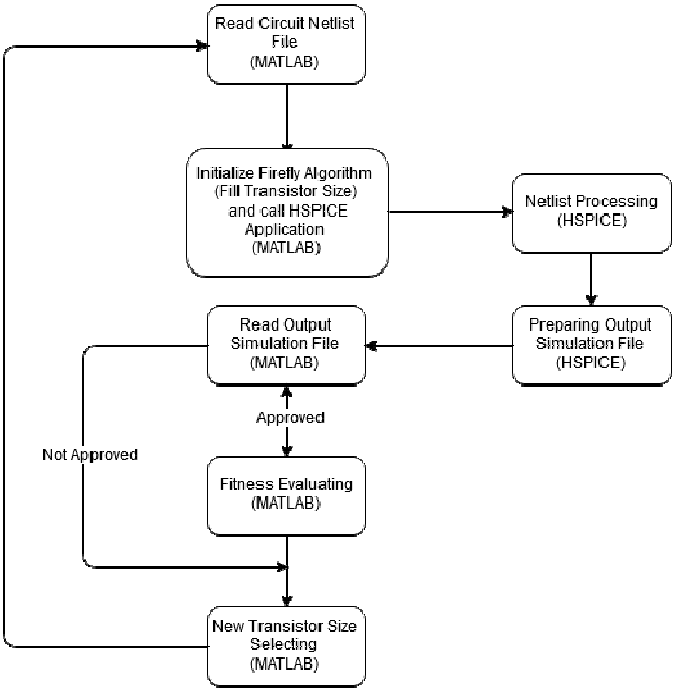

Fig 3. Block diagram of proposed approach

5. SIMULATION RESULTS

The proposed design and optimization algorithm is implemented in MATLAB, while, the circuit simulations are done in HSPICE for a CMOS inverter circuit shown in fig. 2, in 0.25µm technology at 2.5v supply voltage. Furthermore, the number of generations is 100 while, the population size is 50 and the range for selection the main design variable (W) is 0.25µm to 25µm. Moreover, the firefly algorithm is initialized using the parameter values given in table. 1.

Table 1. Variables of firefly algorithm

Variables	Value
(randomness) α	0.5
(absorption) γ	1.0
β	0.2
β_0	1

However, in order to justify the effectiveness of the proposed algorithm over other design methods, the performance of the proposed algorithm is compared with the performance of the [3] and [14] which use particle swarm optimization (PSO) based design and optimization algorithm. Table 2, compares the simulation results which is obtained from simulations of firefly design algorithm and those obtained from PSO design method.

As table 2 shows, T_{phl} and T_{plh} of the proposed algorithm is reduced significantly in comparison with the value obtained from [3], due to the fact that, the value of load capacitor (C_{load}) is 73% smaller than [3]. Also, in order to justify the effectiveness of the proposed algorithm, the T_{phl} of the proposed algorithm is reduced considerable (≈62.7%) and the T_{plh} is reduced 8% in comparison with the value obtained from [14] for the same C_{load} value. According to the comparisons, the proposed algorithm has the best performance over previously reported design methodologies.

Table 2. Simulation Results

	Proposed Algorithm	[3]	[14]
T_{phl}(ps)	40.95	1100	110
T_{plh}(ps)	91.17	1100	100
C_{load}(pf)	0.3	1.12	0.31
V_{DD}(v)	2.5	2.5	2.5
Tech(um)	0.25	0.25	0.25

Finally, the MATLAB simulation result of the fitness function (PDP) is shown in fig. 4, which shows the evolution and optimization of PDP parameter versus the number of generations.

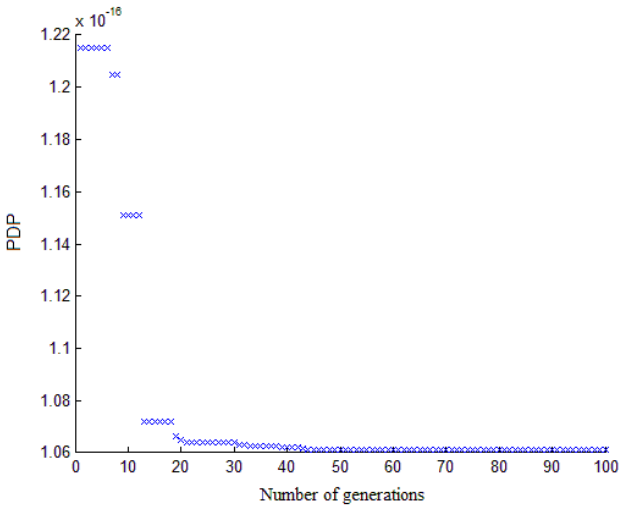

Fig 4. PDP parameter performance for proposed algorithm

6. CONCLUSIONS

A CMOS inverter circuit is designed and optimized in this paper for the main purpose of minimizing the power and delay of the circuit (PDP), using the firefly optimization algorithm in 0.25µm at 2.5v supply voltage. As it is discussed in the paper, to increase the design accuracy, the circuit simulator (HSPICE) is directly used in the MATLAB which implements the firefly optimization algorithm to find a verified and feasible solution with a good accuracy for the design problem in a reduced design time and complexity.

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