SINGLE-PORT FIVE-TRANSISTOR SRAM CELL WITH REDUCED LEAKAGE CURRENT IN STANDBY

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ABSTRACT

In this paper, a new single-port five-transistor (5T) Static Random Access Memory (SRAM) cell with integrated read/write assist is proposed. Amongst the assist circuitry, a voltage control circuit is coupled to the sources corresponding to driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. Specifically, during a write operation, by means of sizing the driver transistor close to bitline to resolve the write '1' issue. In addition, associated with a two-stage reading mechanism to increase the reading speed and to avoid unnecessary power consumption. Finally, with the standby start-up circuit design, the cell can switch to the standby mode quickly, thereby reduce leakage current in standby.

KEYWORDS

Static random access memory, Read/write assist circuitry, Voltage control circuit, Standby start-up circuit

1. INTRODUCTION

Recently, with the digitalization of electronic equipments, semiconductor memories have been used as essential components among various kinds of technical fields. SRAM requires no refreshing and will maintain its information as long as it has sufficient power supplied. This is due to the fact that the SRAM cell includes flip-flop circuitry internally that does not require refreshing. However, it is apparent that SRAM suffers from the disadvantage of relying on too many transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors.

An SRAM cell has three modes of operation, namely read, write and standby [1]. The data stored in the cells may be corrupted when the cells are read. This problem arises from the fact that a higher voltage on the bitline is coupled to a lower voltage in the cell, causing the bitline voltage to drop and the cell voltage to rise. For instance, when a logic '0' stored initially, the voltage rise in the cell may corrupt the data stored. Further, a concern associated with the write operation is that it is relatively difficult to write a logic '1' to the cell if the cell currently stores a logic '0'.

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Accordingly, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written [2].

Memories take up 80% of the die area in high performance processors [3]. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode [4-5]. Recent research has shown that the leakage current will become even greater than the dynamic current in the overall power consumption [6-7]. Typically, there are three major sources of leakage in a MOS transistor, namely subthreshold leakage, gate leakage, and reverse bias junction leakage [8-9]. Amongst them, Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. The GIDL is the result of a deep depletion region that forms in the drain at high drain-to-gate biases. However, Drain-induced barrier lowering (DIBL) is a short-channel effect in MOS transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages [10]. With scaling down of the MOS transistor, each of the leakage sources may increase accordingly, thus resulting in the increase of the total leakage current. As CMOS technology scales down to 90 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption [11]. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than traditional designs when the cell in standby.

The remainder of this paper is organized as follows. Section 2 presents a brief description of standard 6T and 5T SRAM cell topologies. The proposed 5T SRAM cell with integrated read/write assist is described in Section 3. The simulation results of the proposed 5T SRAM cell are discussed in Section 4. Last section is a conclusion and summary for the paper.

2. TRADITIONAL 6T AND 5T SRAM CELL TOPOLOGIES

2.1 STANDARD 6T SRAM CELL

The standard 6T SRAM is built up of two cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bitlines (BL and BLB), as shown in Fig. 1 [12]. The pair of cross-coupled inverters is formed by a pair of load transistors (MP1 and MP2) and a pair of driver transistors (MN1 and MN2) that are stronger than the access transistors. More specifically, the cross-coupled inverters of the memory cell have two storage nodes A and B functioning to store either logic ‘1’ or logic ‘0’. The gates of access transistors are connected to a word line WL. Prior to initiating a read operation, the bitlines are precharged to V_{DD}. The read operation is initiated by enabling the word line WL and connecting the precharged bitlines to the storage nodes.

A concern associated with the read operation is that both BL and BLB are kept high at the beginning of the read operation must not corrupt the value stored in the cell. Therefore, it is desirable to keep the voltage at the storage node which has a logic ‘0’ stored from rising above the trip-voltage of the inverter. In other words, the strength of the access transistors should be less than the strength of the driver transistors for a non-destructive read operation. It is well known that the cell ratio (*CR*) has an effect on access speed and on cell stability. The W/L ratio of the driver transistor to the access transistor is referred to as the cell ratio and can be written as:

$$CR = \frac{(W/L)_{MN1}}{(W/L)_{MA1}} = \frac{(W/L)_{MN2}}{(W/L)_{MA2}} \quad (1)$$

To provide a non-destructive read operation, the cell ratio (*CR*) was conventionally varied from 1 to 2.5 [2]. Similarly, for a successful write operation, it is desirable to bring down the voltage of the storage node A (or B) which has a stored value '1' below the trip-voltage of the inverter. Therefore, both access transistors must be stronger than the load transistors for a successful write operation. The ratio of the load transistor to the access transistor is referred to as the pull-up ratio (*PR*) and can be written as:

$$PR = \frac{(W/L)_{MP1}}{(W/L)_{MA1}} = \frac{(W/L)_{MP2}}{(W/L)_{MA2}} \quad (2)$$

To improve the read-ability of an SRAM cell, cell ratio can be increased, while a lower pull-up ratio is desirable to improve the cell write-ability.

At the end of the read and write operations, the word line voltage is deasserted to ground allowing the cross-coupled inverters to function normally and hold the logic state of the storage nodes.

2.2 TRADITIONAL 5T SRAM CELL

Figure 2 is a circuit diagram of a traditional 5T SRAM cell [13]. As shown in Fig. 2, the access transistor MA2 and bitline BLB in Fig. 1 have been removed to provide a five-transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the standard 6T SRAM cell, while its power consumption is substantially reduced by one half [14].

To guarantee a correct write operation will occur, it is important to note that the storage node A must be pulled up (or down) above (or below) the trip-voltage of INV-2 within the word line WL is logic high, otherwise a write failure will occur. In detail, writing a logic '0' to a cell, when initially storing a logic '1', the high storage node A of the cell has to discharge the bitline BL below the trip-voltage of INV-2. On the contrary, writing a logic '1' to a cell, when initially storing a logic '0', the low storage node A of the cell must be pulled up by the precharged bitline BL above the trip-voltage of INV-2. Undoubtedly, to write the wanted bit properly in the cell, it may be necessary that the access transistor should be very conductive to force the cross-coupled inverters to change its equilibrium condition. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations. These two requirements impose contradicting requirements on cell transistor sizing.

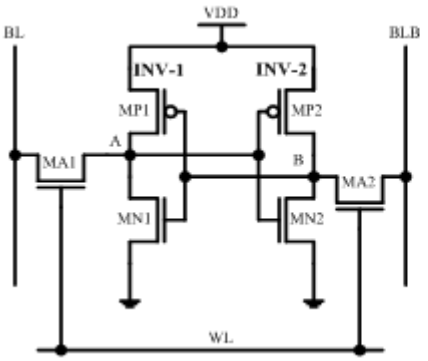

Figure 1. Circuit diagram of standard 6T SRAM cell

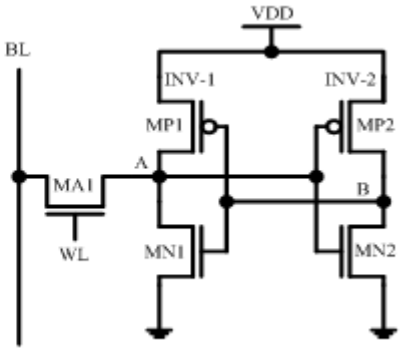

Figure 2. Circuit diagram of traditional 5T SRAM cell

It is well known that it is difficult to write a logic '1' to a memory cell that is storing a logical '0'. In order to resolve write '1' issue of 5T SRAM cells, several techniques have been developed. Some of these techniques rely on boosted word line gate voltage [15-18], reducing the supply voltage V_{DD} [13-14], [19-23], sizing cell transistors [14], [24-25], reduced bitline voltage [26-27], and raising the source voltage V_{SS} [28-31]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process. Hence, there is a need for an effective technique to improve the write-ability of 5T SRAM cells which suffer from inability to write '1'.

3. THE PROPOSED 5T SRAM CELL

3.1 THE PROPOSED 5T SRAM CELL CONFIGURATION

The proposed 5T SRAM cell with a write assist technique is shown in Fig. 4. Unlike the traditional 5T SRAM cell, cross-coupled inverters are asymmetrical by sizing the driver transistor close to bitline BL to improve the write-ability of the cell. Thus, this design has the additional advantage of increased current through the driver transistor during a read operation, and consequently lower read delay than the standard 6T cell. Beyond memory arrays, there are write assist, namely pre-charging circuit, standby start-up circuit and voltage control circuit. In all SRAMs, for each column in the SRAM array there is a bitline BL that connected to the pre-charging circuit. The function of the pre-charging circuit is to pull up the bitline BL of a selected column to V_{DD} before the read or write operation. Furthermore, the standby start-up circuit design is to enable the single-port SRAM to quickly switch to the standby mode, and thus effectively to enhance the standby performance. Besides, the voltage control circuit is connected to the source terminals corresponding to driver transistors of each memory cell in a selected row cells. This configuration is intended to control the source voltages of driver transistors under different operating modes.

During a write operation, the voltage of nodes L1 and L2 are set to the ground voltage. Due to transistor N11 is sized smaller, the issue concerning the difficulty of writing '1' can be resolved. Specifically, the reading operation can be divided into two stages. In the first stage, the voltage of node L1 (V_{L1}) is set to a negative voltage called "RGND" to speed-up the reading speed.

However, in the second stage, the voltage V_{L1} is pulled up to ground to reduce power consumption. Under these circumstances, the voltage RGND can effectively improve the reading speed without incurring unnecessary power consumption. Finally, during a standby operation, V_{L1} and V_{L2} are set to $V_{GS(N23)}$ to reduce the leakage current. Table 1 summaries the operating conditions under different operating modes.

In Table 1, the read control signal RC can be achieved by performing the AND operation on the read enable signal RE (not shown) and its corresponding word line signal WL. It is worth noting that the non-selected word line and non-selected bitline are set to the floating state. However, in the non-reading mode, the voltage of read control signal RC is set to RGND.

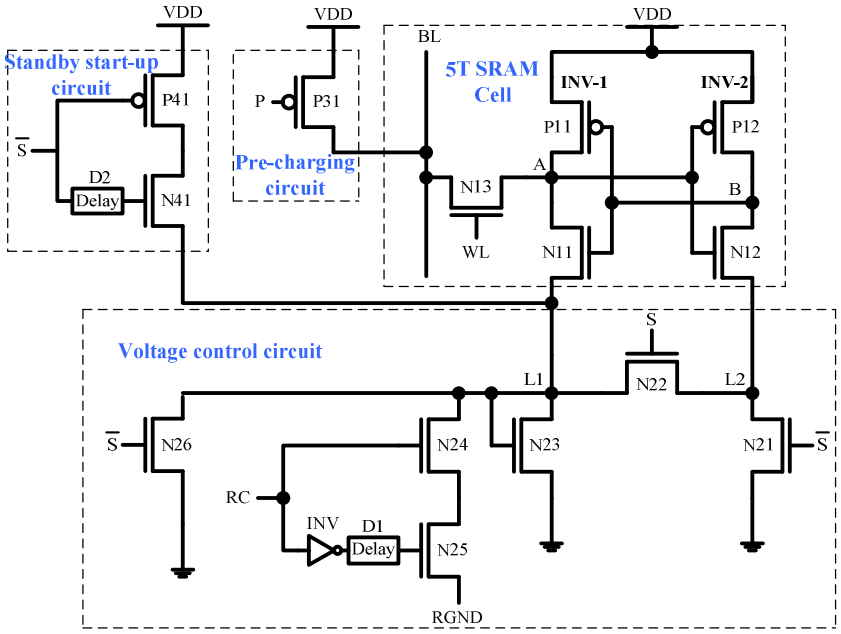

Figure 3. Circuit diagram of the proposed 5T SRAM cell

Table 1. The operating conditions under different operating modes

RC	S	V_{L1}	V_{L2}	mode
RGND	0	0	0	write
V_{DD}	0	RGND (1st stage) 0 (2nd stage)	0	read
RGND	V_{DD}	$V_{GS(N23)}$	$V_{GS(N23)}$	standby

3.2. WRITE OPERATION

Refer to Fig. 3, before and during the write operation is performed, the standby start-up control signal S is at logic low, thereby transistor N26 is turned on, as such V_{L1} is pulled down to ground. During the write '0' operation, the voltage of bitline BL (V_{BL}) is pulled down to logic low and the asserted word line WL turns on transistor N13. Thus, node A is at logic low and node B is at logic high. Conversely, during the write '1' operation, V_{BL} is pulled up to logic high and the asserted word line WL turns on transistor N13. Thus, node A is at logic high and node B is at

logic low. It is worth noting that the W/L ratio of transistor N11 in Fig. 3 is designed smaller than that of transistor MN1 shown in Fig. 1. Consequently, the write '1' problem associated with the traditional 5T SRAM cell can be resolved. Figure 4 shows the simplified circuit diagram during the write operation.

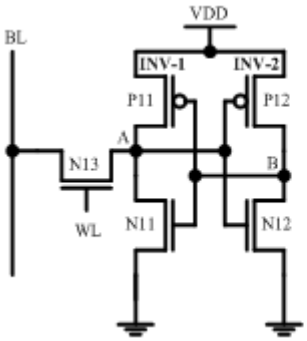

Figure 4. Simplified circuit diagram during the write operation.

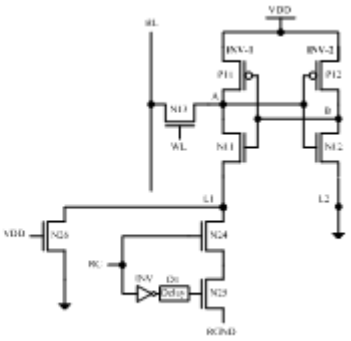

Figure 5. Simplified circuit diagram during the read operation.

3.3. READ OPERATION

The read operation consists of two stages. In the first stage, V_{L1} is pulled down to a negative voltage to speed-up the reading speed. However, in the second stage, V_{L1} is pulled up to ground to reduce the power consumption. Figure 5 shows the simplified circuit diagram during the read operation.

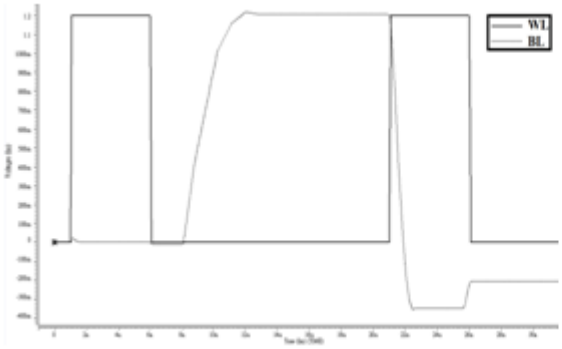

Figure 6. Signal waveforms during a read operation.

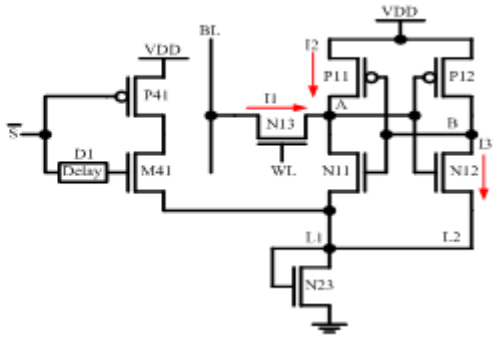

Figure 7. Simplified circuit diagram during the standby operation.

Before the read operation is performed, both the standby start-up control signal S and the read control signal RC are at logic low, thereby both transistors N26 and N25 are turned on and transistor N24 is turned off, as such V_{L1} is pulled down to ground. In the first stage, the read control signal RC is at logic high, thereby transistor N24 is turned on. At this time, since transistor N25 would continue to conduct, V_{L1} is pulled down to a negative voltage RGND. Under this circumstance, the negative voltage RGND can effectively improve the reading speed. In the second stage, the read control signal RC remains at logic high and transistor N24 is continue to conduct. Consequently, V_{L1} is pulled up to the ground voltage in that transistor N25 is turned off, this leads to reduce the power consumption. The two-stage time interval is measured as the time taken from a high on the read control signal RC to the state of the transistor M25 is

turned off. This time interval can be adjusted by the falling time of inverter INV and the delay time of delay circuit D1. Furthermore, either in the first stage or in the second stage, transistor N26 is always on.

3.4. STANDBY OPERATION

Refer to Fig. 3, prior to the standby operation is performed, the inverse standby control signal /S is at logic high so that transistor P41 is off and transistor N41 is on. And then, during the standby operation, the signal /S is at logic low to turn on transistor P41 and turn off transistor N21. In addition, the standby control signal S is at logic high to turn on transistor N22. Consequently, with the conduction of transistor N22, both the V_{L1} and V_{L2} are equal to the threshold voltage of transistor N23 (V_{TN23}). It is worth mentioning that node L1 can be rapidly charged to V_{TN23} at the initial period of the standby mode due to transistor N41 remains on, and thereby improving the standby efficiency. Note that the initial period is determined as the time taken from a low on the signal /S to the state of transistor N41 is off. It is worth noting that after the initial period of the standby mode, transistor N41 is turned off and no current flows. Figure 7 shows the simplified schematic of the proposed design during the standby mode.

4. SIMULATION RESULTS

In traditional 5T SRAM cell, access transistor MA1 is less conductive than driver transistor MN1, thereby making it more difficult to write a logic '1' to cell over a logic '0' stored. Figure 8(a) shows the simulated waveform of a write '1' failure. It's worth noting that sizing of N11 should ensure that INV-2 does not switch causing a destructive read. To elucidate the improvement in write '1' issue, suppose that node A stores '0' and it needs to change to '1' during a write cycle. Before the write operation is performed, both transistors P11 and N12 are off and both transistors P12 and N11 are on. When the write '1' operation is performed, if the voltage of word line WL (V_{WL}) exceeding the threshold voltage of transistor N13 (V_{TN13}), transistor N13 will be turned on. Upon write access shown in Fig. 4, the voltage V_{BL} remains at the precharge level as such transistor N11 remains on and transistor P11 remains off. Effectively, transistors N11 and N13 form a voltage divider whose output is now no longer at zero and is connected to the input of INV-2. Meanwhile, node A can be charged toward $V_{DD} \times (R_{N11} / (R_{N11} + R_{N13}))$, where R_{N11} is the on-resistance of transistor N11, and R_{N13} is the on-resistance of transistor N13, respectively. Since the W/L ratio of transistor N11 is designed smaller than that of transistor MN1 shown in Fig. 1, there will be no destructive reading occurs. In addition, it enables the voltage of node A (V_A) higher than the threshold voltage of transistor N12 (V_{TN12}). Consequently, transistor N12 is on and node B is discharged to a lower voltage level. And then, the voltage V_A rises since transistor N11 is now possess higher resistance value. This higher resistance value helps pulling up node A toward much higher voltage level. Hereafter, by using of INV-2, this much higher voltage V_A will pull node B down to much lower voltage level. Furthermore, by using of INV-1, this much lower voltage level on node B will pull V_A up to much higher voltage. In this way, such operations are alternately repeated until V_A reaches V_{DD}. Hence, the write '1' operation of the proposed cell is accomplished.

To evaluate performance, different SRAM cell structures discussed in this paper were simulated using a 90nm CMOS technology. All simulations were carried out at nominal conditions: V_{DD}=1.2V and at room temperature. The simulated waveform of a successful writing in the

proposed 5T SRAM cell is shown in Fig. 8(b). It is evident that the proposed 5T SRAM cell provides an efficient solution to the write '1' issue, that is, the proposed 5T SRAM cell enabling a logic '1' to be easily written to the SRAM cell, as compared to the traditional 5T SRAM cells.

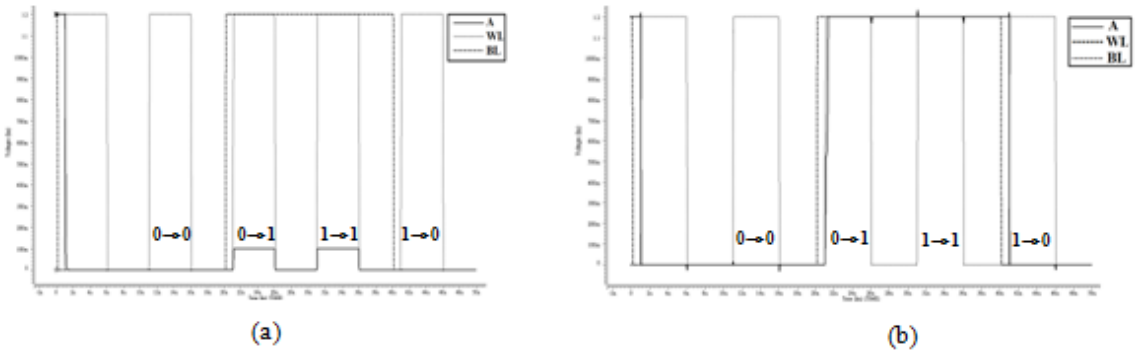

Figure 8. (a) Transient waveforms of a write failure in the traditional 5T SRAM cell, (b) Transient waveforms of a successful writing in the proposed 5T SRAM cell.

Upon standby mode shown in Fig. 7, the voltage V_A remains at V_{TN23}, the voltage V_{WL} is set to the ground voltage and V_{BL} is set to V_{DD}, respectively. Therefore, the gate-source voltage V_{GS} of transistor N13 is negative. In contrast, the V_{GS} of transistor MA1 in Fig. 1 is equal to zero. For NMOS transistors, according to the GIDL effect, the sub-threshold current at V_{GS}=-0.1 is approximately 1% of that at V_{GS}=0. Accordingly, the leakage current I1 flows through transistor N13 caused by the GIDL effect is much smaller than that of flowing through transistor MA1 in Fig. 1. Furthermore, the drain-source voltage V_{DS} of transistor N13 is V_{DD}-V_{TN23}, whereas the voltage V_{DS} of transistor MA1 in Fig. 1 is V_{DD}. According to the DIBL effect, the leakage current I1 flowing through transistor N13 is also less than that of flowing through transistor MA1 in Fig. 1. As a result, the leakage current flows through transistor N13 is much smaller than that flowing through transistor MA1 in Fig. 1. Next, the source-drain voltage V_{SD} of transistor P11 is V_{DD}-V_{TN23} in contrast to the V_{SD} = V_{DD} of transistor MP1 in Fig. 1. According to the DIBL effect, the leakage current I2 flowing through transistor P11 will be less than that of flowing through transistor MP1 in Fig 1. Thus, the base-source voltage V_{BS} of transistor N12 is negative, and the drain-source voltage V_{DS} of transistor N12 is V_{DD}-V_{TN23}. On the contrary, the V_{BS} of transistor MN2 in Fig. 1 is zero, and the V_{DS} of transistor MN2 is V_{DD}. According to the body effect and DIBL effect, the leakage current I3 flows through transistor N12 is much smaller than that of flowing through transistor MN2. From the above analysis, it can be seen that the proposed 5T single-port SRAM having a lower leakage current compared with the standard 6T SRAM. Table 2 shows the standby leakage current for the proposed design and the standard 6T SRAM cell in different corner models.

Table 2. Leakage current comparison

Corner model	Proposed 5T SRAM (pA)	Standard 6T SRAM (pA)	Improvement (%)
TT	2.0576	22.2203	90.7
SS	1.1091	1.6191	31.5
FF	39.3803	309.2402	87.3

As it can be seen from Table 2, compared with the standard 6T SRAM cell in different corner models, the standby leakage current of the proposed design is significantly reduced 90.7%, 31.5% and 87.3%, respectively.

5. CONCLUSIONS

In this paper, a new single-port 5T SRAM cell with a write assist technique is proposed. To speed-up the reading '0' operation, the cell voltage control circuit facilitates such a read operation by supplying the SRAM cell with a speed-up reading voltage RGND that is less than the ground voltage during a read operation. The proposed circuit design is also suitable for technologies below 20nm, with the operating voltage decreased to 1.0V or less. In the write mode, the voltage V_{L1} is set to the ground voltage to improve the writing '1' operation. Furthermore, in the standby mode, both node voltages V_{L1} and V_{L2} are set to a voltage greater than the ground voltage to effectively reduce the standby leakage current. In addition, the standby start-up circuit can make 5T SRAM rapidly switch to the standby mode, and thus improves the standby performance. Particularly, with the effective sizing of the proposed 5T SRAM cell in order to improve write '1' operation is used in simulations. Simulation results for the proposed 5T cell design confirm that there is conspicuous improvement over the standard 6T SRAM cell while it allows writing '1' on the cell with write assist. In addition, with the proposed write assist leads to a 90.7%, 31.5%, and 87.3% less standby leakage in different corner compared with the standard 6T SRAM cell.

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