

# DESIGN OF DIGITAL PLL USING OPTIMIZED PHASE NOISE VCO

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## ABSTRACT

*This paper emphasizes the CMOS implementation of PLL in 130nm technology using Mentor Graphics tool Pyxis. Most of the PLL uses VCO which depends upon variation of supply voltage for high tuning range. Whenever supply voltage changes, the stability will be effected by producing large variations in the frequency output. Since this paper gives the design of current starved or integrator VCO with Schmitt trigger circuit for PLL architecture where instead of varying supply varying the control voltage. In this paper transient analysis, phase noise analysis and jitter analysis of PLL is introduced. This low jittery PLL is further applicable in frequency synthesis, clock recovery that is mainly applicable for wireless communication systems. The PLL gets locked by producing output frequency 1.318GHz with -130dBc/Hz at offset of 10MHz and with cycle to cycle jitter of 5.98ps along with period jitter RMS of 4.92ns. The phase margin is also improved which is 66.280.*

## KEYWORDS

*PD (Phase Detector), LPF (Low Pass Filter), VCO (Voltage Controlled Oscillator), PLL (Phase Locked Loop), PN (Phase noise analysis), SNR (Signal to Noise ratio), ENOB (Equivalent number of bits), BER (Bit Error Rate).*

## 1. INTRODUCTION

In order to keep electronic world properly PLL plays a very important role. Designing of low phase noise and less jittery PLL in generation of clock signals is an important task. Clock signals are required for providing reference timing to electrical system and also to ICs. So in this paper PLL is designed with improved Phase noise and also jitter. Where such types of design is important when sophisticated timing requirements are needed to provide synchronization and distribution of clocks like in ADC, DAC, high speed networking, medical imaging systems. The clock signal's quality depends upon jitter and phase noise. An ideal clock source has zero phase noise and jitter but in reality it has some modulated phase noise. This modulated phase noise spreads the power to the adjacent frequencies, hence produces noise sidebands. The phase noise is typically frequency domain analysis which is expressed in terms of dBc/Hz measured at offset frequency with respect to ideal clock frequency. The low phase noise is important factor mainly in RF and ADC applications. In RF wireless high speed applications, increased PN will leads to channel to channel interference, attenuates quality of signal. In ADC, increased PN limits the SNR and data converter's equivalent no. of bits (ENOB). Jitter is time domain measurement and

expressed in terms of ps (Pico seconds). Jitter can be defined as random variations in the clock signal's edges when compared with actual clock signal that is ideal clock signal. High jitter may lead to higher BER that effects the system requirements. Since low jittery signal can maximizes the rate of performance. So special care has been taken while designing low jittery PLL otherwise it may lead to timing issues. The main contribution for the low phase noise PLL is VCO where VCO acts as heart of PLL. Here in this design the VCO is designed with Schmitt trigger circuit which helps to improve noise immunity. Whenever noisy input signal is applied it generates clean and reliable square wave pulses. As it improves noise margin which leads to optimization in the phase noise.

Mainly PLL is negative feedback system which produces the same frequency and phase output signal as that of input signal to get stable frequency output. PLL multiplies the stable low frequency input signal to get high frequency stable output, which is helpful in high frequency RF wireless systems. Finally in order to improve jitter digital PLL is designed.

## 2. LITERATURE REVIEW

In the early design of PLL, the multiplier can be used as phase detector but the drawback of multiplier is that it has limited lock range. Since instead of multiplier the digital PFD is used. The advantage of PFD over multiplier is PFD has averaged output which is monotonically increasing with the frequency difference between applied input signal and VCO generated output signal if they are different. This is exactly the same condition when the PLL is not under lock condition.

Later, in digital PLL the ring oscillator is used as VCO. It has frequency range from few MHz to several GHz. In this ring oscillator to get high frequency range  $V_{DD}$  has to be increased by making it as  $V_{DD}$  dependent oscillator. This will results high frequency output signals but affects the stability. So in this paper ring oscillator is replaced by VCO with integrator+ Schmitt trigger circuit which is independent of  $V_{DD}$ . To produce high frequency range signals the control voltage is varied instead of  $V_{DD}$  and digital PFD. The multiplier is replaced with digital PFD to reduce the jitter.

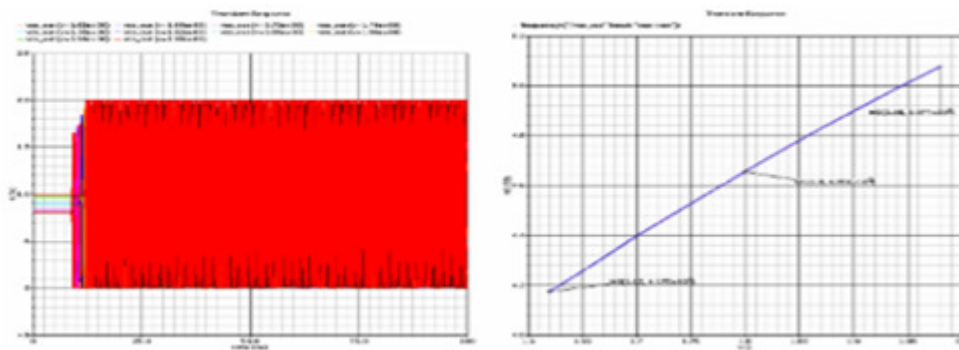


Figure 1 VDD versus output frequency

### 3. RELATED WORK

The block diagram of PLL is given as follows. It consists of three blocks as

- PFD/CP
- LPF
- VCO (integrator+ Schmitt trigger+ CMOS inverter)

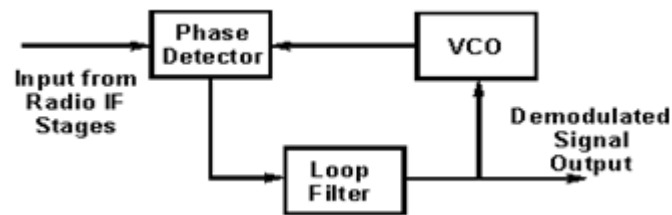


Figure 2 Block diagram of PLL

#### 3.1 PFD/CP

PFD detects the phase and frequency difference between input signal and VCO generated signal, results output voltage which is proportional to the phase error. The gate level implementation of PFD is given as below.

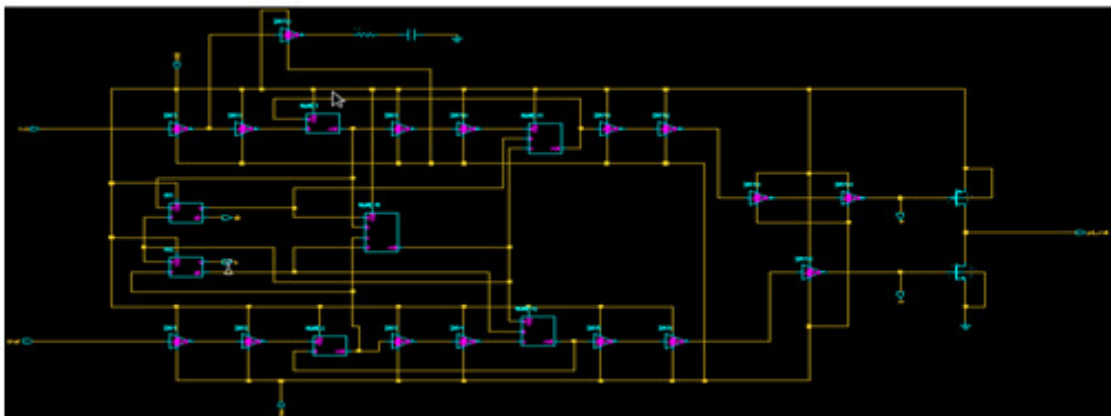


Figure 3 Gate level schematic of PFD

The PFD consists of two SR flip flops and resetting chain. The reset signal is activated when both the inputs are high/valid at the same time. The PFD acts in normal state hence supplies the current, resulting current pulses at the input transition edges. In this design the PFD used is digital one which has the two output levels that are zero and supply voltage level  $V_{DD}$ .

The input supply current of CP/PFD fluctuates with respect to the input signal switching. This analysis is given in four states below.

The PFD/CP operates in four states:

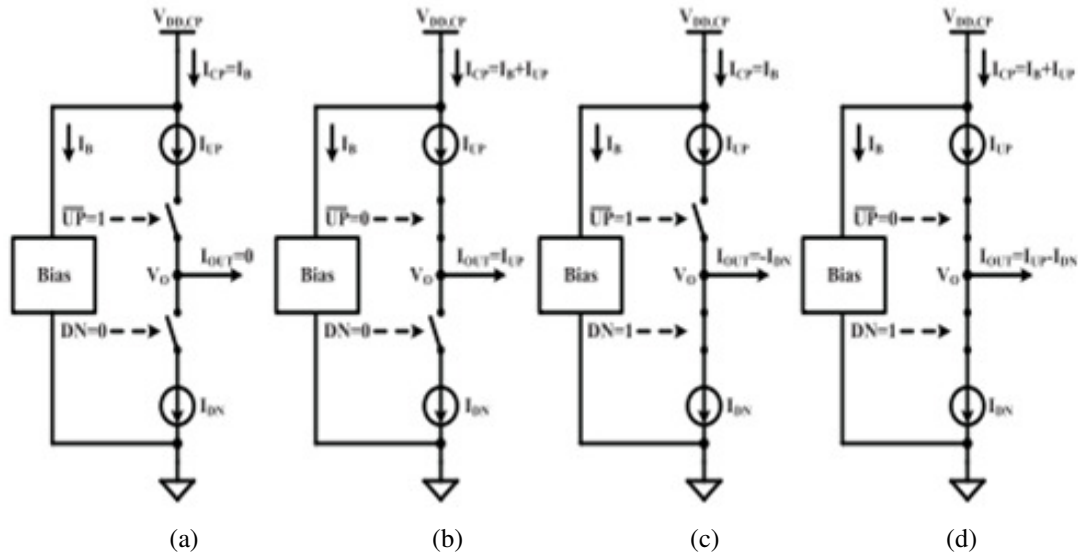


Figure 4 Different states of PFD/CP

Case1:  $\overline{UP}=1$  and  $DN=0$ , then  $I_{OUT}=0$  and  $I_{CP}$  because both discharging and charging switches are turned OFF.

Case2:  $\overline{UP}=0$  and  $DN=0$ , then  $I_{OUT}=I_{UP}$  and  $I_{CP}=I_B+I_{UP}$  because discharging switch is OFF and charging switch is ON.

Case3:  $\overline{UP}=1$  and  $DN=1$ , then  $I_{OUT}= -I_{DN}$  and  $I_{CP}=I_B$  here charging switch is turned OFF while discharging is turned ON.

Case4:  $\overline{UP}=0$  and  $DN=1$ , then  $I_{OUT}=I_{UP} - I_{DN}$  and  $I_{CP}= I_B + I_{UP}$ , in this case both switches are turned ON.

The charge pump pumps in and pumps out the charge from the LPF hence the name Charge pump. The charge pump is used to generate the continuous analog signal from the digital pulses generated from the PFD.

### 3.2 LPF

The LPF is used to suppress the high frequency components that are arrived from the PFD and hence allows only DC voltage which acts as control voltage input to the VCO. The second order LPF RC network is given below which makes the PLL design as third order.

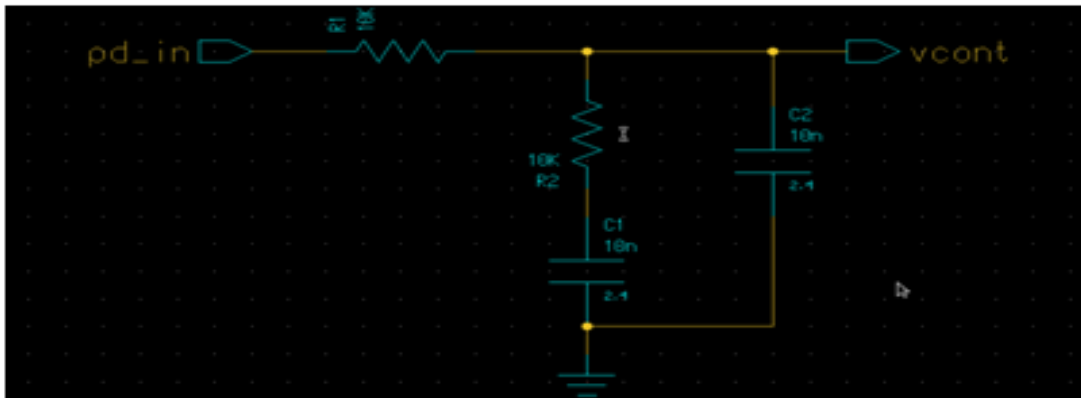


Figure 5 LPF network

In the above LPF, capacitor C2 is added in parallel to the R2 and C1 combination in order to filter out the ripple that is generated by Resistor which will affect the control voltage that is required for VCO. Since this capacitor makes the network second order. In order to provide more stability to loop the R2 is increased but if it is very large it will degrade the stability again.

### 3.3 VCO

VCO is heart of design. It is also source for cause of jitter and phase noise. So care must be taken while designing VCO. VCO responsible for generating frequency output signal from the input voltage hence the name voltage controlled oscillator where by voltage the frequency is controlled. Ideally, most of the applications need linear characteristics of frequency versus control input that is voltage.

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$

Where

$K_{VCO}$ ---gain of VCO in rad/s/V

$\omega_0$ -----frequency at  $V_{cont}=0$

The schematic of VCO consists of three blocks: Integrator, Schmitt trigger circuit and followed by normal CMOS based inverters. The main objective of VCO designing is to reduce the power consumption.

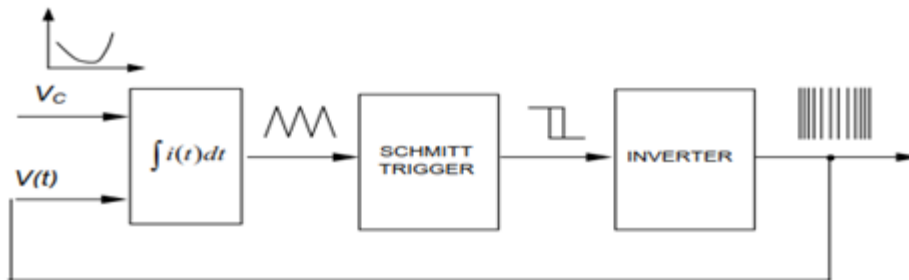


Figure 6 Block diagram of VCO

### 3.3.1 Integrator

Integrator block is main part of the VCO. Integrator block is applicable for high frequency hence it is important block in communication system. Integrator block generally integrates the difference signal which is generated by the comparison of VCO generated signal that is applied as feedback signal with the reference signal that is input signal.

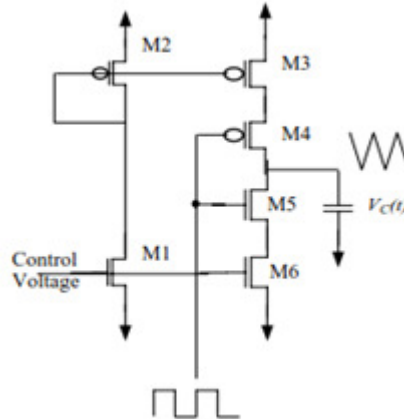


Figure 7 Schematic of Integrator

In the above figure 7, the MOSFETs M1 and M2 acts as current mirror circuits which converts the applied control voltage to the corresponding current. The generated current is mirrored across the transistors M3 and M6 through M4 and M5. The MOSFETs M4 and M5 are responsible for charging and discharging the node capacitance which is at the output side. In order to perform switching actions the square wave input is applied as shown in figure at the gates of M4 and M5. The output capacitor charges whenever the switching signal at the gate is low through M3 and M4 and similarly discharges when switching signal is high through M5 and M6. Since the charging and discharging time constant of nose capacitor is controlled by M4 and M5's drain resistances ( $r_{O4} \parallel r_{O5}$ ) which are in parallel. The time constant of integrator is given as

$$\tau = (r_{O5} \parallel r_{O6})C_{\text{integrator}}$$

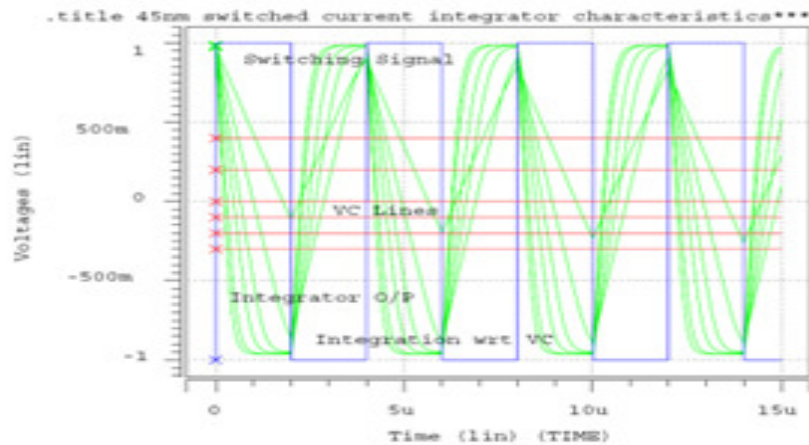


Figure 8 characteristics of integrator

### 3.3.2 Schmitt trigger circuit

Generally, Schmitt circuit is used to generate square wave pulses which are clean and also reliable from noisy input which may be triangular wave or sine wave. Schmitt trigger circuit is generally a comparator which compares the integrator output with the threshold level which is preset and changes the output state whenever it crosses the preset threshold level. The schematic of Schmitt circuit in CMOS is given below

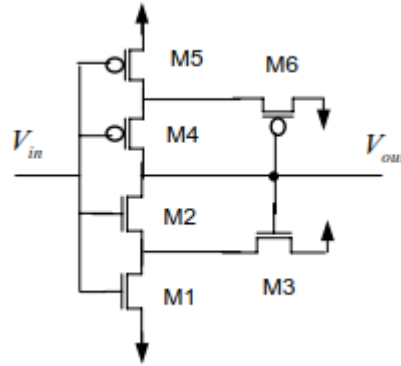


Figure 9 CMOS implementation of Schmitt trigger circuit

The output HIGH-LOW transition occurs when  $V_{in}$  crosses the  $V_H$  that is upper threshold level and similarly LOW-HIGH transition when it crosses the lower threshold level  $V_L$ . In the above figure 9 the MOSFETs M4 and M2 have high threshold voltage than M5 and M1. MOSFETs M3 and M6 are responsible for hysteresis width.

Working: when input voltage is low then M5 and M4 are turned ON while M2 and M1 are turned OFF hence output is at VDD level. When input reaches the threshold voltage of M1 then M1 turns ON while M2 remains in OFF state, because of pass transistor logic M3 also turns ON when M1 turns ON. M2 is turns ON when the input voltage reaches threshold voltage of M2. Hence M3 pulls the node to  $V_{DD}-V_T$  instead of complete supply level. When M1 is turns ON then it pulls the output node between M2 and M1 and when M2 turns ON then there will be low logic level at the output node. This high voltage level is called as  $V_{IH}$ .

When input voltage is logic high then M1 and M2 are turned ON while M4 and M5 are turned OFF. Similarly M6 corresponds to  $V_{IL}$  that is low voltage switching point.

There are few cases such as

Case 1: when (W/L) ratio of M3 varies this will affect the  $V_{IH}$  because in this region NMOS is in strong condition. Similarly,  $V_{IL}$  will get affected when W/L of M6 varies.

Case 2: when W/L of M1 varies, in this case NMOS is strong hence it will pull out the node to low logic output sharply as a result the curve shifts to left.

Case 3: W/L ratio of M4 will results the shifting of curve to right because PMOS is in strong condition hence pulls the output node TO VDD.

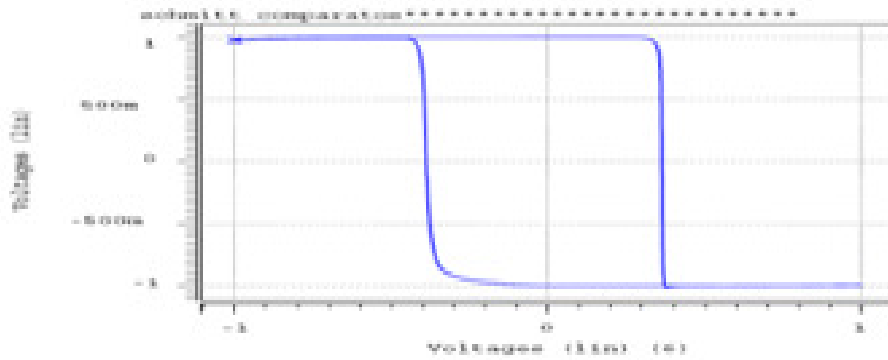


Figure 10 Hysteresis curve

The complete integrated blocks of VCO:

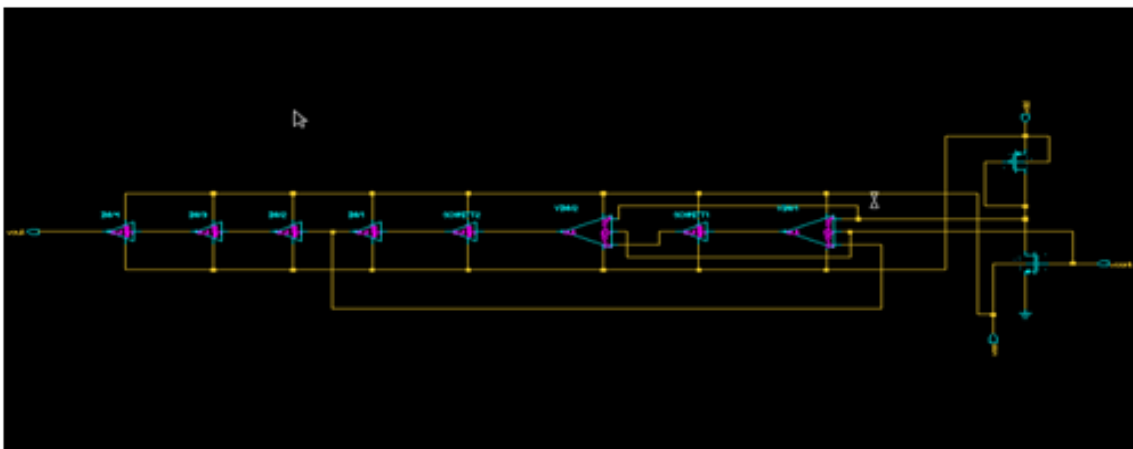


Figure 11 Complete schematic of VCO

The complete PLL architecture:

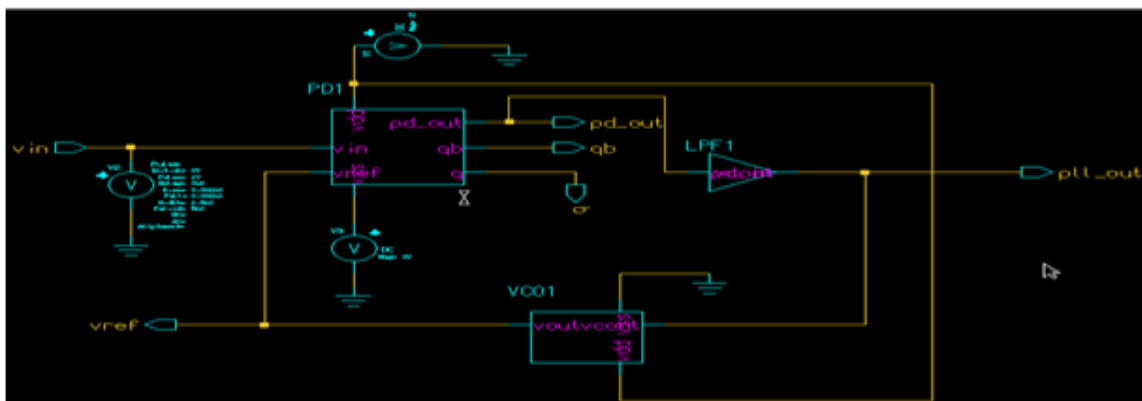


Figure 12 PLL schematic



#### 4. SIMULATION RESULTS AND DISCUSSION

The output frequency of PLL is

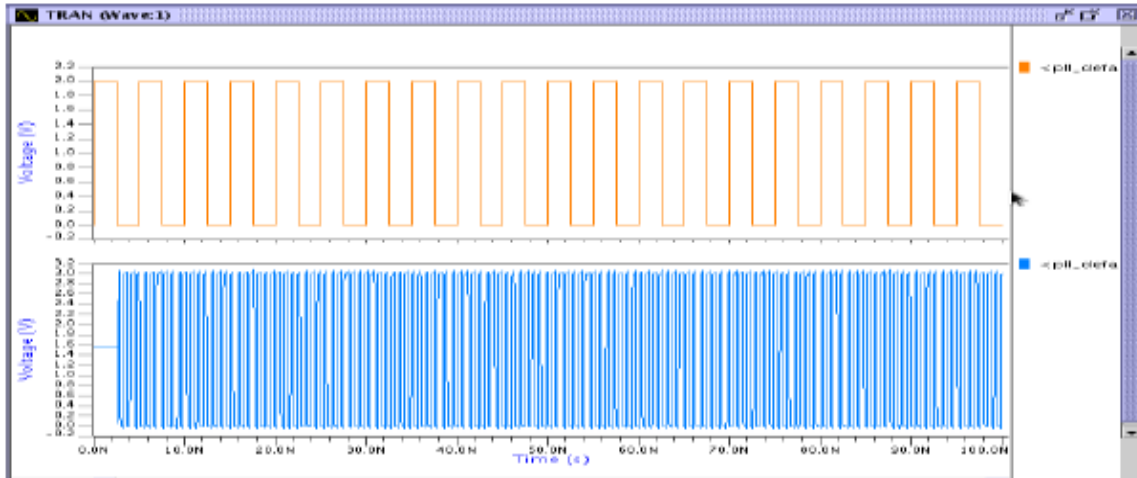


Figure 13 PLL output

The PLL generates 1.312GHz frequency output. PLL operates at 3V supply. In the above figure 13 the blue colour waveform is VCO generated output. The PLL consumes 58mW of power.

The test circuit of PLL design is:

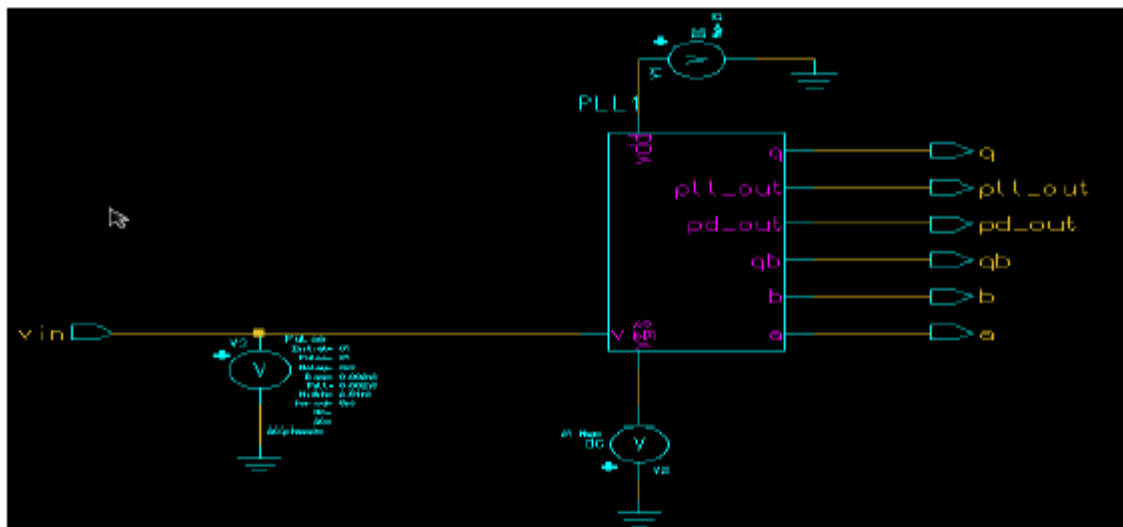


Figure 14 test circuit of PLL

The test circuit operates at 1.9V.

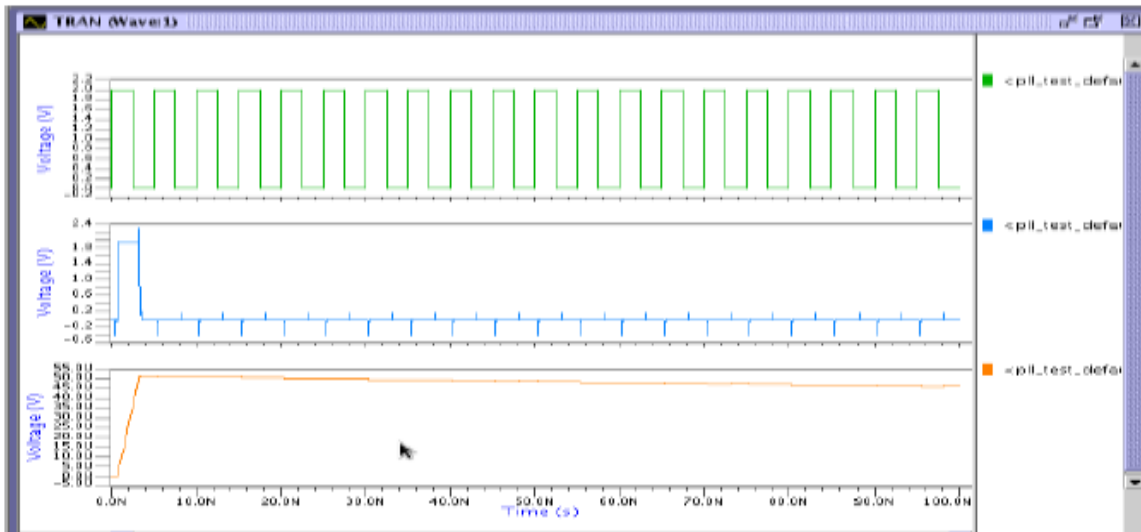


Figure 15 output waveform of PLL closed loop system

The transient analysis of PLL with feedback is given in figure 15. The PLL gets locked after 5ns in the above figure.

Output of VCO for 3V supply and 1V input control voltage. The VCO generates 1.7132GHz frequency when 1v input control voltage is applied.

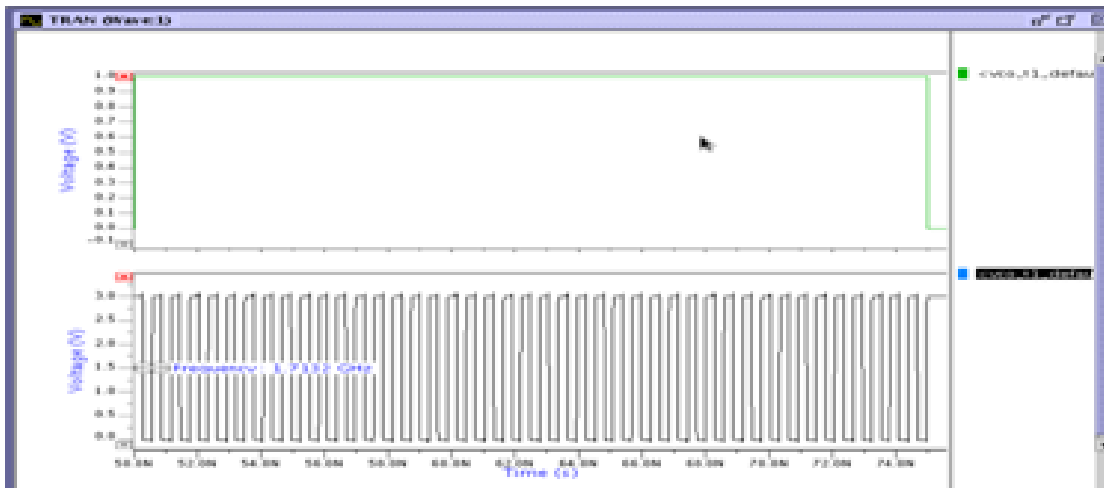


Figure 16 output waveform for VCO

The control voltage Vs Frequency output is given in below table 1

Table 1 Frequency Vs control voltage

0.42V	152.89MHz
0.6V	686.01MHz
0.8V	1.315GHz
1V	1.7970GHz
1.2V	2.1819GHz
1.4V	2.4643GHz
1.8V	2.873GHz
2V	2.9971GHz
2.2V	3GHz
2.4V	3.134GHz
2.6V	3.2GHz
2.8V	3.2209GHz
3V	3.2406GHz

VCO characteristics:

Centre frequency of VCO: it is the frequency at the mid-range of control voltage. Since the applications depends upon the centre frequency of VCO where it can be used.

Power consumption: power consumption depends upon/loggerheads with noise and frequency that is speed. If power consumption is more, it enables the VCO for high frequencies and results in more immune to noise. Low power enables the VCO with limited frequency range and also results difficulties in distinguishing the noise from signal hence degrade the SNR.

Tuning range: this is the range over which frequency output of VCO changes with respect to the applied control voltage.

VCO gain: it is expressed in terms of rad/S/V.

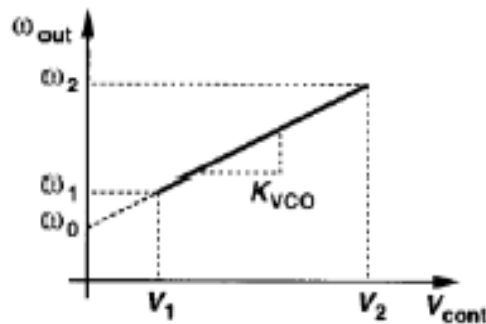


Figure 17 gain of VCO

The cycle to cycle jitter RMS of PLL is given as

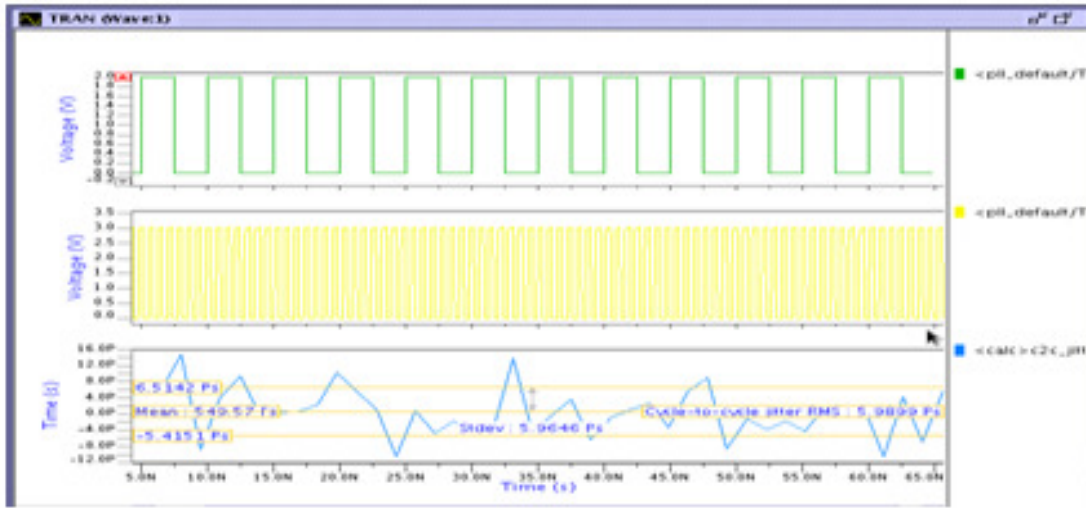


Figure 18 Cycle to Cycle jitter

From the above figure 17, it is clear that the jitter RMS is 5.98ps.

The Peak to Peak jitter RMS is given as 4.2652ns.

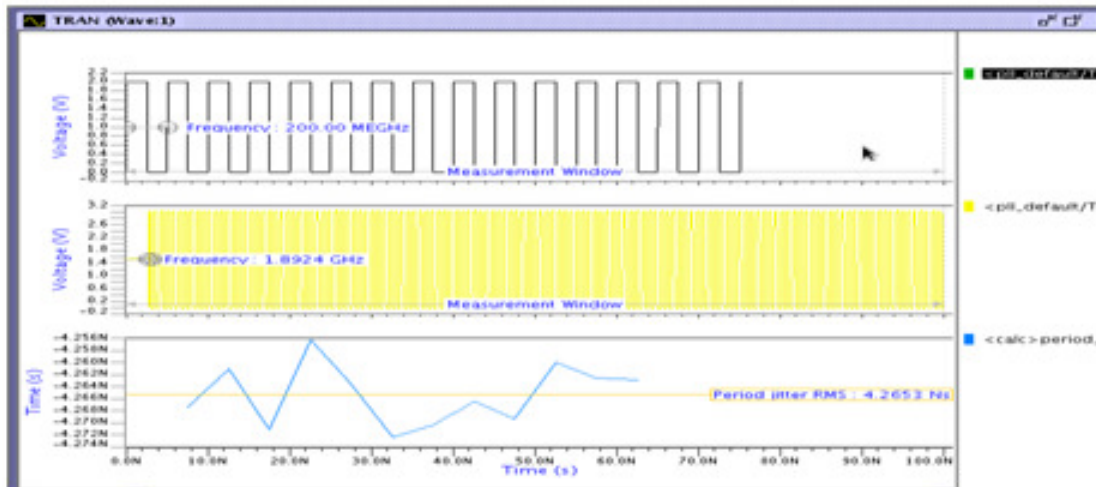


Figure 19 Period jitter RMS for PLL

Phase noise of VCO is -130dBc/Hz at offset of 10MHz. The phase noise is frequency domain analysis which will affect the frequency stability of PLL. Hence phase noise of VCO in this paper is improved.

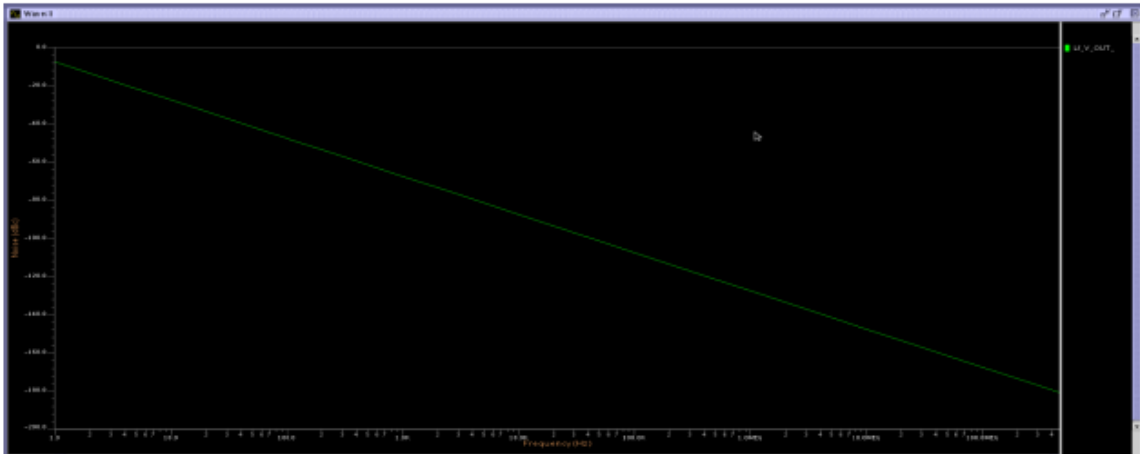


Figure 20 Phase noise analysis of VCO

The FFT analysis of PLL which will help to calculate the SNR of PLL:

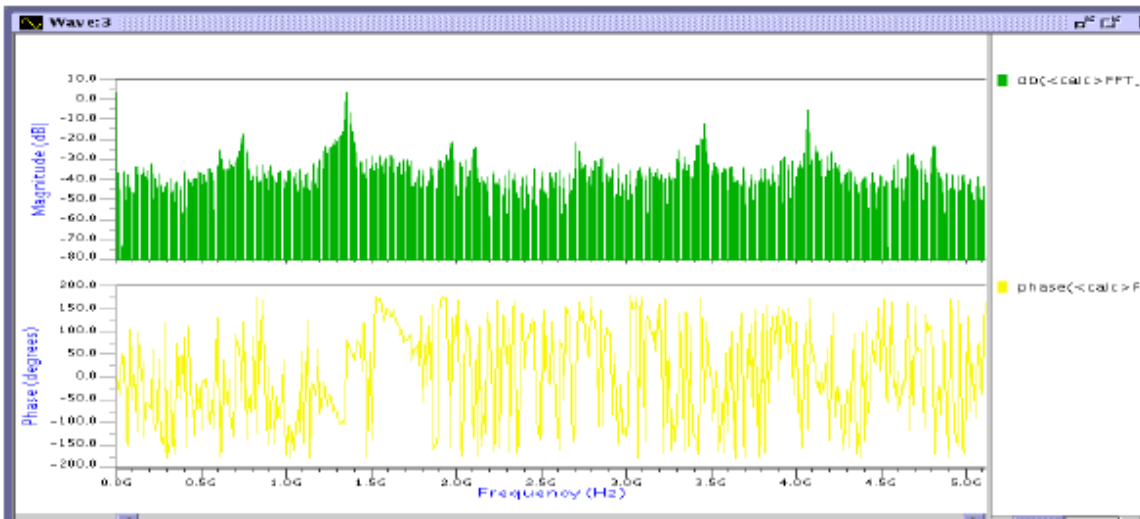


Figure 21 FFT analysis of PLL

The SNR is 36dB. SNR function computes the SNR of input signal by using the FFT result's gain.

From the following equation SNR is computed for input.

$$10 \log_{10} \left( \frac{\sum |AS(f)|^2}{\sum |AN(f)|^2} \right)$$

Where

$\sum |AS(i)|^2 =$  sum over all squares of amplitudes of the sinusoidal frequencies

$\sum |AN(j)|^2 =$  sum over all squares of noise amplitudes of the signal

Power consumption of VCO for 1V and 3V supply:

VOLTAGE SOURCE CURRENT			
NAME	CURRENT	VOLTAGE	POWER
V1	0.0000	0.0000	0.0000
V2	-240.4113U	1.0000	-240.4113U
TOTAL POWER DISSIPATION:			240.4113U WATTS

VOLTAGE SOURCE CURRENT			
NAME	CURRENT	VOLTAGE	POWER
V1	0.0000	0.0000	0.0000
V2	-3.8599M	3.0000	-11.5796M
TOTAL POWER DISSIPATION:			11.5796M WATTS

From the above result for power consumption of VCO, 1V supply VCO has limited range but have low power consumption 240.4113μW hence this can be used for low power application. The VCO with 3V supply has range from 0.152GHz to 3.24GHz which is used in RF wireless communication system which consumes 11.04mW power.

The PLL acts as low pass filter to suppress the high frequency components of PFD and acts as high pass filter to suppress the jitter of VCO.

Specifications of PLL designed:

Table 2 Specification of PLL

Input frequency	100MHz
Gain of PFD ( $K_{PFD}$ ) in rad/V	0.48 rad/V
Gain of VCO ( $K_{VCO}$ ) in Hz/v	1.24GHz/V
Tuning range	182.22%
Power consumption	58mW
Centre frequency	1.776GHz
Jitter RMS	5.98ps
Output frequency	1.312GHz
Power supply	3V

Comparison table for VCO

Table 3 Result comparison table

parameters	[13]	[4]	[7]	[11]	[8]	proposed work
Operating frequency(GHz)	0.39-1.41	0.12-1.3	0.528	0.0022-0.008	0.125-2.4	0.152-3.2406
Phase Noise	no	yes	yes	no	no	yes
VDD (V)	1.8	0.5	1.8	0.5	1.8	1-3
Technology(nm)	180	180	180	180	180	130
Power consumption (mW)	12.5	0.085	143	14.5	19.8	11.5796
Passive components used	yes	yes	no	yes	yes	yes

## 5. CONCLUSION AND FUTURE SCOPE

The PLL in this paper is designed in 130nm technology using Mentor Graphics tool. The designed PLL is locked by generating 1.312GHz frequency output signal which can be used for RF wireless communication system. The PLL has jitter RMS value of 5.98ps and peak-peak jitter RMS is 4.2652ns, these two parameters are important factor for ADC and RF systems. If jitter is more than it will produces timing issues which are required for clock synchronization and distribution in systems such as medical imaging, ADC, DAC and Communication System The power consumption of PLL is 58mW. The power consumption of VCO designed is 24.4113 $\mu$ W for 1V supply which has limited frequency range hence used for low power applications which is required for longer battery life. The power consumption of VCO for 3V supply is 11.04mW which has frequency range from 0.152GHz to 3.240GHz, hence used in HF applications. The phase margin for implemented PLL is 66.28<sup>0</sup>. The phase noise of VCO at 10MHz frequency is -130dBc/Hz. The future scope of design is further reduction of jitter RMS value by applying power grid circuit which consists of R and C to the entire circuit [16].

## REFERENCES

- [1] J. Craninckx and M. Steyaert, "A 1.8-GHz low-phase noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, pp. 736–744, May 1997.
- [2] Yalcin, A.E. and P. John, 2004. A 5.9-GHz voltage controlled ring Oscillator in 0.18  $\mu$ m CMOS technology. *IEEE J. Solid-State Circuit*, 39(1): 230-233.
- [3] C. H. Park and B. Kim, "A low-noise, 900-MHz VCO in 0.6- $\mu$ m CMOS" *IEEE J. Solid-State Circuits*, vol. 34, pp. 586–591, May 1999.
- [4] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Phase noise in multi-gigahertz CMOS ring oscillators," in *Proc. IEEE 1998 Custom Integrated Circuit Conf.*, 1998, pp. 49–52.
- [5] T. Friedrich, "Direct phase noise measurements using a modern spectrum analyser," *microwave J*, vol. 35, pp. 94,96,99,101-104, Aug. 1992.

- [6] K. M. Ring and S. Krishnan, "Long-term jitter reduction through supply noise compensation," in Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'08), pp. 2382–2385, Seattle, Wash, USA, May 2008.
- [7] Y. Chen, Z. Wang and L. Zhang, "A 5GHz 0.18- $\mu$ m CMOS technology PLL with a symmetry PFD," in Proceedings of the International Conference on Microwave and Millimetre Wave Technology (ICMMT'08), vol. 2, pp. 562–565, Nanjing, China, April 2008
- [8] Rahajandraibe, A.W., L. Zaid, V.C. de Beupre and J. Roche, 2007. Low-gain-wide-range 2.4-GHz phase locked loop. 14th IEEE International Conference on Electronics, Circuits and Systems, pp: 26-29.
- [9] S. B. Rashmi and Siva S. Yellampalli, "Design of Phase Frequency Detector and Charge Pump for High Frequency PLL," International Journal of Soft Computing and Engineering, vol.2, Issue-2, May 2012, pp 88-92.
- [10] V.Lule and V.Nasre, "Area efficient 0.18 $\mu$ m CMOS phase frequency detector for high speed PLL", International Journal of Engineering Scientific and Research Publication, vol.2, Feb. 2012, pp 1-3.
- [11] Chakraborty, B. and R.R. Pal, 2007. Study of speed enhancement of a CMOS ring VCO. J. Phys. Sci., 11: 77-86.
- [12] M. Shahruz, "Novel phase-locked loops with enhanced locking capabilities," Journal of Sound and Vibration, Vol. 241, Issue 3, Pages 513-523, 29 March 2001.
- [13] Sung-Rung Han, Chi-Nan Chuang, and Shen-Iuan Liu, Member, IEEE, "A Time-Constant Calibrated Phase-Locked Loop With a Fast-Locked Time", IEEE transactions on circuits and systems, vol. 54, no. 1, January.
- [14] Behzad Razavi, "Design of Analog CMOS Integrated Circuits".
- [15] Ronald E. Best, "Phase-Locked Loop Design, Simulation and Applications" Fifth Edition.
- [16] Bo Zhao and Huazhong Yang " Supply-Noise Interactions Among Sub modules Inside a Charge-Pump PLL" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, year: 2015, Volume: 23, Issue: 4.