LEAKAGE REDUCTION TECHNIQUE AND ANALYSIS OF CMOS D FLIP FLOP

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ABSTRACT

Power consumption and delay are the two major issues in the design of today's VLSI based battery operated portable electronic devices. Memory units in these devices are made of flip flops and each flip flop will consume more power in both active and idle conditions. Through this paper we try to explore alternate techniques to implement D flip-flop with the aim of reducing leakage power, delay and to increase the speed. All the different configurations of D flip-flops are simulated using HSPICE in 90nm process technology with BSIM4 MOS transistor models of level 54.

KEYWORDS

Pass transistor, Transistor stacking, Leakage Power, LECTOR, VCLEARIT

1. INTRODUCTION

The expansion of battery operated portable device is continuously increasing the demand for low power, minimum delay and high speed integrated circuits. In many of the portable devices the standby periods are longer than the active periods and thus consume more power in the standby state [2]. It is extremely important to reduce the power consumption in the standby mode. In today's high performance integrated circuits the leakage power contributes major power consumption than overall total power consumption. In deep submicron circuits the leakage power increases than the dynamic power and also in the circuits when there are no transitions at the input and the transistors are in steady state [1]. Leakage power is mainly due to leakage current that flows in the circuit when the circuit is operated in sleep or standby mode. The leakage current is composed of sub-threshold leakage current, gate current, gate leakage current and reverses biased leakage. Among all leakages, sub-threshold leakage contributes major part of the leakage. The sub-threshold leakage current of a metal oxide semiconductor device is expressed as

$$I_{leakage} = I_o e^{\frac{Vgs-Vth}{\eta Vt}} \left(1 - e^{\frac{Vds}{Vt}}\right) \quad (1)$$

Where $I_o = \mu_o C_{ox} \frac{W}{L} V_t^2 e^{1.8}$, μ_o is the mobility of electrons/holes, C_{ox} denotes oxide capacitance of gate per unit area, W and L are width and channel length of MOS device respectively, Vgs is the gate to source voltage Vt is the thermal voltage and η is the swing coefficient. The contents of this paper are organized as follows: Section 2 describes some of the

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work related to flip flops. Section 3 presents the design of D flips flop using MTCMOS technique, pass transistor and pass transistor with transistor stacking. Section 4 presents two D flip flop designs using LECTOR and VCLEARIT techniques. Section 5 gives the performance comparison of the proposed flip flops. Section 6 draw the conclusion on the results obtained.

2. LITERATURE REVIEW

Flips flops are the basic memory and critical timing elements in digital systems. Flip flops consumes more power both in active and idle mode and have large impact on speed and delay. Researchers are continuously finding new techniques in the field of sequential circuits for reduced power, delay and increased speed. In [5] author proposes a mixed and multi Vt flip flop that reduces leakage power with slightly increased delay. In [6] author describes power gating method of reducing the leakage power in a two phase complementary pass transistor adiabatic logic. A clock skew scheduling algorithm to control leakage power is proposed in [7]. A conventional data retention flip flop that uses a balloon latch applied to a transmission gate flip flop is presented in [8]. A dual Vt method of reducing leakage power is enumerated in [9]. This scheme assigns low threshold transistors to critical path and high threshold transistors to non critical path to reduce leakage currents. D flip flop implementation using GDI technique is proposed in [10]. In [16] author presents GDI multiplexer technique for the design of flip flop and describes two architecture for it. Threshold voltage tuning methodology is proposed in [11] to suppress the ground bouncing noise. A forward body bias generator is used to dynamically tune the threshold voltage in different mode of operation of noise aware data preserving sequential MTCMOS circuits. In [12] author presents a scheme for ultra low power system using power gating to reduce leakage power dissipation in flip flops Sub clock power gating scheme is proposed in [13] to minimize leakage power. During active mode leakage is controlled by clock gating. In [14] self adjustable voltage level circuit is presented for controlling leakage power. During active mode the self adjustable circuit supplies maximum voltage to the load and in the silent mode lower voltage to the load. A clocked pair shared flip-flop (CPSFF) using Multi-Threshold CMOS technique is presented in [17]. Double edge triggering and low swing clocking is implemented in the clocking system. In [18] author presented a modified Single Edge Triggered D flip flop design for various substrate bias voltages. In this design substrate of all NMOS transistors are connected to supply and substrate of all PMOS transistors are connected to ground.

3. CMOS D FLIP FLOP IMPLEMENTATION

D flip flop is widely used in the design of sequential circuits and memory storage devices. Design of high speed and low power memory elements is desirable for the today's battery operated portable devices. Three different design of D flip flops are outlined in this section. Design 1 uses MTCMOS technique that uses high V_t PMOS and NMOS devices to minimize leakage current in the silent mode. The circuit is implemented by adding sleep transistors in the pull up and pull down network of the 5T latch circuit is as shown in the fig. 1. When input and CLK is high the transistors T1 and T5 are OFF and a transistor T2, T3 and T5 are ON and causes the output to follow input. In this circuit high threshold transistors are used for sleep transistors. In the active mode, the high V_t transistors are turned ON to keep the low Vt transistors to operate with low switching power dissipation and minimum delay. In the idle mode high V_t transistors are turned OFF to cut off the conduction path such that any leakage currents arise from internal circuitry can be controlled. Design 2 uses master slave latch configuration to built flip flop using

inverters and pass transistors as shown in the fig.2. When CLK is low PMOS loop transistor in the two series connected inverters are ON and other two series inverters are OFF. The state of the flip flop is changed during falling edge of the clock. Design 3 describes stack based D flip flop using pass transistor shown in the fig 3. By taking width of stacked transistor equal to half of the width of the single transistor the leakage across stacked transistor is lowered compared to the single transistor. The lower transistor in the stacked configuration induces a reverse bias to the below transistor thus increases the threshold voltage which in turn controls the leakage current.

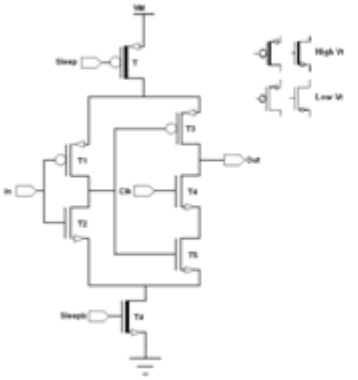

Fig. 1 D FF using MTCMOS

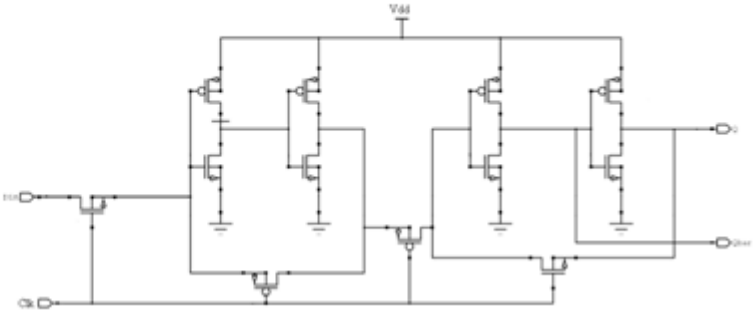

Fig. 2 D FF using pass transistor

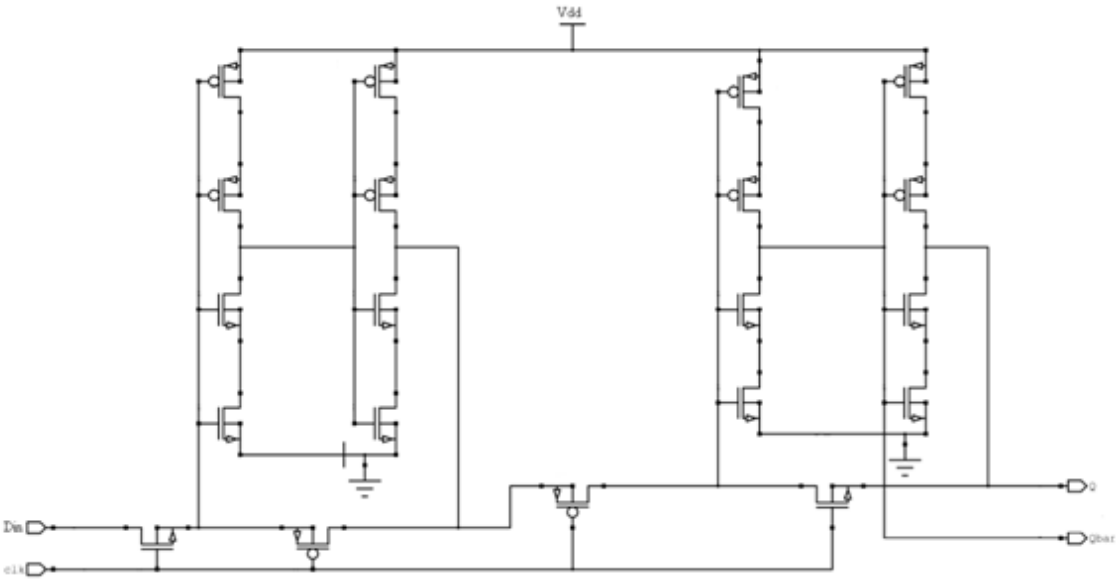

Fig. 3 D FF using pass transistor with transistor stacking

4. PROPOSED TECHNIQUES

In this section two leakage reduction techniques such as LECTOR and VCLEARIT based on transistor stacking is described.

4.1. STACK EFFECT

Stacking effect is known as turning OFF of more than one transistor in a stacked series connected transistors to control leakage current. When two or more stacked transistors are turned OFF, results in reduced DIBL effect. The model presented here is taken from leakage reduction model in [3] and [4]. The leakage current I_{sub0} for a single turned-off transistor shown in fig. 4(a)

$$I_{sub} = Ae^{\frac{1}{nVt}(Vgs-Vth-\gamma Vsb+\eta Vds)}\left(1-e^{\frac{-Vds}{Vt}}\right) \quad (2)$$

$$I_{sub} = Ae^{\frac{1}{Vt}(-Vth0+\eta Vdd)} \quad (3)$$

Where $A = \mu_0 C_{ox}(W/L_{eff})V_t^2 e^{1.8}$ Vt is thermal voltage, Vgs is the gate to source voltage, n is the sub-threshold swing coefficient, Vth is the threshold voltage, Vds is the drain to source voltage, Vsb is the source to body voltage, μ_0 is the zero-bias voltage, W is the width, Leff is the effective channel length, γ is the body-effect coefficient, η is DIBL coefficient and C_{ox} is the gate oxide capacitance.

The leakage current of the stacked turned-off transistors shown in fig. 4(b) are

$$I_{sub0} = Ae^{\frac{1}{nVt}(Vgs0-Vth0-\gamma Vsb0+\eta Vds0)}\left(1-e^{\frac{-Vds0}{Vt}}\right) \quad (4)$$

$$I_{sub0} = Ae^{\frac{1}{Vt}(-Vx-Vth0-\gamma Vx+\eta(Vdd-Vx))} \quad (5)$$

$$I_{sub1} = Ae^{\frac{1}{nVt}(Vgs1-Vth1-\gamma Vsb1+\eta Vds1)}\left(1-e^{\frac{-Vds1}{Vt}}\right) \quad (6)$$

$$I_{sub1} = Ae^{\frac{1}{Vt}(-Vth0+\eta Vx)}\left(1-e^{\frac{-Vx}{Vt}}\right) \quad (7)$$

Assuming $W_{n0} = W_{n1} = W_n$ also $1>>e^{Vds0/Vt}$ the sub-threshold leakage current reduction factor can be expressed as

$$X = \frac{Isub}{Isub0} = \frac{Ae^{\frac{1}{Vt}(-Vth0+\eta Vdd)}}{Ae^{\frac{1}{Vt}(-Vx-Vth0-\gamma Vx+\eta(Vdd-Vx))}} = e^{\frac{Vx}{Vt}(1+\eta+\gamma)} \quad (8)$$

Where V_x is the voltage between source of N_0 to source of N_1 can be obtained by solving $I_{sub0} = I_{sub1}$

$$Ae^{\frac{1}{nVt}(\eta Vdd-Vx((1+2\eta+\gamma))} + e^{\frac{Vx}{Vt}} = 1 \quad (9)$$

Solving equations (9) and (10) to obtain leakage power reduction factor X. This factor is depends only on the process parameter η and γ, hence leakage through stacked transistor is less than single off transistor.

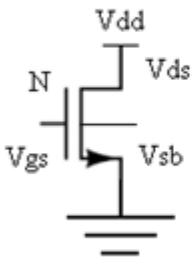

Fig. 4(a) Single transistor

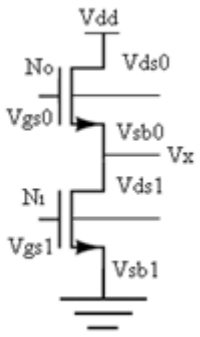

Fig. 4(b) Stacked transistor

4.2 LECTOR (LEAKAGE CONTROL TRANSISTOR) APPROACH

[15] In this approach D flip flop using pass transistor is modified by inserting self controlled leakage control transistors (LCT's) between pull up and pull down circuit as shown in the fig. 5. One of the leakage transistors is always drives near the cut OFF for any input combination. The gate of the LCT's is controlled by the source of the other. These leakage control transistor provides sufficient resistance between supply and ground during standby mode and hence reduces the leakage current.

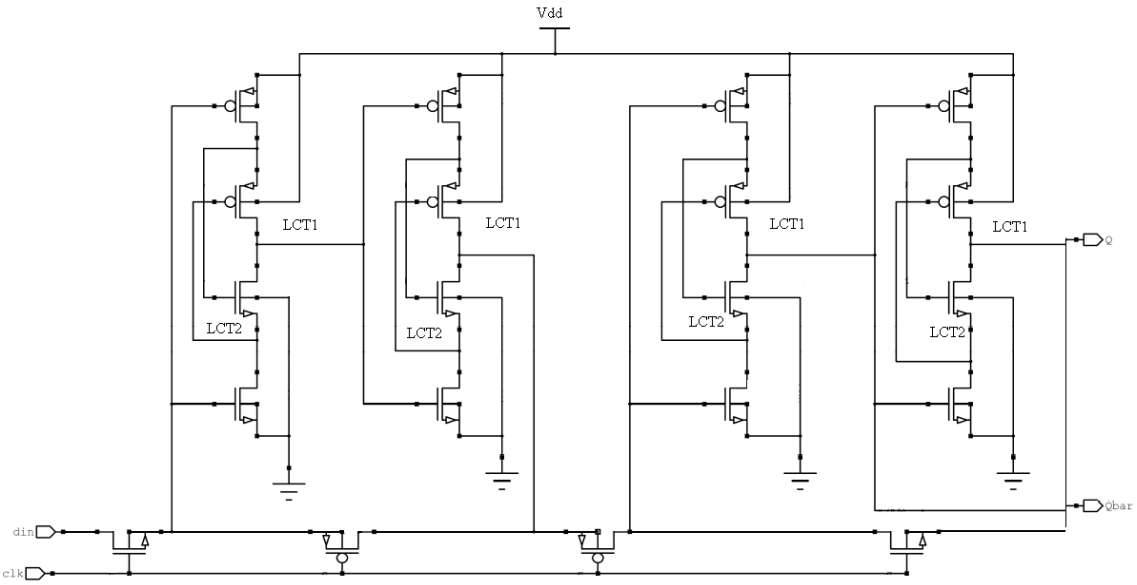

Fig. 5 D FF using LECTOR approach

4.3 VCLEARIT (VLSI CMOS LEAKAGE REDUCTION) APPROACH

[16] In this approach a combination of high Vt and standard Vt to sleep transistors are connected between pull up and pull down circuit of the D flip flop using pass transistor as shown in the fig. 6. During standby mode these sleep transistor are ON, providing a direct path from supply to ground through high Vt transistor. Thus leakage loss is only through the high Vt transistor which is turned OFF. In the active mode the sleep transistor are OFF to behave like CMOS logic.

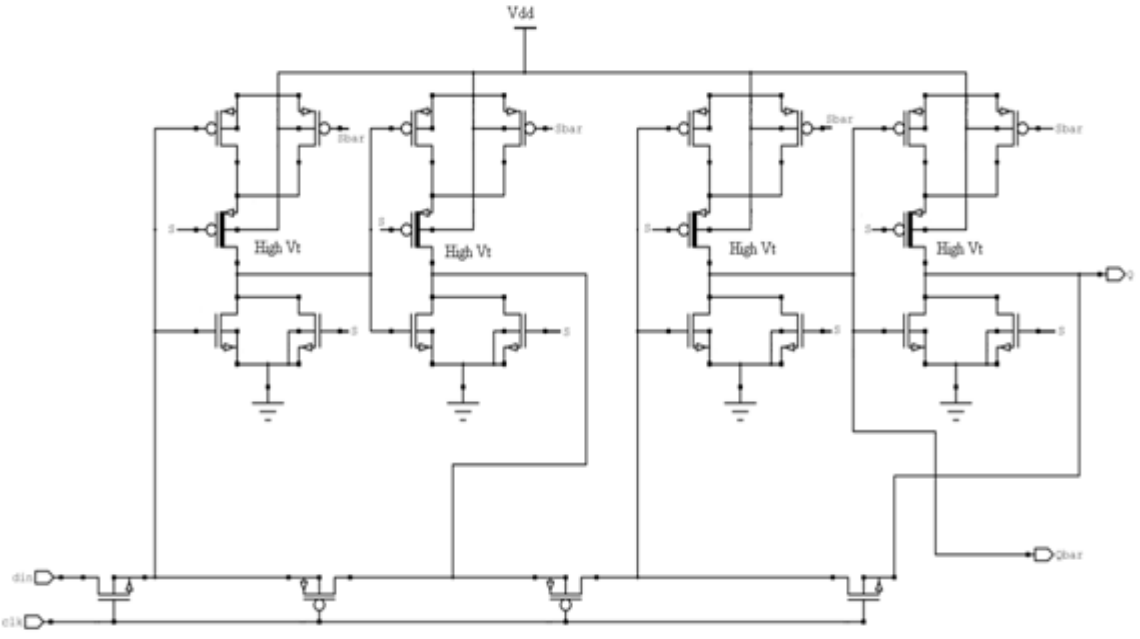

Fig. 6 D FF using VCLEARIT approach

5. SIMULATION RESULTS

In this work we implemented two designs of D flip flop using stack based LECTOR and VCLEARIT techniques in 90nm CMOS process technology. HSPICE simulator is used to simulate all circuit schematics of various approaches. Simulation is done with 1 volt supply and 1GHz clock frequency, at a temperature of 27^{o}C. The net lists are extracted and simulated using BSIM4 MOSFET models of level 54. The power consumption, delay and leakage power of the existing D flip flops are given in table 1. The comparison of power consumption delay and leakage power of the proposed D flip flops are given in table 2.

Table 1: Power computation and Delay of D FF's at 1GHz clock frequency

D flip flop using	No. of transistors	Avg. Power consumption (µW)	Delay (ns)		Avg. Leakage power (nW)
			CLQ-Q		
			LH	HL	
MTCMOS technique	5	5.549	0.96	0.248	14.67
Pass transistors	12	5.29	3.57	2.037	11.59
Pass transistor with stack	20	15.52	1.65	2.094	10.01

Table 2: Power computation and Delay of proposed D FF's at 1GHz clock frequency

D flip flop using	No. of transistors	Avg. Power consumption (µW)	Delay (ns)		Avg. Leakage power (nW)
			CLQ-Q		
			LH	HL	
LECTOR approach	20	36	1.72	2.13	1.194
VCLEARIT approach	24	16.91	1.78	2.19	0.869

5. CONCLUSIONS

In this work CMOS implementation of D flip flop using LECTOR approach and VCLEARIT approach is presented. The average power consumption of all design is calculated at 1GHz clock frequency. Also the delay and average leakage power of each of the design is estimated. From the simulated results we can draw that the leakage power decreases when reduction techniques are applied. The percentage of leakage power reduction is more in VCLEARIT approach with slightly increase in the delay. LECTOR approach gives minimum leakage with minimum delay but consumes more power. Overall VCLEARIT and LECTOR approach can be consider for the design of CMOS D flip flop with lesser leakage power.

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