GLITCH ANALYSIS AND REDUCTION IN DIGITAL CIRCUITS

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ABSTRACT

Hazard in digital circuits is unnecessary transitions due to gate propagation delay in that circuit. Hazards occur due to uneven delay offered in the path of the various ongoing signals. One of the important reasons for power dissipation in CMOS circuits is the switching activity .This include activities such as spurious pulses, called glitches. Power optimization techniques that concentrate on the reduction of switching power dissipation of a given circuit are called glitch reduction techniques. In this paper, we analyse various Glitch reduction techniques such as Hazard filtering Technique, Balanced Path Technique, Multiple Threshold Technique and Gate Freezing Technique. We also measure the parameters such as noise and delay of the circuits on application of various techniques to check the reliability of different circuits in various situations.

KEYWORDS

Glitch, Power dissipation, Gate freezing, balanced path delay, multiple threshold transistor, Hazard filtering, Noise, Delay and switching activity
.

1. INTRODUCTION

Low Power Circuit Design has become very crucial in today's era of modern portable consumer gadgets. For CMOS combinational circuits, the reduction of dynamic power dissipation is very important. A signal transition can be of two types: a functional transition and glitch. Before reaching the steady state, a signal might go through several state changes which are called glitches. As they dissipate 20-70% of total power dissipation, glitch is needed to be eliminated for low power design.

$$P_{Total}=P_{Static}+P_{dynamic} \quad (1)$$

$$P_{Total}=P_{Switching}+P_{Short\text{-}Circuit}+P_{leakage} \quad (2)$$

Total Power dissipation consists of mainly dynamic power dissipation and static power dissipation, further these are divided into switching power dissipation, leakage power dissipation, short circuit power dissipation. Dynamic power dissipation is a major source of leakage power, which is directly proportional to the number of signal transitions(1-0 and 0-1) in a digital circuit. Switching power dissipation ($P_{switching}$) is directly proportional to switching activity(a),load capacitance(C_{load}), Voltage supply (V_{dd}) and clock frequency(f_{clk}) as shown in equation(3).

$$P_{switching} = a \cdot C_{load} \cdot V_{dd}^2 \cdot f_{clk} \quad (3)$$

In this paper we have chosen the best available techniques to reduce the glitch power. We have selected highly glitchfull circuits in our analysis and tried to reduce glitch power, delay and noise using these techniques. Using Tanner tool simulation, we have also put up the statistics to make the analysis simpler to understand.

2. TECHNIQUES FOR GLITCH REDUCTION

2.1 Gate Freezing

This method is useful for minimization of glitches. In this method, glitchfull and high power dissipating circuits are selected and replaced by a modified library cell called 'F-gate' with a control signal(CS) as shown in Fig.1 where Vdd is supply voltage ,I is input ,O is output CS is control signal to n-type library cell and Gnd is ground. This gate is controlled in order to freeze the cell's output for reducing the amount of glitch from the circuit. Basic CMOS gate and Gate freezed CMOS layout is shown in Figure1.The control signal(CS) drives the gate input of this n-type cell .This method transforms some of the gates that are more glitchfull into modified devices that are able to filter out unnecessary output transitions when a control signal(CS) is activated.

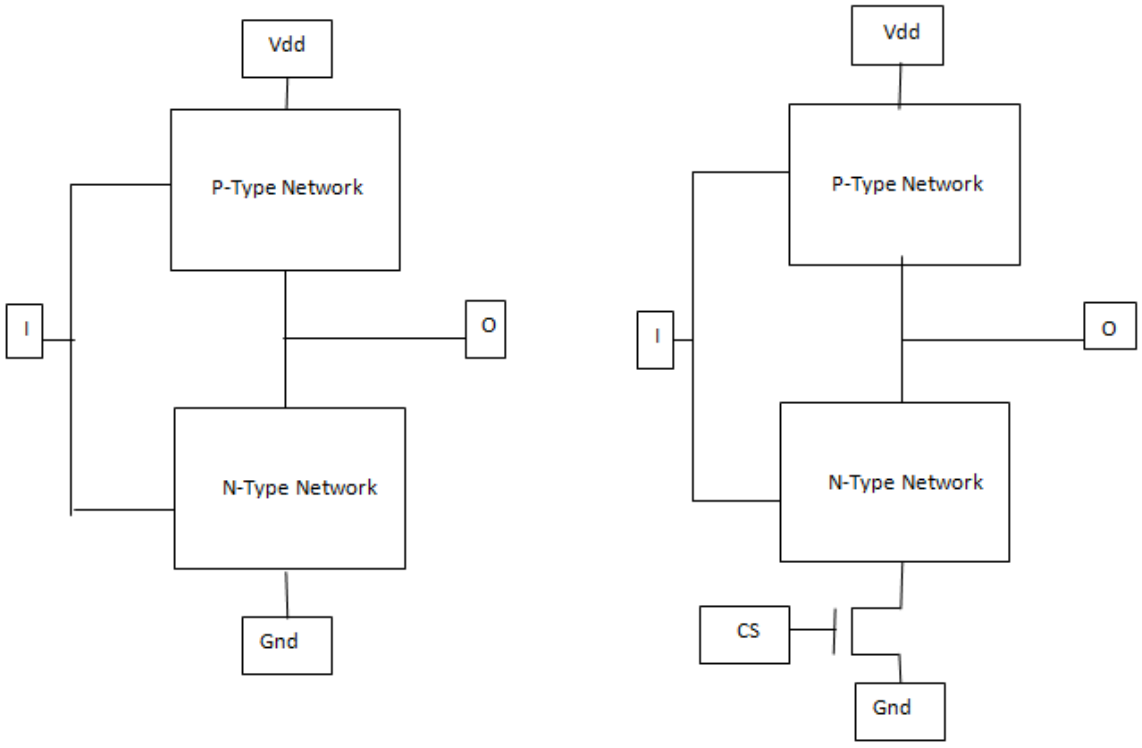

Figure 1 CMOS logic and CMOS logic with library cell

2.2 Balanced Path Technique

Balanced path delay technique is used for resolving differing path delays. To make path delays equal, buffer insertion is done on the faster paths. Balanced path delay will avoid glitches in the output. This technique is not considered efficient in terms of power consumption due to addition of buffers. Hence the more innovative method is hazard filtering discussed next.

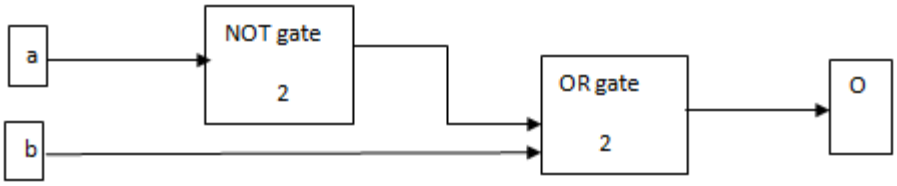

Figure 2 Original Circuit with glitch output

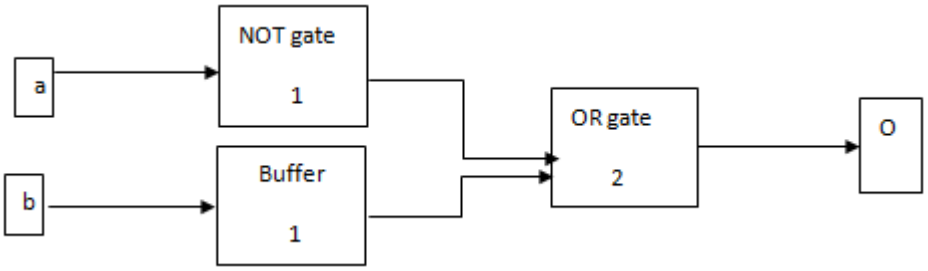

Figure 3 After applying balanced path delay technique

2.3 Hazard Filtering Technique

Hazard in digital circuits is unnecessary transitions as in case of glitch due to gate propagation delay in that circuit.

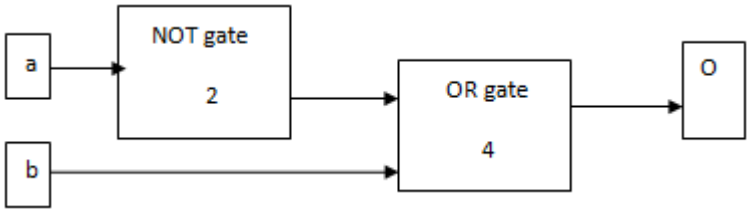

Figure 4 After applying hazard filtering technique

Hazards occur due to uneven delay offered in the path of the various ongoing signals. So apart from balanced path delay technique and using buffers to balance the delays in path ,we use the hazard filtering technique in which we increase the delay of receiving hardware to such an extent so that spurious transitions are eliminated and hence the glitch is eliminated. This is shown in the figure and also verified using simulation.

2.4 Multiple Threshold Technique

This is a technique to reduce power dissipation and reducing glitch in digital circuits. As delay of each gate is a function of threshold voltage(Vth), gates that are in non critical paths were selected

and their threshold voltages were rised manually, then the propagation delays along different paths can be balanced so that unnecessary transition will be minimized. Therefore, it is a new efficient technique for minimizing glitch in digital circuits that lead to low power dissipation.

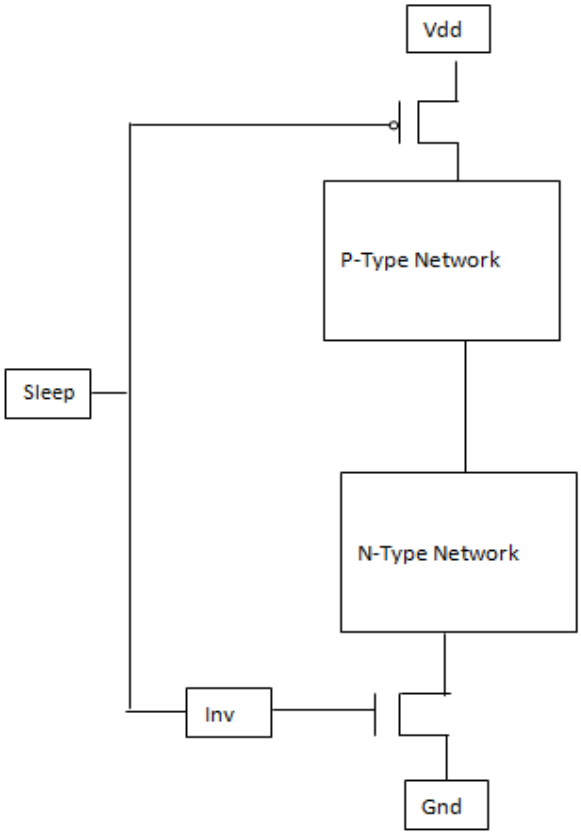

Figure 5 Multiple Threshold Implementation

3. SIMULATION AND RESULTS

We present the analysis of various parameters after applying various techniques on original glitchfull circuits.

Analysis of Circuit1(a'+b)

Name	Avg. Power V_1(watts)	Max.Power V_1(watts)	Delay(s)	Noise (Sq V/Hz)
Orignal Circuit	3.048279e-013	2.642508e-002	2.9497e-007	13.02006a
Hazard Filtering Technique	1.384576e-013	1.968104e-002	2.9513e-007	8.69371a
Balanced Path Delay Technique	4.538634e-013	6.502845e-002	2.9515e-007	4.36361a
Multiple Threshold	2.208378e-013	1.084178e-002	9.5208e-008	13.20418a
Gate Freezing	5.211884e-013	5.674504e-002	2.0005e-007	8.69361a

Analysis of Circuit 2 (AB'+BC)

Name	Avg. Power V_1(watts)	Max.Power V_1(watts)	Delay(s)	Noise (Sq V/Hz)
Orignal Circuit	5.786543e-013	5.488896e-002	2.9443e-007	4.41438a
Hazard Filtering Technique	8.379241e-013	1.790674e-001	2.9508e-007	4.41438a
Balanced Path Delay Technique	8.639895e-013	8.481847e-002	2.9511e-007	4.41438a
Multiple Threshold	3.182036e-013	5.595556e-002	2.9462e-007	4.41438a
Gate Freezing	5.191436e-013	5.683199e-002	2.9508e-007	8.86631a

Analysis of Circuit3 ((a'b)'c)'

Name	Avg. Power V_1(watts)	Max.Power V_1(watts)	Delay(s)	Noise(Sq V/Hz)
Orignal Circuit	2.425840e-013	3.211329e-002	1.9991e-007	4.36533a
Hazard Filtering Technique	1.192698e-013	1.766607e-002	1.9986e-007	17.28354a
Balanced Path Delay Technique	1.008878e-012	9.210829e-002	2.9510e-007	4.36537a
Multiple Threshold	3.604858e-014	8.604082e-003	1.9956e-007	30.15881a
Gate Freezing	1.024181e-013	1.775080e-002	1.9987e-007	17.28324a

3.1 Average Power Analysis:

Results show that Hazard Filtering Technique and Multiple Threshold Technique are better than other techniques where it is reduced upto 54.58% and 85.13% respectively. Also in multiple threshold technique the output voltage is reduced as compared to maximum voltage. So in this situation, we may prefer Hazard Filtering Technique to fulfill this criterion. The power consumption is highest for balanced path technique as expected.

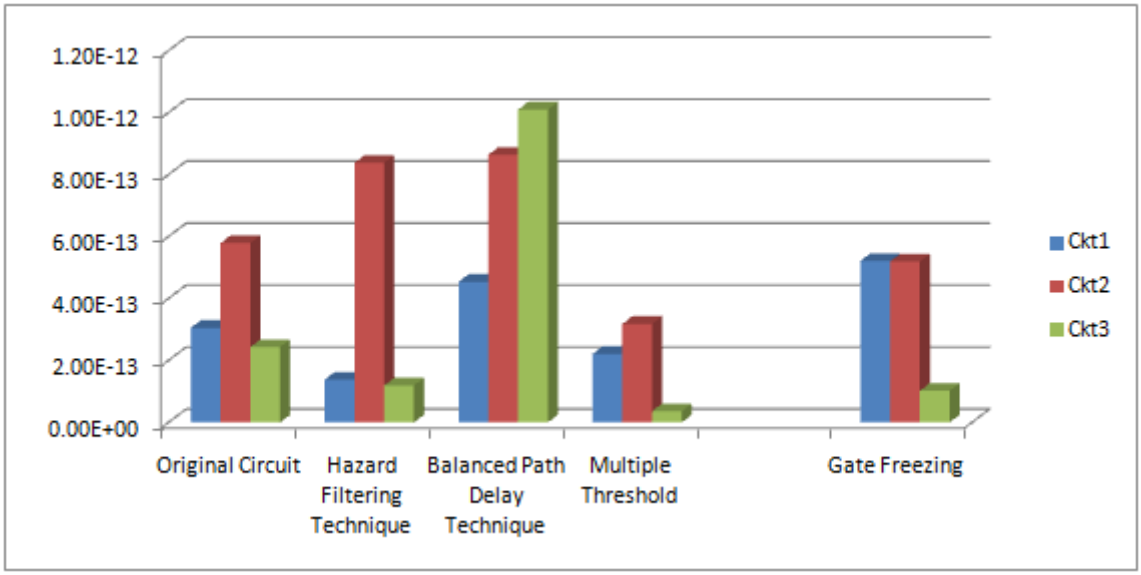

Figure 6 Circuit wise Average power consumption in watts

3.2 Max. Power Analysis

Similar to Average Power Analysis, we see that Maximum Power dissipation follows the same trend except for ckt2 Hazard filtering technique. Otherwise, Multiple threshold Technique and Hazard Filtering Techniques are advisable. The power consumption in balanced path technique as expected is higher.

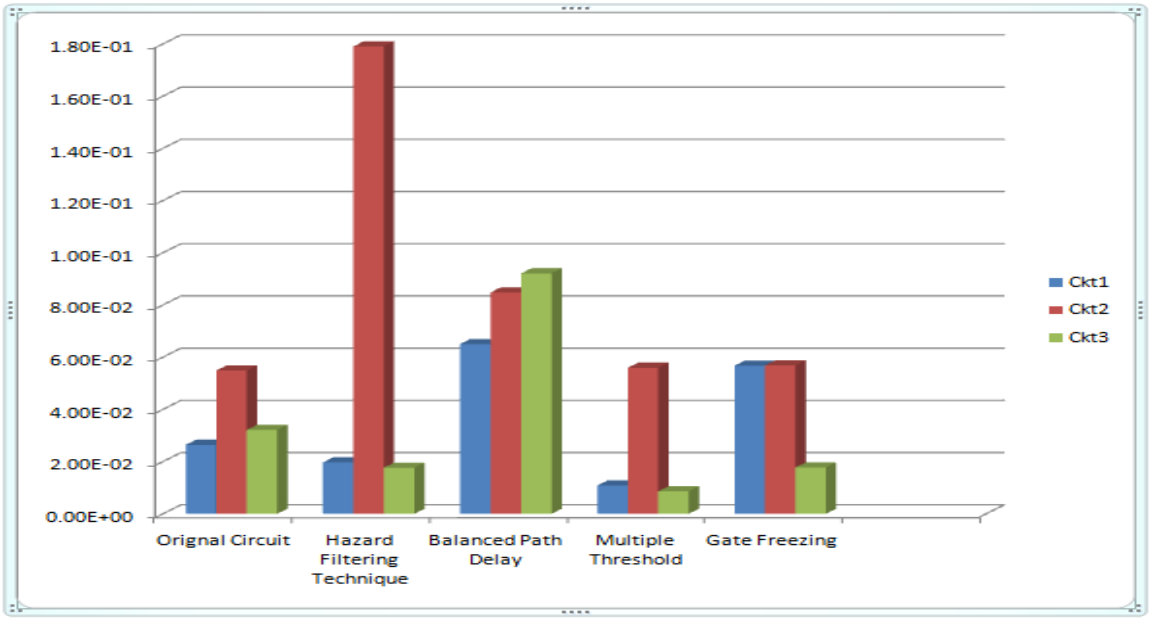

Figure 7 Circuit wise Maximum power consumption in watts

3.3 Delay Analysis

All techniques perform in similar manner for delay analysis of various circuits with a smaller lead to Gate Freezing upto 67.72% and Multiple Threshold Technique upto 32.18%. Hence these techniques may be used with proper analysis for reducing delay of the circuit.

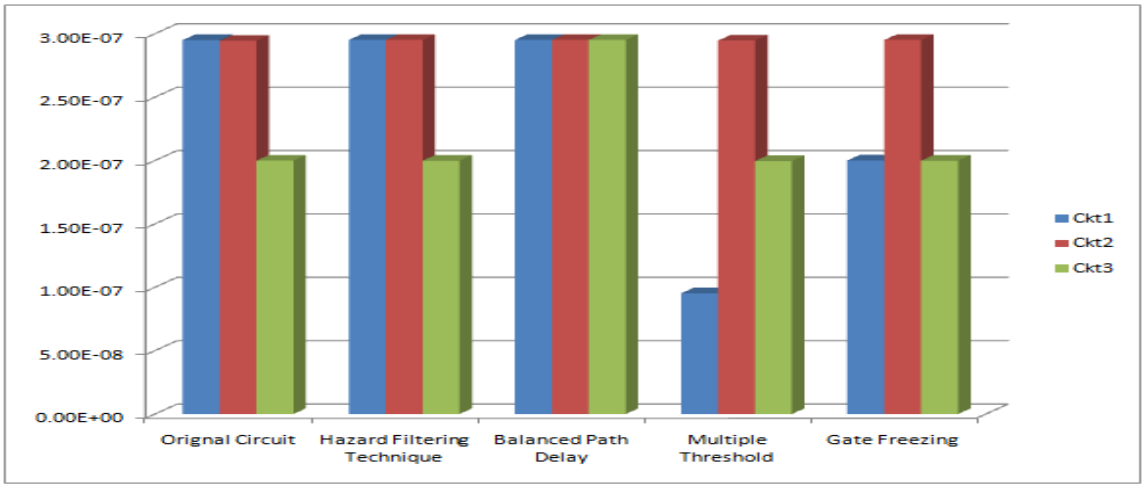

Figure 8 Circuit wise delay analysis in sec

3.4 Noise Analysis

As seen from the chart, balanced path technique is the best when analyzed for least noise in the output waveform upto 66.48%. The second best technique is the hazard filtering technique which also offers lesser noise in the output.

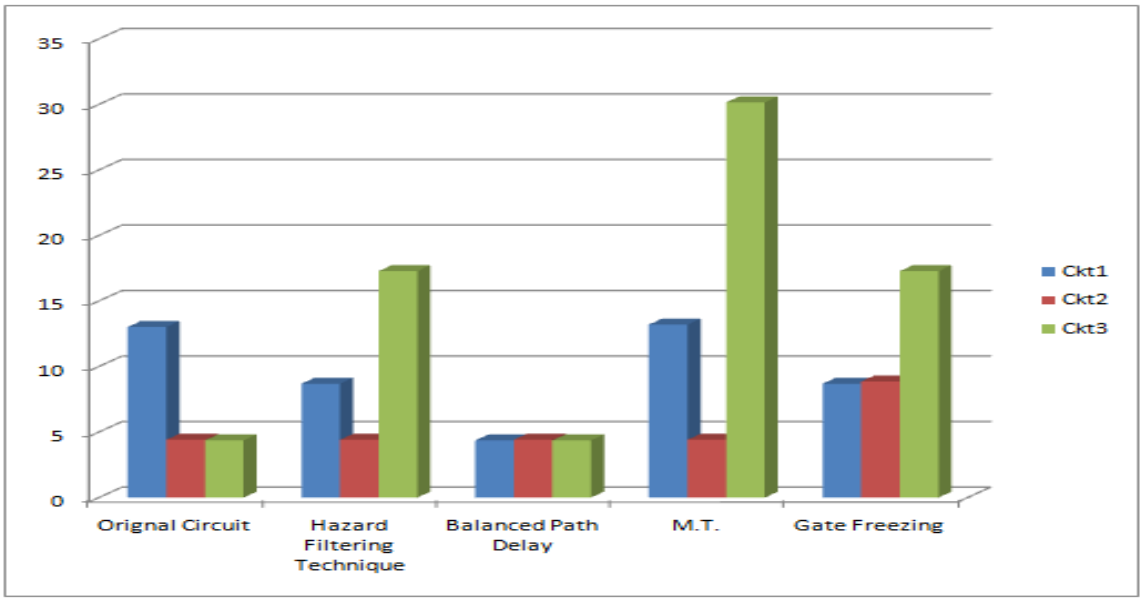

Figure 9 Circuit wise noise analysis (in Sq V/Hz)

4. CONCLUSION

In this paper, we try to reduce the glitch power in the circuits and analyze the various available techniques such as gate freezing, hazard filtering, balanced path delay and Multiple threshold technique for noise, delay and power using tanner tool. We ascertain the various techniques according to required specification in terms of these parameters. We show that Hazard Filtering Technique and Multiple Threshold Technique are better than other techniques to reduce power consumption in the circuit upto 54.58% and 85.13% respectively. To reduce delay and speed up the circuit, we can use Multiple Threshold Techniques where it is reduced upto 67.72%,Gate freezing technique is the second best approach to speed up the circuit upto 32.18%.Noise is best reduced in balanced path delay technique upto 66.48%. Hence we check and analyse the adaptability of various techniques for glitch reduction in various situations for its better application in real life problems.

ACKNOWLEDGMENT

This research was supported by National Institute of Science and Technology under summer undergraduate research fellowship.

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