500nW A LOW POWER SWITCHED CAPACITOR BASED ACTIVE LOW PASS FILTER FOR BIOMEDICAL APPLICATIONS

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ABSTRACT

This paper presents a low power, high gain, low area low pass filter design. The pre-processing block in this filter is the two-stage operational amplifier which is designed using the DTMOSFETS. This filter is operated at very low supply voltages of +0.2V.The PMOS input differential pairs are used to enhance the driving capability of the op-amp. input stage of the op-amp is the differential amplifier in which the inputs are provided to the two PMOS transistors. The second stage is the gain stage in which common source amplifier is used. The design parameter values are determined which optimize an objective feature satisfying specifications or constraints. The low pass filter is designed with a cut-off frequency of 100-HZ and a resistance of 10ohms, which occupies more layout area. In order to reduce the layout area the low pass filter is designed using the switched capacitor. The circuit is implemented with a supply voltage of 0.4V in 0.9-um technology, with a power consumption of 300nW and the simulations are performed using HSPICE simulator and layouts are designed using CUSTOM DESIGNER tool.

KEYWORDS

DTMOS, Switched-capacitor, Low pass filter.

1. INTRODUCTION

With rapid development of micro-electrons in the recent past years, more and more applications require an ultra-low amplitude signal measurement module, such as implantable devices in biomedical applications. Filters are the most important blocks in many biomedical devices. The design of low pass filter is presented in this paper. The op-amp is the most important pre-processing block in the filter. The op-amp designed using the CMOS transistors will operate supply voltage of 1V, which exhibits more power dissipation. To lower the power dissipation in the op-amp the voltages must be scaled down. Scaling down the voltages will lead to less threshold voltages, which increases the leakage current as reported in [1]. The other alternative to decrease the power dissipation at low supply voltages is to use the DTMOS technology[6][7]. The most interesting feature of the DTMOSFET is the dynamic variation of the threshold voltage of the MOSFET, which reduces the leakage power when the transistor is at off state. This method lowers the threshold voltage when the transistor is turned on and Increases the threshold voltage when the transistor is off. Thus, the method can reduce leakage current when the transistor is off.

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2. LOW POWER TWO-STAGE OPAMP DESIGN

The existing two-stage opamp is designed at a supply voltage of 1V, with a input swing of 0.5v to 0.8v. The gain obtained by the opamp using CMOS transistors is very low i.e. 22.5dB. To increase the gain of the opamp the voltage need to be reduced, which increases the leakage power and reduces the speed of the opamp. The CMOS two-stage opamp is as given below:

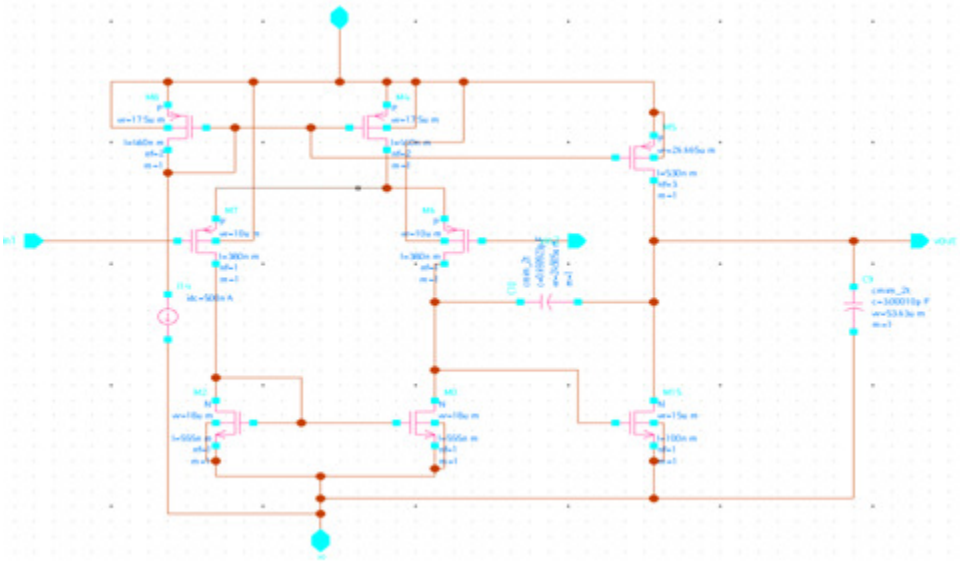

Figure:1 Two-stage opamp using CMOS

The W/L ratios used in the design of the opamp are as listed below:

Device	Type	W(um)	L(um)
M1&M2	P	10	0.378
M3&M4	N	18	0.556
M5&M8	P	35	0.460
M7	P	80	0.530
M6	N	15	0.100

3. LOW VOLTAGE DTMOS BASED OPAMP

In order to reduce the power the op-amp is designed at low supply voltages[8]. The proposed two-stage op-amp is designed with a supply voltage of $\pm$0.2v. The input stage of the op-amp is the differential amplifier stage, in which the PMOS transistors are used. The usage of PMOS at the input will improve the driving capability of the op-amp. The current mirror is used as the load in the differential amplifier. The second stage of the op-amp is the common source amplifier, which is driven by the output of the differential amplifier. The input stage transistors are replaced by the DTMOSFETs to achieve high gain at the low supply voltages. The design of the DTMOS based two-stage op-amp is as given below:

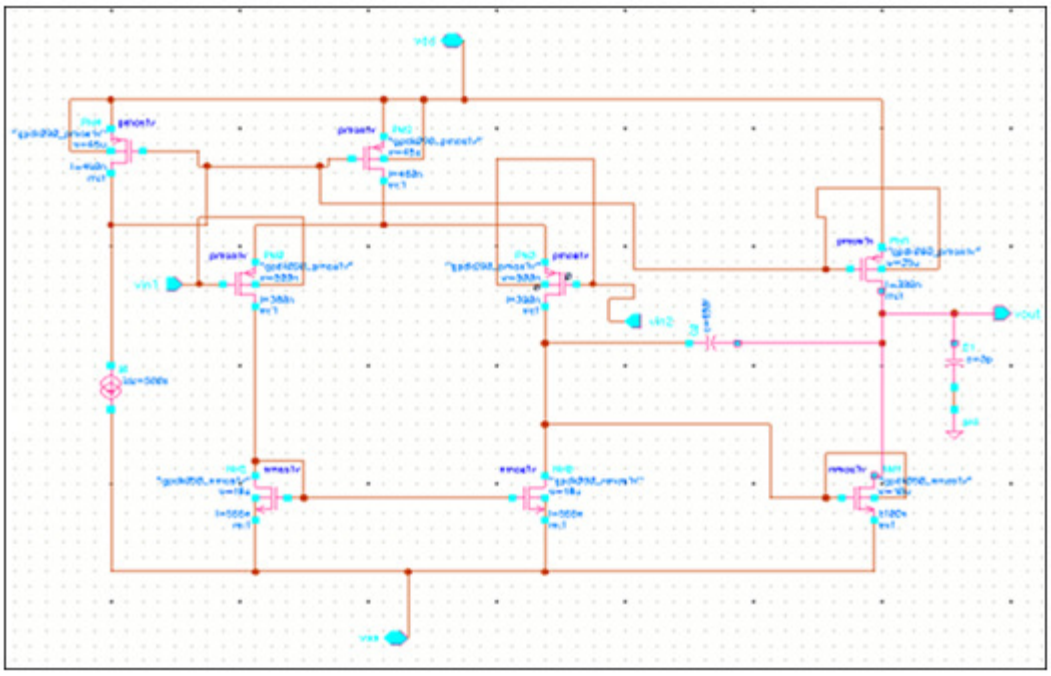

Figure: 2 Two-stage op-amp using DTMOS op-amp

This op-amp will operate at input common mode voltage range of 0.17v to 0.35v. The design parameter values are determined from the input specifications chosen as 0.5v/µs slew rate from which the current obtained as 500nW. The W/L ratios of the DTMOSFETs used in the design of two-stage op-amp are as listed below:

Device	**Type**	**W(um)**	**L(um)**
M1&M2	P	5	0.380
M3&M4	N	45	0.480
M5&M8	P	18	0.555
M7	P	10	0.380
M6	N	25	0.100

The gain obtained by the op-amp designed using the DTMOSFET is 42.5dB, which is very high compared to the op-amp designed using he CMOS transistors.

Comparison of CMOS op-amp with DTMOS op-amp:

The usage of DTMOS over the CMOS in op-amp design will improve the gain of the op-amp at low supply voltages. The following are the results obtained from the HSPICE simulator.

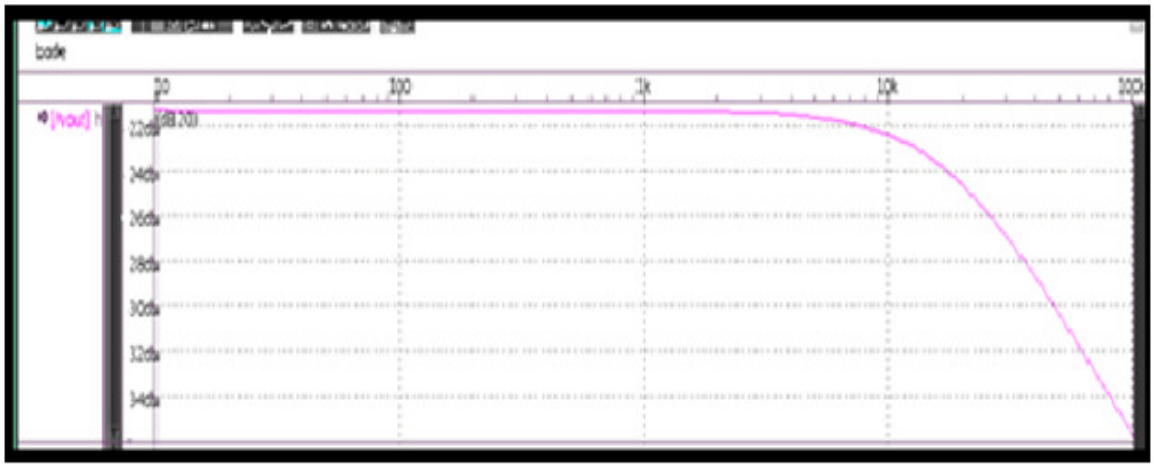

Figure: 3 Gain response of CMOS op-amp

The above is the gain response of the op-amp using the CMOS transistors in which the gain is obtained as 22.5dB. The gain response of the DTMOS op-amp is as plotted below:

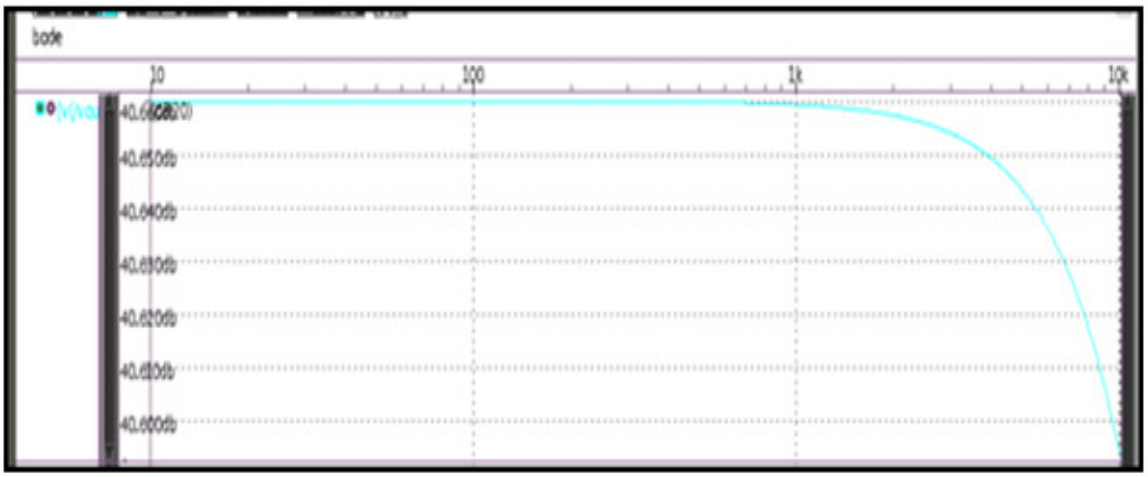

Figure: 4 Gain response of DTMOS op-amp

4. ACTIVE LOW PASS FILTER DESIGN

The low pass filter is designed using the DTMOS two-stage op-amp as the pre-processing block. The parameters required to design a low pass filter are the resistance and capacitance. The frequency of the low pass filter will depend on these parameters. The relation between the resistance, capacitance and frequency is given as below:

$$f = 1/2*\pi*R*C$$

The low pass filter is designed for biomedical applications. As the biomedical signal frequencies are low, here the cut-off frequency chosen to design the low pass filter is 100HZ. The R & C

values are calculated by the above relation based on the chosen cut-off frequency. The values of the parameters used in the low pass filter are as given below:

F = 100HZ
R = 100ohms
C = 890pf

The low pass filter is designed by using the DTMOS op-amp and the circuit diagram of the low pass filter using DTMOS op-amp along with resistor and a capacitor is as shown below:

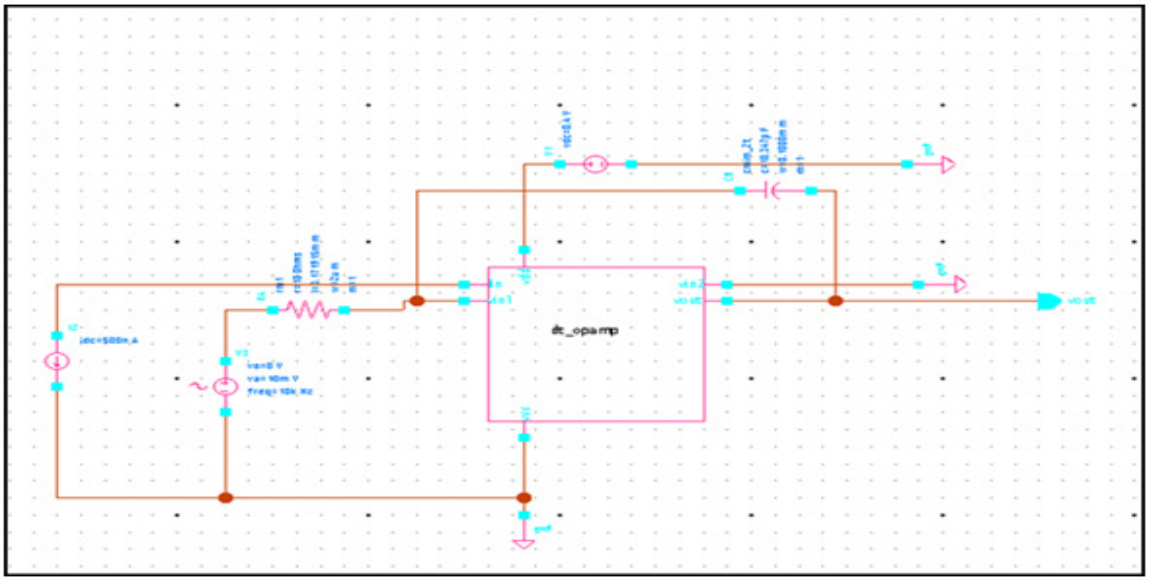

Figure: 5 Low pass filter without switched-capacitor

Designs of low pass filter using switched capacitor:

The low pass filter using the switched capacitor is designed in which the resistance in the filter is replaced by the switched capacitor. This filter is designed with the same specifications as the previous low pass filter which is designed with the resistor and capacitor. The switched capacitor is designed with two transistors and a capacitor, which provides the resistance of 10 ohms. This filter is designed in order to reduce the layout area of the filter which is designed with a resistor. Since the resistor occupies most of the design area, it is replaced by the switched capacitors which occupy less layout area.

The circuit diagram of the switched capacitor based low pass filter in which the resistor is replaced by the switched capacitor is as given below:

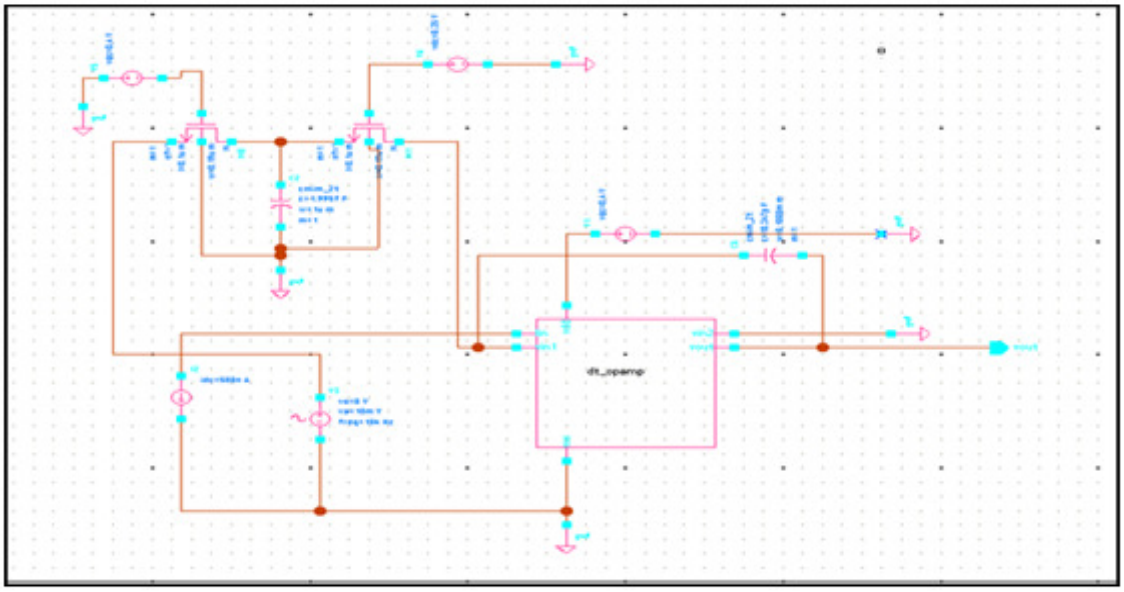

Figure: 6 Low pass filter using switched capacitor

The main advantage of switched capacitor based LPF over the low pass filer designed without switched capacitor is the reduction in the layout area.

5. RESULTS & ANALYSIS

The layouts have been designed for low pass filters with a resistor as well as for a low pass filter using switched capacitor. These layouts are designed in the CUSTOM DESIGNER tool. The below are the layouts of the LPF with and without switched capacitor:

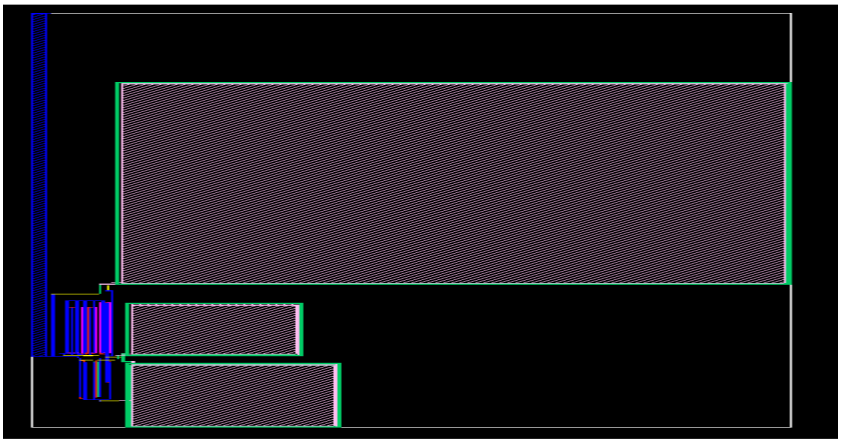

Figure: 7 Layout of the LPF without Switched-capacitor

The area obtained by the above LPF is the 23380um^2. The layout of the LPF with switched capacitor is as given below:

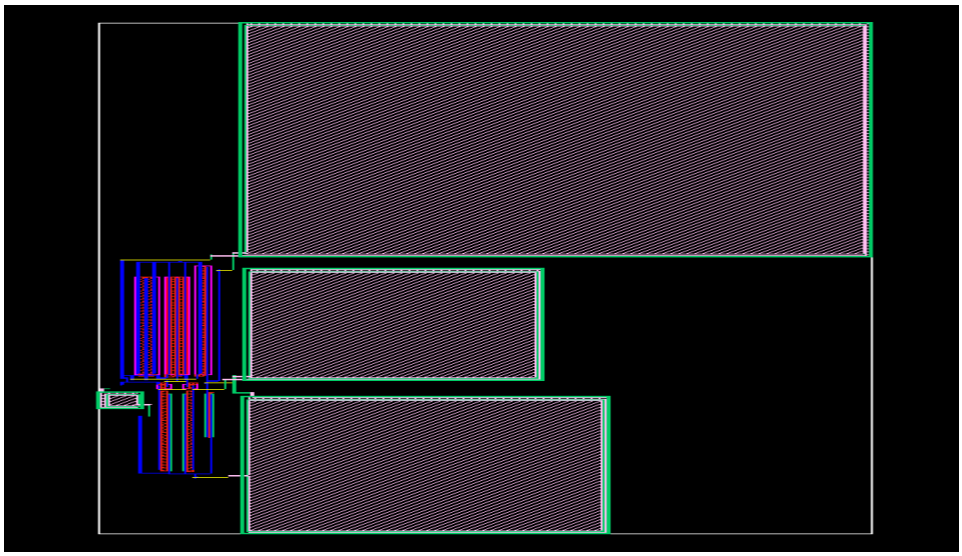

Figure: 7 Layout of the LPF with Switched-capacitor

The area obtained by the LPF with switched-capacitor is 7975um^2 which is very less compared to the layout area of the LPF without Switched-capacitor.

Comparison of various parameters results are as listed below:

Measured parameters	CMOS op-amp	DTMOS op-amp	LPF without SC	LPF with SC
Supply voltage	1V	0.4V	0.4V	0.4V
Gain	22.5db	40.5db	40.5db	40.5db
Power	600nW	300nW	300nW	320nW
Area	-	-	23380 um^2	7975 um^2

6. CONCLUSION

The Active switched-capacitor based low pass filter using Two-stage operational amplifier with low voltage and low power is designed. This two-stage amplifier with Miller compensation can be used in low power, low voltage High CMRR and PSRR applications such as Biomedical instruments and a small battery operated devices. The circuit has been designed in CUSTOM DESIGNER using 0.90um CMOS technology. We have described an ECG amplifier with a 300nW of power consumption, and good cardiac signal fidelity. The layouts have been designed and the areas have been compared. The Proposed two-stage operational amplifier with Miller compensation is well suited to biomedical systems such as cardiac pacemaker, electrocardiogram (ECG) where low-power consumption is of primary concern.

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