REDUCED COMPLEXITY QUASI-CYCLIC LDPC ENCODER FOR IEEE 802.11N

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ABSTRACT

In this paper, we present a low complexity Quasi-cyclic -low-density-parity-check (QC-LDPC) encoder hardware based on Richardson and Urbanke lower- triangular algorithm for IEEE 802.11n wireless LAN Standard for 648 block length and 1/2 code rate. The LDPC encoder hardware implementation works at 301.433MHz and it can process 12.12 Gbps throughput. We apply the concept of multiplication by constant matrices in GF(2) due to which hardware required is also optimized. Proposed architecture of QC-LDPC encoder will be compatible for high-speed applications. This hardwired architecture is less complex as it avoids conventionally used block memories and cyclic-shifters.

KEYWORDS

Quasi-cyclic -low-density-parity-check (QC-LDPC), WLAN (IEEE802.11n), Richardson and Urbanke lower- triangular algorithm, encoder

1. INTRODUCTION

In recent years, Low -density parity –check codes [1], which were first proposed by R. Gallager in the early 1960's and rediscovered by MacKay and Neal [2], have received a lot of attention due to their remarkable error correction capabilities near Shannon's limit with advancements in VLSI. Many current and next generation communications standards such as WLAN (IEEE802.11n), Mobile WiMAX (IEEE802.16e), DVB-Sand, 10GBaseT (IEEE802.3an) have adopted or considering the use of LDPC codes In spite of the better performance and lower decoding complexity of LDPC codes, the major drawback of LDPC codes is it's high encoding complexity. Low complexity of the encoder can be achieved by using structured LDPC codes. Many encoding algorithms were used in the past, it is suggested that the encoding complexity can be significantly reduced by using an approximate upper triangular parity check matrix to construct LDPC codes.

In this work, we have adopted structured LDPC codes known as the Quasi-cyclic Low-density parity check codes. Quasi-Cyclic has been proposed to reduce the complexity of LDPC while obtaining the similar performances. In QC-LDPC codes, the parity check matrix is a sparse

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matrix as it consists of less no of one's but the generator matrix is not a sparse matrix. Hence, most commonly lower-triangular matrix algorithm is used to simplify the encoding methods as suggested in Richardson and Urbanke method [4]. The encoder based on Richardson and Urbanke algorithm [3] which provides effective linear running time for some codes with a sparse parity-check matrix. The algorithm consists of two phases: preprocessing and encoding. To increase the encoding throughput, Parallel encoding and pipelining structures are applied. The encoding throughputs are determined by using encoding clock frequency and number of encoding iterations.

2. LOW-DENSITY PARITY CHECK CODES

LDPC codes are linear block codes that can be denoted as (n, k) or (n, wc, wr), where n is the length of the codeword, k is the length of the message bits, wc is the column weight (i.e. the number of nonzero elements in a column of the parity-check matrix), and wr is the row weight (i.e. the number of nonzero elements in a row of the parity-check matrix).

2.1. Characteristics for LDPC codes

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2.1.1. Parity-check

LDPC codes are represented by a parity-check matrix H, where H represents a binary matrix that, must satisfy Equation 1.

$$Hx^T = 0 \tag{1}$$

Where x is a codeword.

2.1.2. Low-density

H is a sparse matrix (i.e. the number of '1's is much lower than the number of '0's). It is the sparseness of H that guarantees the low computing complexity.

2.2. Representation of LDPC codes

Graphical representation of LDPC code is known as Tanner graph. Fig. 1. shows an example of (12, 6) LDPC code parity check matrix and its Tanner graph. Tanner graph consists of two sets of nodes, check nodes and variable nodes. Rows and columns of parity check matrix H can be mapped to check node units and variable node units. An edge between check node and the variable node is drawn only if there is '1' in the H matrix as in equation 2. The connected nodes represent that the mutual information can be transmitted between check nodes and variable nodes.

$$H = \begin{bmatrix} 1\,1\,0\,1\,0\,1\,1\,0\,0\,1\,0\,0 \\ 1\,1\,1\,1\,1\,0\,0\,0\,0\,0\,1\,0 \\ 0\,0\,0\,0\,0\,1\,1\,1\,0\,1\,1\,1 \\ 1\,0\,1\,0\,0\,0\,0\,1\,1\,0\,1\,1 \\ 0\,0\,1\,1\,1\,0\,1\,1\,1\,0\,0\,0 \\ 0\,1\,0\,0\,1\,1\,0\,0\,1\,1\,0\,1 \end{bmatrix} \quad (2)$$

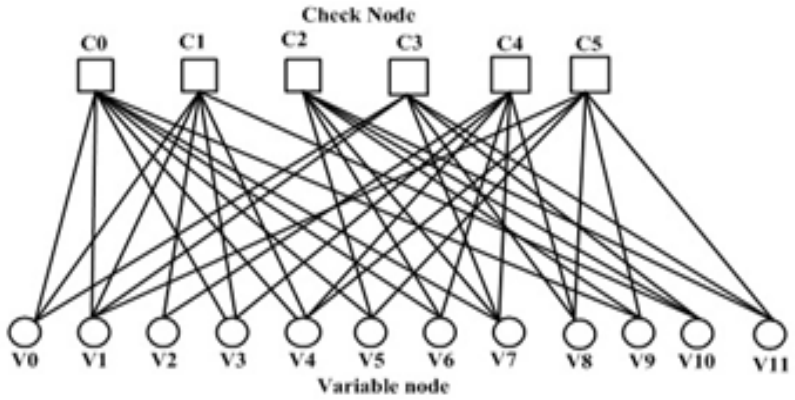

Figure 1 . Tanner graph representation of Parity Check matrix (12, 6)

2. QC-LDPC CODE CHECK CODES FOR IEEE 802. 11N STANDARD

Quasi-Cyclic LDPC (QC-LDPC) codes are structured LDPC codes come along with a more efficient implementation, while maintaining great performance. Quasi-cyclic codes are codes in which a cyclic shift of one codeword results in another codeword. Due to the cyclic structure, they require less memory as compared with the conventional LDPC codes. In addition, QC-LDPC codes also show the high-speed decoding because of the sparseness of its parity check matrix [5]. In all recent wireless communication standards, such as IEEE 802.11n, IEEE 802.11ac, and IEEE 802.16e, the QC-LDPC codes are used as an error correction code [6]-[8].All these wireless communication standards support a very high data rate over hundreds of Mbps. These standards also support various code rates and block lengths. QC-LDPC codes adopted by IEEE 802.11n/ac standards support four code rates, i.e., 1/2, 2/3, 3/4 and 5/6, and three block lengths, i.e., 648, 1296 and 1944 for a total of 12 possible codes as shown in Table 1.

Table 1. Twelve LDPC codes for IEEE 802.11n Standard

Codes	No of Columns (ρ)	No of Rows (γ)	Code rate (r)	Sub matrix size(z)	Codeword length(n)	Information Length(k)
1	24	12	1/2	27	648	324
2	24	12	1/2	54	1296	648
3	24	12	1/2	81	1944	972
4	24	8	2/3	27	648	432
5	24	8	2/3	54	1296	864
6	24	8	2/3	81	1944	1296
7	24	6	3/4	27	648	486
8	24	6	3/4	54	1296	972
9	24	6	3/4	81	1944	1458
10	24	4	5/6	27	648	540
11	24	4	5/6	54	1296	1080
12	24	4	5/6	81	1944	1620

In the IEEE 802.11 n wireless standard involves three sub-blocks (27, 54, and 81 bits) and four code rates (1/2, 2/3, 3/4, and 5/6). Each sub-block contains Z x Z sparse matrices. Before beginning the encoding process, the code check matrix must be expanded based on the sizes of sub-blocks [27]. According to all parameters expanded size of the matrix is given in Table 2.

Table 2. Expanded Matrix sizes corresponding to sub-block size

Code rate		1/2	2/3	3/4	5/6
Matrix size		12 x 24	8 x 24	6 x 24	4 x 24
Expanded Matrix size corresponding to sub block size	Sub-block 27	324 x 648	216 x 648	162 x 648	108 x 648
	Sub-block 54	648 x 1296	432 x 1296	324 x 1296	216 x 1296
	Sub-block 81	972 x 1944	648 x 1944	486 x1944	324 x 1944

Fig. 2 represents the parity check matrix for code length 648 and code rate 1/2 . Each entry in the square represents a 27 by 27 square matrix, where 0 represents the identity matrix and the dash, '-', indicates a cyclic shift to the right of the identity matrix by a number of places equal to the entry given in a box.

0	-	-	-	0	0	-	-	0	-	-	0	1	0	-	-	-	-	-	-	-	-	-
22	0	-	-	17	-	0	0	12	-	-	-	-	0	0	-	-	-	-	-	-	-	-
6	-	0	-	10	-	-	-	24	-	0	-	-	-	0	0	-	-	-	-	-	-	-
2	-	-	0	20	-	-	-	25	0	-	-	-	-	-	0	0	-	-	-	-	-	-
23	-	-	-	3	-	-	-	0	-	9	11	-	-	-	-	0	0	-	-	-	-	-
24	-	23	1	17	-	3	-	10	-	-	-	-	-	-	-	-	0	0	-	-	-	-
25	-	-	-	8	-	-	-	7	18	-	-	0	-	-	-	-	-	0	0	-	-	-
13	24	-	-	0	-	8	-	6	-	-	-	-	-	-	-	-	-	-	0	0	-	-
7	20	-	16	22	10	-	-	23	-	-	-	-	-	-	-	-	-	-	-	0	0	-
11	-	-	-	19	-	-	-	13	-	3	17	-	-	-	-	-	-	-	-	-	0	0
25	-	8	-	13	18	-14	9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
3	-	-	-	16	-	-	2	25	5	-	-	1	-	-	-	-	-	-	-	-	-	0

Figure 2. Basic Matrix for IEEE 802.11n for the rate ½ and codeword length 648

LDPC encoder can be designed using the lower triangular matrix approximation, where the parity check matrix is converted into a lower triangular form by row and column permutations without changing its linearity [3]. To convert into a lower triangular form, the parity check matrix has been divided into sub matrices A, B, C, D, T, E has a certain order as shown in equation 3. The encoding complexity is O (n+g2), g is the row of matrix E. Figure 3 shows a standard lower triangular form of Parity Check Matrix obtained by performing certain column switching operations.

$$H = \begin{bmatrix} A_{(m-g)*(n-m)} & B_{(m-g)*(g)} & T_{(m-g)*(m-g)} \\ C_{g*(n-m)} & D_{g*g} & E_{g*(m-n)} \end{bmatrix} \quad (3)$$

Where A is (m-g)*(n-m), B is (m-g)* g , C is g *(n-m), D is g * g, E is g * (m-g) , T is (m-)*(m-g), T is a proposed lower triangular matrix.

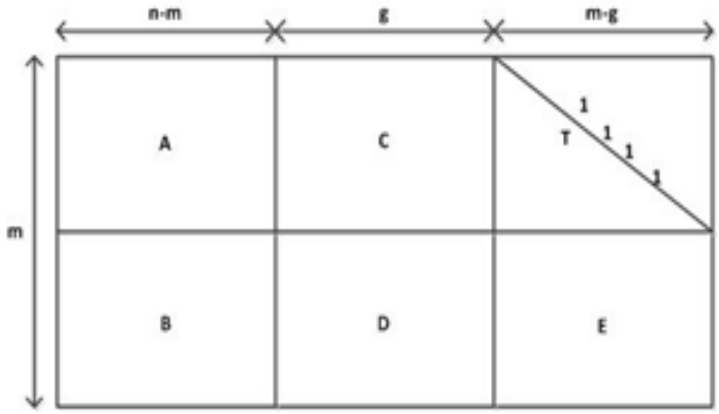

Figure 3. Lower Triangular Form of Parity Check Matrix

3.1 Richardson - Urbanke Encoding Method [3]

3.1.1. Pre-processing Step

Input : Non Singular Parity Check Matrix 'H'

Output: To obtain an equivalent parity check matrix of the form such that $-ET^{-1}B + D$ is non singular.

Step 1: By performing row and column permutation to bring the parity-check matrix H into an appropriate lower triangular form such as

$$\mathbf{H} = \begin{bmatrix} \mathbf{A} & \mathbf{B} & \mathbf{T} \\ \mathbf{C} & \mathbf{D} & \mathbf{E} \end{bmatrix}$$ with a small gap g.

Step 2: Use of Gaussian Elimination to perform Pre- Multiplication.

$$\begin{bmatrix} I & 0 \\ -ET^{-1} & I \end{bmatrix} \begin{bmatrix} A & B & T \\ C & D & E \end{bmatrix} = \begin{bmatrix} A & B & T \\ -ET^{-1}A + C & -ET^{-1}B + D & 0 \end{bmatrix} \quad (4)$$

To check whether $-ET^{-1}B + D$ is non singular . If necessary further column permutation can be used to achieve this property.

3.1.2. Encoding Step

Input: Parity-check matrix of the form $H = \begin{bmatrix} A & B & T \\ C & D & E \end{bmatrix}$ such that $-ET^{-1}B + D$ is non singular.

Output: The vector x=(s, p_1, p_2) such that $H x^T = 0$

$$\begin{bmatrix} A & B & T \\ -ET^{-1}A + C & -ET^{-1}B + D & 0 \end{bmatrix} \begin{bmatrix} s \\ p1 \\ p2 \end{bmatrix} = 0 \quad (5)$$

Solving equation 5 we get following two equations

$$As^T + Bp1^T + Tp2^T \quad (6)$$

$$\left(-ET^{-1}A + C\right)s^T + (-ET^{-1}B + D)\,p_1^T = 0 \quad (7)$$

Let $\phi = -ET^{-1}B + D$ which is non singular. From equation 6 and7, we get

$$p_1^T = -\phi^{-1}(-ET^{-1}A + C)s^T \quad (8)$$

$$p_2^T = -T^{-1}(As^T + Bp_1^T) \quad (9)$$

The encoding process flow chart is shown Fig.4. The area complexity in the encoding process of LDPC codes is described in Table 3 [3].

Table 3. p1 and p2 computational complexity

p1 Complexity		
Operation	**Requirements**	**Complexity**
As^T	(m-g) * (n-m) sparse multiplication	O(n)
$T^{-1}[As^T]$	(m-g) * (m-g) back subtraction	O(n)
$-ET^{-1}[As^T]$	(g) * (m-g) sparse multiplication	O(n)
Cs^T	(n-m) *(g) sparse multiplication	O(n)
$-ET^{-1}[As^T]+Cs^T$	(n-m) bit addition	O(n)
$-\phi^{-1}[-ET^{-1}[As^T]+Cs^T]$	(g) * (g) dense multiplication	$O(g^2)$
p2 Complexity		
Operation	**Requirements**	**Complexity**
As^T	(m-g) * (n-m) sparse multiplication	O(n)
Bp_1^T	(m-g)*x (g) sparse multiplication	O(n)
$As^T + Bp_1^T$	(m-g) bit addition	O(n)
$-T^{-1}[As^T + Bp_1^T]$	(m-g) * (m-g) back subtraction	O(n)

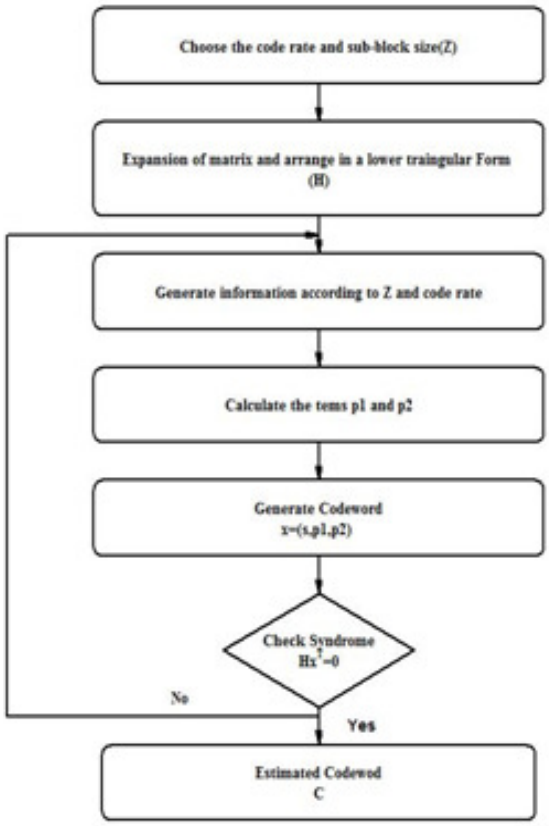

Figure 4, Flow chart of Encoding Process

The inverse of the matrix in the equation of p_1^T is not a sparse matrix, thus the computational complexity of the encoder is high. The LDPC decoder operates in linear time, hence it may be difficult to perform low-complexity encoding of these codes [11]. *S. Myung et al.* , in their paper proposed an encoding algorithm for LDPC codes with linearly scaled complexity, based on the principal to choose the matrix φ as the identity matrix or a circulant permutation matrix [26].The encoding procedure of Block-LDPCs is simplified and summarized in equation 10-14 as follows[5].

Simplified Encoding Steps :

Step1: Calculate $As^T \text{ and } Cs^T$ (10)

Step2: Calculate $ET^{-1}As^T$ (11)

Step3: Calculate $p_1^T = ET^{-1}As^T + Cs^T$ (12)

Step4: Calculate $Tp_2^{\ T} = As^T + Bp_1^{\ T}$ (13)

Step5: Calculate Codeword $x = [s, p_1^{\ T}, p_2^{\ T}]$ (14)

Where s are message bits and p_1,p_2 are parity bits.

4. LOW-DENSITY PARITY CHECK CODES ENCODER ARCHITECTURE

In this section we describe a hard-wired methodology for implementing QC-LDPC encoder architecture based on Richardson - Urbanke encoding method for the IEEE 802.11n standard with 1/2 code rate, 648 coward length and sub-block size z =27. In many QC LDPC encoder designs hard-wired in the LUTs, cycles-shifters and block-memories conventionally are used. In the present work, all these are eliminated, which result in the hardware optimization and high throughput [10]. This work focuses on the reduction of hardware multiplication by constant binary matrices. Fig.5 describes an architecture of the QC-LDPC encoder for the IEEE 802.11n standard (Rate = 1/2 and sub-block size z =27).

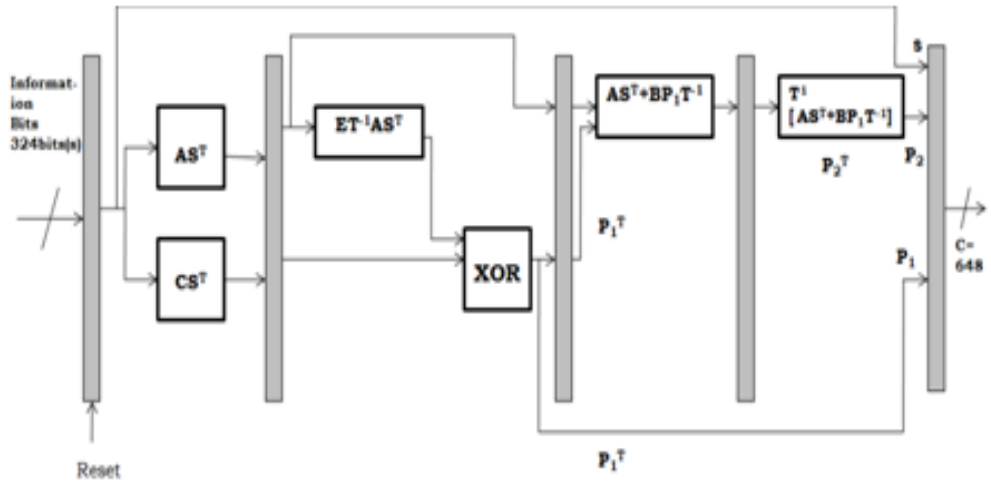

Figure 5. Architecture of the QC-LDPC encoder for the IEEE 802.11n standard (Rate = 1/2 and sub-block size z =27)

In the above architecture the arithmetic operations of the binary LDPC codes are in GF (2) (i.e.modulo-2 addition). Hence XOR operators are used for all the generated blocks in the given architecture. Number of LUTS required for implementation of each block is not fixed. The proposed architecture shows that there is no need of block memories and there is a usable of a smaller number of gate results in a low complexity hardware.

5. RESULTS AND DISCUSSION

Most of the wireless communication standards described their parity-check matrix (PCM) in quasi-cyclic low-density parity-check (QC-LDPC) form. A Block-structured PCM for IEEE802.11, N =648 bits, and R = ½ is constructed using an identity sub-matrix which is rotated or shifted by an amount specified by a shift matrix is shown in Fig.6.

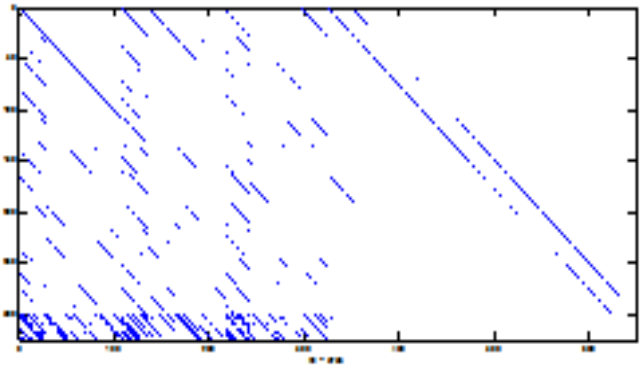

Figure 6. An IEEE 802.11n rate ½, 648 code length QC-LDPC parity check matrix

The proposed encoder architectures have been implemented in hardware for IEEE 802.11 QC-LDPC defined by the parity- check matrix given by the standard for codeword length n = 648 bits, rate1/2 and block size z = 27.Table IV lists the corresponding occupied area in the Xilinx Virtex-5 FPGA device xc5vlx110t-1ff1136. The proposed rate QC-LDPC encoder can support up to 12.12 Gbps throughput at 301.433MHz clock frequency.

Table 4: Resource consumption of proposed encoder in Xilinx Virtex-5 FPGA

Resource	Number	Usage Rate
Number of slice registers	2906	4%
Number of slice LUTs	1335	1%
Number of Fully used LUT-FF Pairs	1164	37%
Number of bonded IOBs	64	10%
Number of BUFG/BUFGCTRLs	1	3%

Table 5. lists Comparison of the existing LDPC encoder for wireless IEEE 802.11n with proposed architecture. The comparison shows that as we avoid cyclic shifters, block memories that are used in conventional encoders and apply hardwired method leads to high encoding speed, significantly higher throughput. As far no barrel shifters are used proposed architecture is less complex and area efficient

Encoders in the literature survey are implemented using different technologies and FPGA devices. These are applied for different codes and applications. Hence complexity and performance are not directly comparable. Table VI summarizes Comparison of proposed LDPC encoders with reported works stating several encoding parameters. Aaron E. Cohen, Keshab K. Parhi design encoders for a 10-Gigabit Ethernet transceiver which is compliant with the IEEE 802.3an standard using Hybrid (G -Matrix method and RU) method. They apply hybrid method on the RS (2048, 1723) LDPC codes.A new Hybrid LDPC encoder is compared with existing known methods G matrix multiplication and the RU method in terms of area, critical path, and power consumption[9]. Zhuo Ma et al. proposes a bidirectional recursion arithmetic method a

quasi-parallel LDPC encoder code in IEEE 802.16e. This method reduces the encoding complexity and improves the coding efficiency. The encoder design for half rate LDPC code with code length 2304 can work at 50MHz[12]. Zhibin Zeng applies LU decomposition with dynamic programming for LDPC encoder for CMMB. For the 1/2 code rate, encoder work at.

Table 5. Comparison of LDPC encoder for wireless IEEE 802.11n.

Work	Code rate	Code word length	FFs	XOR Gates	Barrel shifter	2nd-stage cyclic shifter	Clock cycles	Block-memories	Target device	Frequency
[16]	1/2	1296	1701	1620	20	-	24	√	Spartan-3	-
[17]	1/2	1296	162	243	1	-	73-83	√	Spartan-3	-
[18]	5/6	1944	1053	1053	1	11	24	√	-	-
[5]	5/6	1944	2187	-	-	-	4	X	Virtex5	290MHZ
[21]	1/2	648	-	-	22	-	21	√	ASIC	100MHz
Proposed	1/2	648	1164	-	-	-	4	X	Virtex-5	301.433MHz

maximum frequency 200 MHz, system pure encoding achieves 54 Mbps throughput and 86 Mbps for 3/4 code rate [13]. Ale Aldin AL Hariri, Fabrice Monteiro et.al. design LDPC encoder for a length of 64800 bits and the code rate of 5/6 were used for DVBS2, whereas for DVB-T2 block length of 16200 bits and code rate of 7/9 [14]. They also proposed Configurable and High-throughput Architectures for Quasi-Cyclic Low-Density Parity-Check encoder for the WiMAX (IEEE 802.16e) and the WiFi (IEEE 802.1 In) protocols. Throughput up to 32 Gbits/s have been achieved for the encoder [22]. Silvia Anggraeni et al.use bit-wise matrix-vector Multiplication method for proposed encoder applied to IEEE 802.16e. The architecture works in terms of information throughput ranging from 0.235 to 8.83 times higher than other works [15]. Sunitha Kopparthi and Don M. Gruenbacher design LDPC encoder for IEEE 802.16e standard. The encoder design presented has a significantly high throughput of 422 Mbps.[19]. Hemesh Yasotharan et.al present encoder that simplifies the calculations found in other flexible encoders results in increasing memory usage also parallelization and faster encoding .The encoder had a throughput between 115Mbps and 360Mbps depending upon the code rate and block length[20]

Table 6. Comparison of proposed LDPC encoders with Existing works

Work	Parity check matrix structure		Type of Architecture			Application standard	Encoding Algorithm	Code length	Code rate	Frequency	Throughput	Technology
	QC/struct	Non-struct	Serial	Partial Parallel	Fully-Parallel							
[9]	√				√	IEEE 802.3an (10GBase-T ethernet)	hybrid encoding/ G matrix multiplication method.	2048 - 1723	-	-	High(Gbps)	Xilinx Virtex 4 (xc4v1x25-12sf363
[12]	√				√	IEEE 802.16e	bidirectional recursion encoding	2304	1/2		50 Mb/s.	Xilinx's XC3S1000
[13]	√				√	CMMB	LU decomposition	4608,	1/2-3/4	200 MHz	54 - 86 Mbps	Altera Stratix II EP1S180F1020 14
[14]	√			√		DVB-T2	F.Sub	64800-16200	5/6-7/9	328Mhz	28.9 Gbps	Altera Stratix EP3SE50F484 C2 device
[15]	√				√	IEEE 802.16e	Bit-wise matrix-vector multiplication	576	1/2	154.63Mhz	4.948 Gbps	Altera Stratix EP1S80F1508 C5
[19]	√				√	IEEE 802.16e	F.Sub.(dual H2)	576-2304	1/2, 2/3, 3/4 5/6	422.12 MHz.	400 Mbps	Altera Stratix
[20]	√				√	IEEE 802.16e	generator matrix	2304 bits	1/2	60 MHz	119 Mbpss	Xilinx Virtex-II XCV4000-6 FPGA
[21]	√				√	IEEE 802.11n	Linear Encoding	648, 1296, 1944	1/2, 2/3, 3/4, 5/6	100 MHz	7.7 Gbps	ASIC
[22]	√				√	(IEEE 802.16e	Linear Encoding	1152, 2304	1/2	112Mzs	32832 Mbps	Altera Stratix III device (EP3SE50F780 C2).
[23]	√				√	DVB-S2	F.Sub	360		100MHz	10 Gbps	Xilinx Vertex5-LX155T
[24]		√			√	CMMB	RU		1/2 and 3/4)	200.23 MHz	34 Mbps and 69 Mbps	Altera Stratix II EP1S180F1020 14
[25]	√		√			CMMB	LU decomposition	9219 -	1/2-3/4	200MHz	32-67 Mbps	*Altera Stratix II EP2S90*
Proposed	√				√	IEEE 802.11n	RU	648	1/2	301.433MHz	12.12 Gbps	Xilinx Virtex-5 xc5vlx110t-1ff1136

Yong-Min Jung et al. proposes a high-throughput encoder architecture for quasi-cyclic low-density parity-check codes in IEEE 802.11ac standard. It is implemented with 130-nm CMOS technology for LDPC (1944, 1620) irregular code which achieved 7.7 Gbps throughput at 100 MHz clock frequency[21]. InKi Lee et al. propose high-speed LDPC Encoder Architecture for Digital Video Broadcasting Systems. They used an efficient encoding method for DVB-S2 LDPC codes which is done without reference to the code generation matrices. This architecture results in maximum throughput is up to 10 Gbps with a 100 MHz clock[23].

Xiangran Sun, Zhibin Zeng, Zhanxin Yang design Low Complexity LDPC Encoder use Optimized RU Algorithm With Backtracking for CMMB. This encoder work at the maximum frequency is 200.23 MHz achieve throughputs up to 34.12 Mbps for 1/2 code rate and 69.23 Mbps for 3/4 code rate [24]. Wang Peng, Chen Yong-en have proposed low-complexity real-time LDPC encoder design for CMMB based on the LU decomposition method. It shows Maximum frequency achieved is 200 MHz. Throughput ranges from 32.44 Mbps for (1/2 code rate) and 67.16 Mbps for 3/4 code rate [25]. It is shown that the proposed architectures compare favourably to the other works in the sense of flexibility and complexity. The proposed architecture focuses Low complexity and high throughput for IEEE 802.11n standard.

6. CONCLUSIONS

We have described RU encoding methodology for QC-LDPC codes for IEEE 802.11n standard with 1/2 code rate, 648 codeword length, and sub-block size z =27. The proposed encoder is found to be low complexity compared to previous encoder designs and allow efficient parallelism, flexibility, and high throughput rate. The hard-wire based encoder leads to high encoding speed and less resources utilization due to elimination cyclic shifters and block memories and utilization of multiplication by the constant binary matrix method. The proposed QC-LDPC encoder can support up to 12.12 Gbps throughput at 301.433MHz clock frequency.

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REFERENCES

[1] R. G. Gallager,(1962)"Low-density parity check codes.', IRE Transaction Info.Theory, Vol.8,No.1, pp 21–28.

[2] D. J. C. MacKay and R. M. Neal, (1996) "Near Shannon Limit Performance of Low Density Parity-Check Codes," Electronics Letters, Vol. 32 No. 18, pp. 1645–1646.

[3] Thomas J. Richardson and Rudiger L. Urbanke,(2001) "Efficient encoding of low-density parity-check codes.", IEEE Transactions on Information Theory, Vol 47 No 2,pp. 638–656.

[4] Huxing Zhang, HongyangYu,"Multi-rate QC-LDPC Encoder.", IEEE Circuits and Systems International Conference on Testing and Diagnosis , 2009, pp 1-4.

[5] Georgios Tzimpragos,Christoforos Kachris and Dimitrios Soudries "A low-complexity implementation of QC-LDPC encoder in reconfigurable logic.", International Conference on Field programmable Logic and Applications.; ,2013, pp 1-4.

[6] IEEE P802.11n/TM-2009, IEEE Standard for Information Technology Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications. 2001.

[7] IEEE 802.11acTM/D2.0., Draft Standard for Information Technology Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications, Amendment 4: Enhancements for Very High Throughput for Operation in Bands below 6GHz. 2013.

[8] IEEE Std 802.16eTM-2005, IEEE Standard for Local and metropolitan area networks Part 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems.2006.

[9] AE Cohen, KK Parhi.., (2009)" A Low-Complexity Hybrid LDPC Code Encoder for IEEE 802.3an (10GBase-T) Ethernet"., IEEE TRANSACTIONS ON SIGNAL PROCESSING.,Vol.57,No.10,pp 4085 - 4094 .

[10] Georgios Tzimpragos,Christoforos Kachris and Dimitrios Soudries ,"Automatic Implementation of Low-Complexity QC-LDPC Encoders.", Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS),Sept. 2013,pp 243 - 246 .

[11] Ahmad Mahdi , Nikos Kanistras and Vassilis Paliouras ," An encoding scheme and encoder architecture for rate-compatible QCLDPC codes." IEEE Workshop on Signal Processing Systems (SiPS), Oct.2011,pp 328–333.

[12] Zhuo Ma,Ying L and Xinmie Wang , "A Quasi-Parallel Encoder of Quasi-Cyclic LDPC Codes in IEEE 802.16e." International Conference on Information Science and Engineering ,Dec 2009,pp-2492 - 2495 .

[13] Zhibin Zeng ,"A High-efficiency LDPC Encoder for CMMB with Dynamic Programming. ",. International Conference on Intelligent Computation Technology and Automation (ICICTA). ,Mar 2011,pp 337– 340.

[14] Alaa Aldin Al Hariri, Fabrice Monteiro and Loic Sieler.,"A High Throughput Configurable Parallel Encoder Architecture for Quasi-Cyclic Low-Density Parity-Check Codes." IEEE 19th International On-Line Testing Symposium (IOLTS)., July 2013; pp163-166

[15] Silvia Anggraeni; Fawnizu Azmadi Hussin; Varun Jeoti,"High Throughput Architecture for Low Density Parity Check (LDPC) Encoder.", IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) ., Aug 2013;pp- 948 – 951.

[16] Z. Cai, J. Hao, P.H. Tan, S. Sun and P.S. Chin, (2006.),"Efficient encoding of IEEE 802.11n LDPC."; Electronics Letter.,Vol. 42 No. 25 ,pp 1471–1472.

[17] J.M. Perez, V. Fernandez, (2008) ,"Low-cost encoding of IEEE 802.11n.", Electronics Letter., Vol. 44, No. 4, pp 307–308.

[18] Y. Jung., J. Kim ,(2010),"Memory-efficient and high-speed LDPC Encoder.", Electronics Letter. , Vol. 46, No. 14 ,pp 1035-36.

[19] Sunitha Kopparthi , Don M. Gruenbacher," Implementation of a flexible encoder for structured low-density parity-check codes", IEEE Pacific Rim Conf. Commun., Comput. Signal Process. Aug 2007; pp-438–441.

[20] Hemesh Yasotharan, Anthony Chan Carusone,"A flexible hardware encoder for systematic low-density parity-check codes," IEEE Internatinal Midwest Symposium on Circuits System. (MWSCAS'09). ,Aug 2009; pp 54–57.

[21] Yong-Min Jung , Chul-Ho Chung , Yun-Ho Jung , and Jae-Seok Kim . , (2014) '7.7 Gbps Encoder Design for IEEE 802.11ac QC-LDPC codes.', JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.14, NO.4, pp 419-425.

[22] Alaa Aldin Al Hariri, Fabrice Monteiro, Loic Sieler and Abbas Dandache"Configurable and High-Throughput Architectures for Quasi-Cyclic Low-Density Parity-Check Codes.", IEEE International Conference on Electronics, Circuits and Systems (ICECS).,Dec 2014,pp 790-793.

[23] InKi Lee, DeockGil Oh, MinHyuk Kim, JiWon Jung ,"High-speed LDPC Encoder Architecture for Digital Video Broadcasting Systems" International Conference on ICT Convergence (ICTC).,Oct 2013,pp 606-607.

[24] Xiangron Sun, Zhibin Zeng, Zhanxin Yang." A Novel Low Complexity LDPC Encoder Based On Optimized RU Algorithm With Backtracking",. International Conference on Multimedia Technology (ICMT).,Oct 2010,pp1-4.

[25] WANG PENG, CHEN YONG-EN," LOW-COMPLEXITY REAL-TIME LDPC ENCODER DESIGN FOR CMMB." ",. INTERNATIONAL CONFERENCE ON INTELLIGENT INFORMATI-O N HIDING MULTIMEDIA SIGNAL PROCESS. ,AUG 2008; PP-1209–1212.

[26] Seho Myung, Kyeongcheol Yang, and Jaeyoel Kim,(2005) "Quasi-cyclic ldpc codes for fast encoding.", IEEE Transactions on Information Theory,Vol.51, No.8,pp 2894-2901.

[27] Yi Hua Chen, Jue Hsuan Hsiao, Zong Yi Siao, "Wi-Fi LDPC Encoder with Approximate Lower Triangular Diverse Implementation and. Verification",'International Multi-Conference on Systems, Signals & Devices (SSD). ,Feb 2014,pp1-6.

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