DESIGN OF LOW POWER SAR ADC FOR ECG USING 45nm CMOS TECHNOLOGY

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ABSTRACT

Design of a low power Successive Approximation Register Analog to Digital Converter (SAR ADC) in 45nm CMOS Technology for biopotential acquisition systems is presented. It is designed by using a high threshold voltage (Vt) cell to reduce power dissipation. A 10-bit SAR ADC is designed and compared with the low resolution SAR ADC and normal threshold voltage (Vt) ADC with respect to power and delay. The results show that high Vt SAR ADC saves power upto 67% as compared to low Vt SAR ADC without any penalty of delay. Other performance metrics studied are the Effective Number of Bits (ENOB) and Signal to Noise Ratio (SNR), Signal to Noise and Distortion Ratio and Spurious Free Dynamic ratio.

KEYWORDS

Analog-to-Digital Converter, Digital-to-Analog Converter, CMOS, ENOB, SNR and Low power.

1. INTRODUCTION

In biomedical applications, all the signals are physical in nature. Bio medical signals are of low frequency with noise in millivolt range. These signals are converted into electrical signals using sensors. The sensor device is required for sensing the bio-medical signals of human body such as Electro Encephalo Graphy (EEG), Electro Cardio Graphy (ECG), Electro Myo Graphy (EMG) [1]. The main block diagram of Electrocardiogram (ECG) is shown in Figure 1. After sensing, the electrical signals from human body need to be converted to digital signals. Processing of the signals is carried out in the digital domain. For this conversion Analog to Digital Converter (ADC) is required in all bio medical applications. The main aim of the ADC is the conversion of analog signal to its equivalent digital form [2]. This digital signal is further processed and used for transmission. These characteristics necessitate low power and long battery life ADCs. The design of low power ADC with an architecture for low power consumption is the challenge. ADCs should also have less power consumption, moderate resolution and medium sampling rate. This paper presents SAR ADC that meets the above requirements. The proposed SAR ADC operates with medium resolution (8 to 12 bits) and consumes low power. This is due to less number of blocks being used at medium sampling frequency.

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1.1. The Power Reduction by High-V_t Transistors

Short Circuit (SC) power strongly depends on the threshold voltage and can change significantly while moving to a new process. This characteristic can be utilized for SC power optimization in modern multi-threshold processes. Devices with various threshold voltages are used in non critical paths for leakage reduction. Alternatively, leakage reduction is achieved in many processes by using long-length (LL) transistors. These devices usually operate at lower threshold voltage than high-V_t transistors, but allow leakage reduction due to longer channels. Both transistor types can be considered for low-power design while maintaining a similar performance and leakage power [3][4]. The long-channel devices are popular choice for low-leakage design in modern process. However, due to lower threshold voltages, they are less effective in terms of short- circuit. This fact creates an opportunity for SC power optimization in designs with Long Length (LL) transistors. In MTCMOS process, the long-length transistors are replaced with high-threshold transistors. Due to the aforementioned properties of the devices, leakage and timing of the replaced cells can be maintained as before, while reducing the short circuit power consumption.

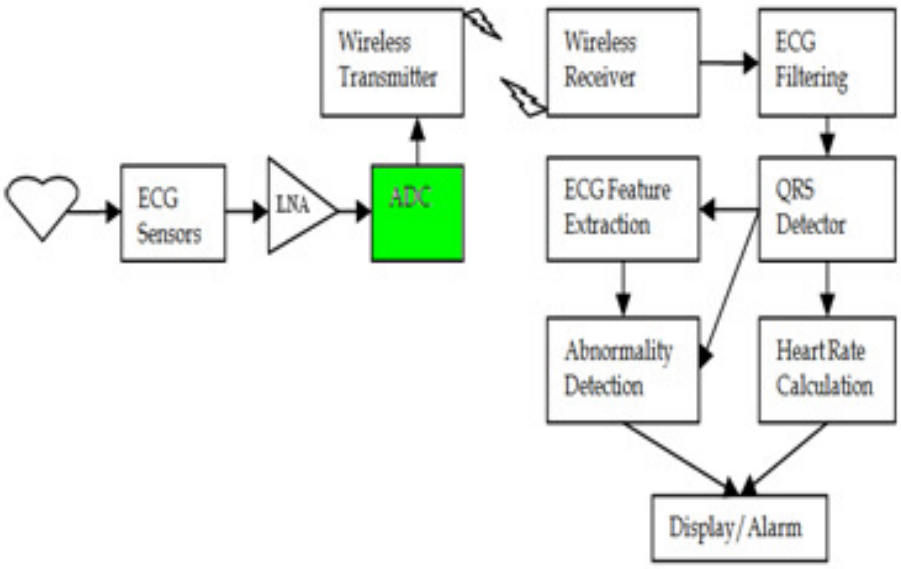

Fig 1. Block diagram of ECG system.

2. SUCCESSIVE APPROXIMATION ADC

The biopotential Acquisition System ASIC (Application Specific Integrated Circuit) requires an Analog- to- Digital Converter for digitizing the analog signals of the readout front end channels. A Successive Approximation Register ADC (SAR ADC) architecture is selected due to its moderate resolution, less conversion time and superior power dissipation characteristics as compared to other architectures [5]. Figure 2 represents the block diagram of the 10-bit SAR ADC.

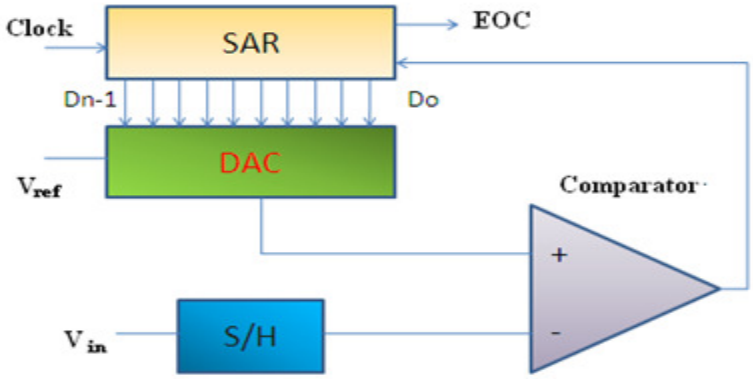

Fig 2. Architecture of SAR ADC.

The SAR ADC works on the principle of binary search algorithm, which performs analog to digital conversion by using the previously determined bits to set the decision condition for the next significant bit. It consists of four internal blocks as shown in Figure 2. A Sample and Hold circuit acquires the input voltage from the ECG system, and then a comparator compares the sampled voltage with the internal DAC output value. DAC then provides the required reference level to the comparator which is placed in the feedback loop. Successive approximation register is used to convert the analog output value into a digital code. This digital code is converted to an analog value by DAC that indicates the consequent reference value [6]. Figure 3 illustrates the binary search algorithm of the SAR ADC.

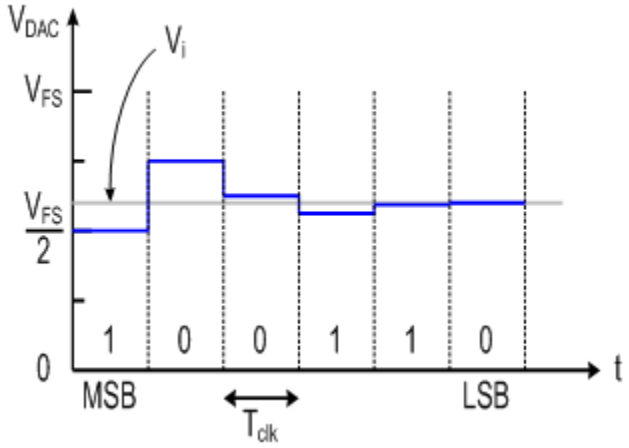

Fig 3. SAR ADC operation using binary search Algorithm.

2.1. Sample and Hold circuit

In the proposed work, a simple transmission gate switch is designed for the sample and hold function as shown in Figure 4. The switch gate-to-source voltage is fixed at the supply voltage V_{DD}. Due to this, the ON-resistance of the sampling switch is less and the linearity of the switch is improved. Figure 5 shows the output of the sample and hold circuit with sinusoidal input signal. Table-I gives the power and delay vlaues for the designed sample and hold circuit in 45 nm CMOS technolgy.

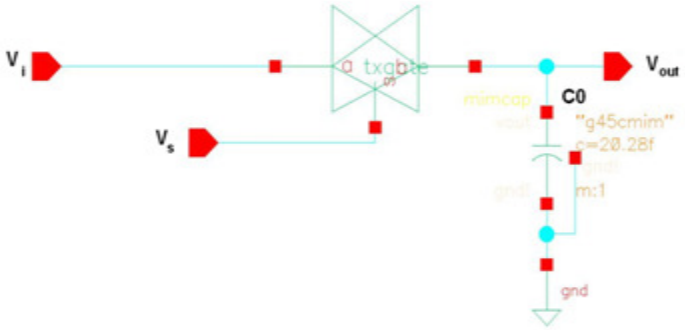

Fig 4. Sample & Hold circuit

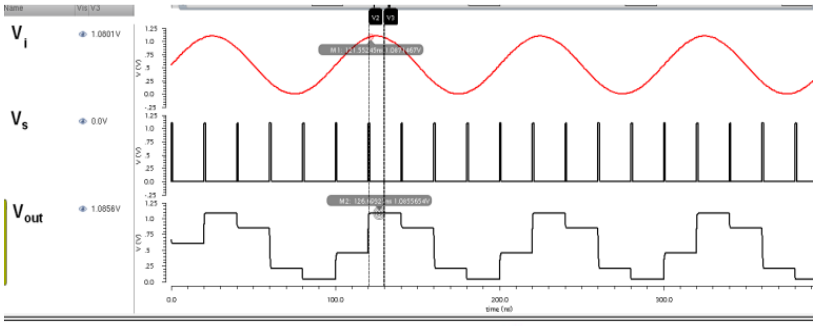

Fig 5. Output of the Sample & Hold circuit.

Table I. Power and delay values of Sample and Hold circuit.

Parameters	Normal V_t	High V_t
Power	101.1 nW	98.43 nW
Delay	4.785 ns	7.979 ns

2.2. Comparator

Comparator compares the analog sample value with the output of the internal DAC. After comparison, it gives the result, high or low logic levels. This output is applied to the SAR. Accuracy and speed of the comparator are two important factors. The comparator needs to resolve voltages with small differences. The offset voltage of the comparator employed in SAR ADC is translated to the transfer characteristic of the ADC. This will not affect the linearity of ADC [7]. In this paper, an open loop comparator is designed and implemented in 45 nm CMOS technology. Figure 6 represents the practically designed circuit of an open loop comparator for the 10- bit SAR ADC.

The main advantage of an open-loop comparator is that, if enough gain is provided, the minimum detectable differential input can be very small (<1mV). It would be reasonable to assume that by simply designing the comparator with the largest possible gain an almost infinite resolution can be achieved. However, increasing the gain also reduces the bandwidth of Op-Amps.

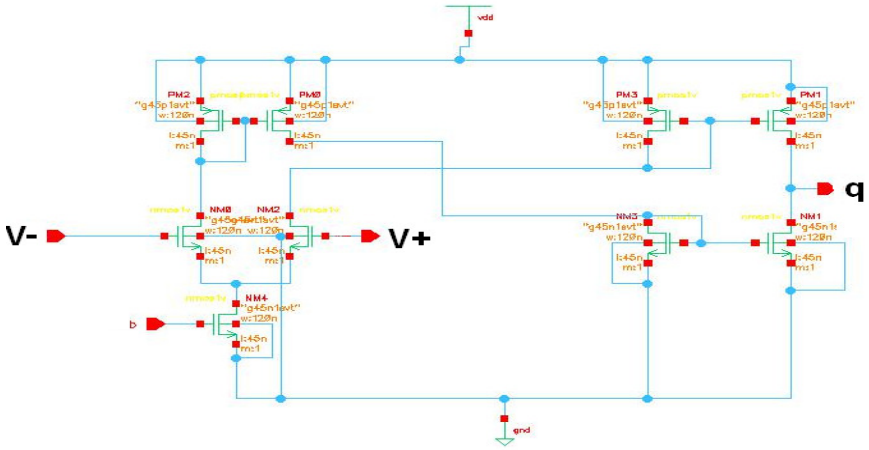

Fig 6. Schematic of a Comparator.

This implies that although the resolution improves, the time response of the comparator degrades. Thus, a trade-off between speed and resolution must be made. The absolute maximum resolution of open-loop comparators is limited by the input-referred noise and the offset voltage present in the OP AMP. Figure 7 shows the output waveform of the proposed open loop comparator and Table II presents corresponding the power and delay values of the designed comparator using normal and high V_t cells respectively.

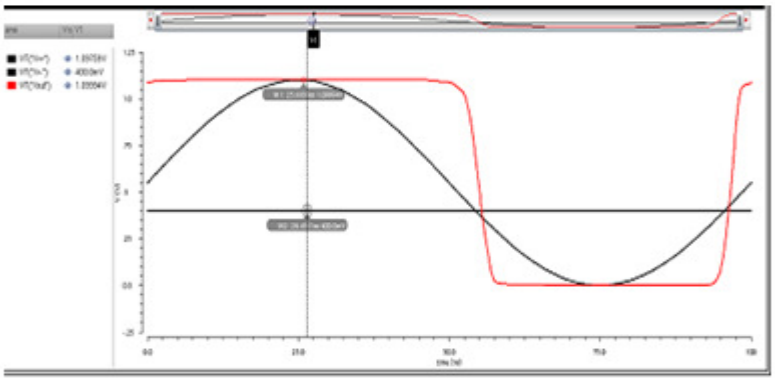

Fig 7. Output waveforms of a Comparator

Table II. Power and delay values of Comparator

Parameters	**Normal V_t**	**High V_t**
Power	2.998 µW	884.3 nW
Delay	1.904 ns	152.1 ps
Offset	115.42 mV	1.35 nV

2.3. Digital Analog Converter

In this work, a resistor string type DAC, that consists of a parallel resistor network is designed in 45 nm CMOS technology. Individual resistors are enabled or bypassed in the network based on the applied digital input. Figure 7 shows the main architecture of the 10- bit resistor string DAC,

which consists of two 9- bit DACs and a transmission gate. Each 9- bit DAC internally consists of two 8- bit DACs and so on. Figure 8 represents the final output of the 10-bit resistor string type DAC. Table III presents the power values of 10- bit resistor string DAC.

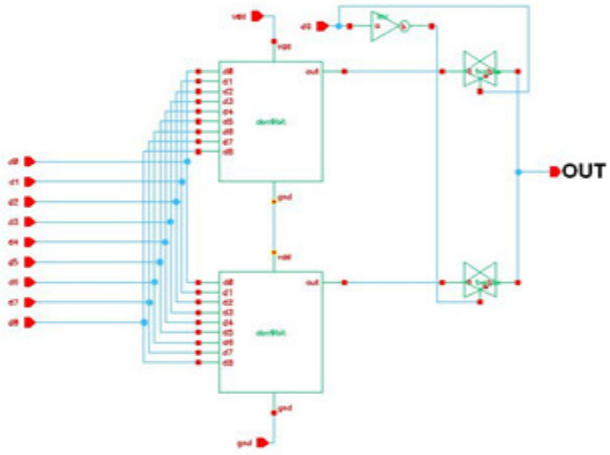

Fig 7. 10 bit Digital to Analog Converter

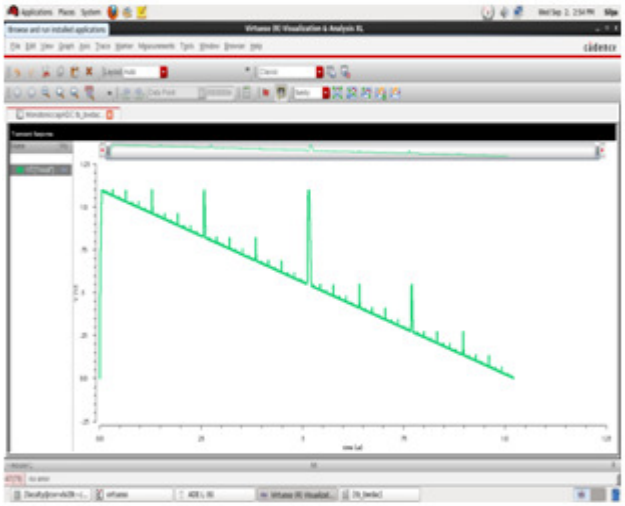

Fig 8. 10- bit DAC Output waveform.

Table III. Power and delay values of 10- bit DAC.

Parameters	**Normal V_t**	**High V_t**
Power	118.5 µW	109.7 µW

2.4. Successive Approximation Register

The purpose of the SAR circuit is to determine the value of each bit of the ADC in a sequential manner, depending on the value of the comparator output. This SAR is implemented by two sets of D-flip flops. For the N-bit ADC, the SAR requires at least 2^N states and hence 'N' flip flops.

The different types of Flip Flops and the arrangement of flip flops are shown in Figure 9 for overall SAR ADC. The D-FF with Clr and Preset, D-FF with only Clr and D-FF with only preset are mainly used in the design of SAR ADC to implement binary search algorithm. Tables IV, V and VI show the practical power and delay values for the D flip flops.

Table IV. Power and delay values of D-FF with Clr

Parameters	**Normal V_t**	**High V_t**
Power	2.058µW	1.842 µW
Delay	4.01ns	4.02 ns

Table V. Power and delay values of D-FF with Preset.

Parameters	**Normal V_t**	**High V_t**
Power	2.089 µW	1.848 µW
Delay	5.257 ps	22.02 ns

Table VI. Power and delay values of D-FF with preset and Clr.

Parameters	**Normal V_t**	**High V_t**
Power	2.08 µW	1.875 µW
Delay	12.44 ps	2.081 ns

3. DESIGN OF SAR ADC

The 10-bit SAR ADC is implemented in TSMC (Taiwan Semiconductor) 45nm technology using high threshold voltages and normal threshold cells using CADENCE tools. The practical designed circuit and the ADC output waveforms are shown in Figures 9 and 10 respectively.

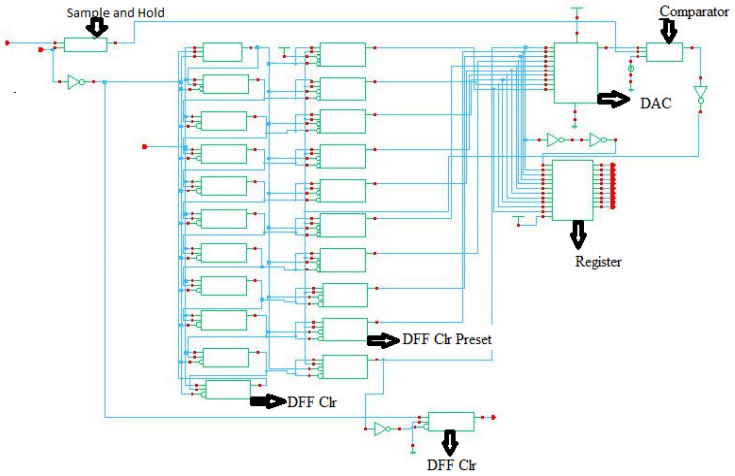

Fig 9. The 10-bit SAR ADC Schematic

3.1. Power Consumption

The total power consumption of a CMOS circuit can be expressed by dynamic Power Consumption, leakage Power Consumption or direct-path consumption and short circuit power. The last item is neglected due to lower contribution to power. The dominant factor is the dynamic power is:

$$P_{dynamic} = \alpha C_L V_{dd}^2 f$$

where C_L = total output capacitive load

f = frequency of operation

α = switching activity factor

V_{dd} = Supply Voltage

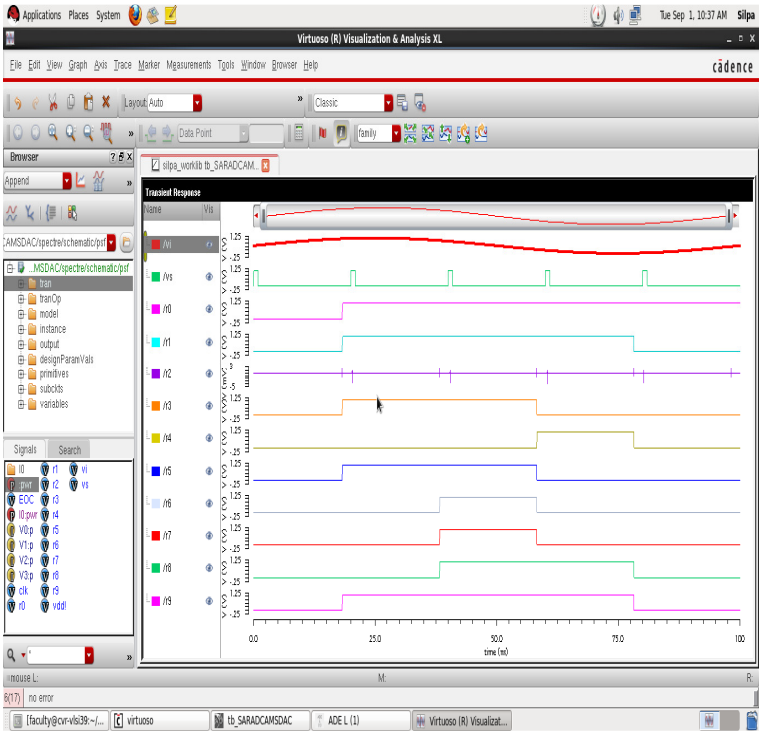

Fig 10. The output Waveforms of the 10-Bit SAR ADC

This equation indicates that dynamic power consumption is proportional to the square of the supply voltage. In this circuit the supply voltage is 1.1V, which is very less in 45 nm technology. Further reduction of leakage power consumption is done by high V_t cells which are used in the transmission gate of Sample and Hold circuit. The above circuit is designed in 45nm technology. As technology expands, the sub threshold leakage current increases.

3.2. Sub-threshold region

The region just below V_t of a transistor is called sub-threshold region. When the gate to source voltage V_{gs} is less than V_t , then the leakage current

$$I_{leakage} = \mu(W/L)e^{(-qV_t/\eta KT)}$$

Where μ = mobility
W = width of MOSFET
L = Length of MOSFET
K = Boltzmans constant
T = Temperature
q = Charge of an electron
V_t = Threshold Voltage
η = Sub-threshold switching Coefficient

This indicates that the parameters μ, K, q are constants and only V_t and W are dependent on $I_{leakage}$. As width of MOSFET increases leakage current also increases and as V_t increases, the leakage current decreases exponentially. This in turn reduces leakage power. This justifies the usage of high V_t devices in our design.

4. RESULTS

Table VI describes the performance metrics of the 4-bit SAR ADC and 10- bit SAR ADC, which are implemented in 45 nm COMS technology using CADENCE tools.

Table VII. Dynamic Performance Characteristics of 4-bit and 10 bit SAR ADC

Parameter	**4bit SAR ADC**		**10 bit SAR ADC**	
	Normal V_t	**High V_t**	**Normal V_t**	**High V_t**
Power (μW)	98.85	91.89	330.5	109.0
Delay (ns)	48.09	44.79	75.39	77.72
ENOB (bits)	3.73		9.1	
SINAD (dB)	24.22		56.64	
SNR (dB)	24.2		40.0	
SFDR (dB)	33.915		47.66	

Power consumption of the 10-bit SAR ADC using low V_t cells is 330.5 µW. If high V_t cells are used in the implementation, then 10-bit SAR ADC power consumption is 109.0 µW. Hence, the overall power reduction in the 10- bit SAR ADC is 67% because of high V_t cells.

In the case of the 4-bit SAR ADC, the power of low V_t circuit is 98.85 µW and high V_t cell circuit consumes power of 91.89 µW. The power reduction due to the high V_t cells is only 10%. In comparison with 10- bit SAR ADC using high V_t and 10-bit SAR ADC with low V_t circuits, the power reduction is 33%. Hence it is evident that higher resolution ADC saves more power.

Table-VII also presents comparative results of delay for 10-bit and 4-bit SAR ADCs for low V_t and high V_t circuits. From the above results, it appears that the delay is almost maintained as a constant. Due to high V_t cells the delay of the SAR ADC is increased to 1.03% only.

The other performance metrics for 4-bit and 10-bit SAR ADCs, such as the Effective Number of Bits (ENOB) is 3.71 and 9.1, Signal to Noise Ratio (SNR) values are 24.2dB and 40dB, Signal to Noise and Distortion Ratio(SNDR) are 24.22 and 56.64dB and Spurious Free Dynamic Ratio(SFDR) values are 33.9 and 47.66 dB respectively.

5. CONCLUSION

A SAR ADC architecture using high threshold voltage cells has been presented. The transmission gate Sample and Hold circuit is designed using high threshold voltage transistors and compared with low V_t Sample and Hold circuit. The open loop comparator using basic operational amplifier has been designed with high V_t cells to reduce power consumption and delay using 45 nm CMOS technology. The resistor string type DAC block has also been designed in 45 nm technology using high threshold voltages. Such an ADC approach significantly reduces power consumption and delay of the ADC. This ADC uses the binary search algorithm and fit with the sampling rate of the ECG and gives the best performance.

REFERENCES

[1] Xiaoyuan Xu, Xiaodan Zou, Libin Yao and Yong Lian, "A 1-V 450- nW fully integrated biomedical sensor interface System," IEEE Symp. VLSI Circuits Dig. Tech. Papers, pp. 78-79, June. 2008.

[2] Ming Yin and Maysam Ghovanloo, "A flexible clockless 32-ch simultaneous wireless neural recording system with adjustable resolution," in ISSCC Dig. Tech. Papers, pp. 432-433, February. 2009.

[3] Chatterjee, A.Nandakumar, M.Chen, I. "An investigation of the impact of technology scaling on power wasted as short-circuit current in low voltage static CMOS circuits". Proceedings of the International Symposium on Low Power Electronics and Design, Mnonterey, CA, USA, 12–14 August 1996; pp. 145–150.

[4] Yuffe, M. Knoll, E. Mehalel, M. Shor, J. Kurts, T. "A Fully Integrated Multi-CPU, GPU and Memory Controller 32 nm Processor". In Proceedings of IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 19–23 February 2011.

[5] M.VanElzakker, E.Van Tuijl, P.Geraedts, D.Schinkel, E.klumperink,and B.Nauta,"A 1.9µW 4.4fJ/Conversion/Step 10b 1MS/s charge-redistribution ADC", ISSCC Dig.Tech.Papers, pp.244-610,Feb.2008.

[6] Y.K. Chang, C.S. Wang, and C.K. Wang, “A 8-bit 500-KS/s low power SAR ADC for bio-medical applications”, Asian Solid-State Circuits Conference (A-SSCC) Dig. Tech. Papers, pp. 228-231, November. 2007.