

DESIGN OF LOW POWER MEDICAL DEVICE

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ABSTRACT

This paper describes the design of an MMIC phase shifter which can be used in a 4-channel 26-28 GHz transmitter IC. The MMIC phase shifter is used for 5G RF front ended applications. MMICs usually include power amplifiers with 4-bit digital phase shifters to make the phase adjustable. The whole design was used for the transmit chain of a mobile device and in a base-station. Future topology will continue to be improved.

KEYWORDS

Doherty Power Amplifier, MMIC, phase shifter

1. INTRODUCTION

5G technology is becoming a hot topic these days; many universities and companies are putting effort and money into this area. The 5G standard is not fixed yet, so all of the major players want to position themselves as key players in the market, since it can provide wide bandwidth, faster speed, and higher data rates. All the benefits which the current 4G network cannot provide. With the improved performance, a customer can download a high definition TV show in a second, or a high virtual reality gaming show; It will enable new markets, technologies and applications[1].

Since 5G is still under construction, the possible spectrum will be much higher than current cellular frequencies - possibly around 27G, or 60G. Because all the frequencies under 3G Hz are taken, the higher spectrum must be used. Therefore, for the 5G radio frequency, higher frequency will be used, since it will also reduce the interference with currently used frequencies. Mm-waves are a good option in the USA and many Asian countries. Research is looking at using phased array of antennas to transmit power[2][3]. Due to the high frequency, the size is small which is good to save cost. Bands within 27 GHz to 29.5 GHz are also an excellent solution for 5GHz radio research.

The Figure 1 shows a 28GHz transmit IC RF front end circuit. It shows a 4 element antenna array, with each antenna controlled by a phase adjusted power amplifier. The phase shift cannot just change the phase but also reject the harmonics in the receive band[1].

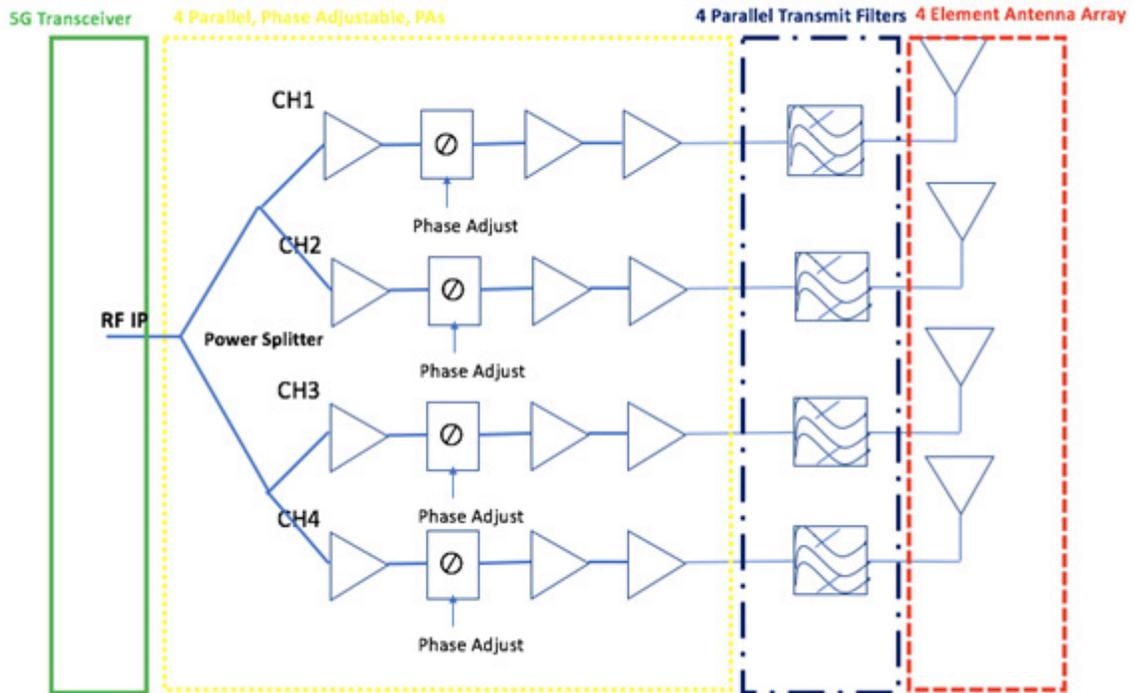


Figure1: MMIC schematic

2. BACKGROUND

For transmitters, power amplifiers (PA) are always a central element, which can highly affect the linearity and power efficiency of the whole system[4]. For a high efficiency PA at a wide range of output power the Doherty Power Amplifier (DPA) is a good solution, since it has excellent linearity while dealing with amplitude modulated signals. In this paper, a design for a low power and high linearity DPA for wireless networks is explored.

Table 1. DPA Comparasion.

Type	Output Power	Efficiency	RF Band	Mod. Band
Class AB	High	Low	High	High
DPA	High	High	Low	High
Outphasing	High	Medium	Low	Low
Envelope tracking	Medium	High	High	Low
Bias Modulation	Low	High	High	Low

Because of the demands of high data rates with specific modulation, high efficiency with an excellent peak to average power ratio is required[5]. Class AB PAs are well suited for the maximum output power, but their efficiency is low. The DPA is highly linear using digital predistortion, making it a suitable solution for 3G and 4G handset systems, as seen in Table 1. The combination of a DPA and digital predistortion can achieve high average efficiency and the required linearity.

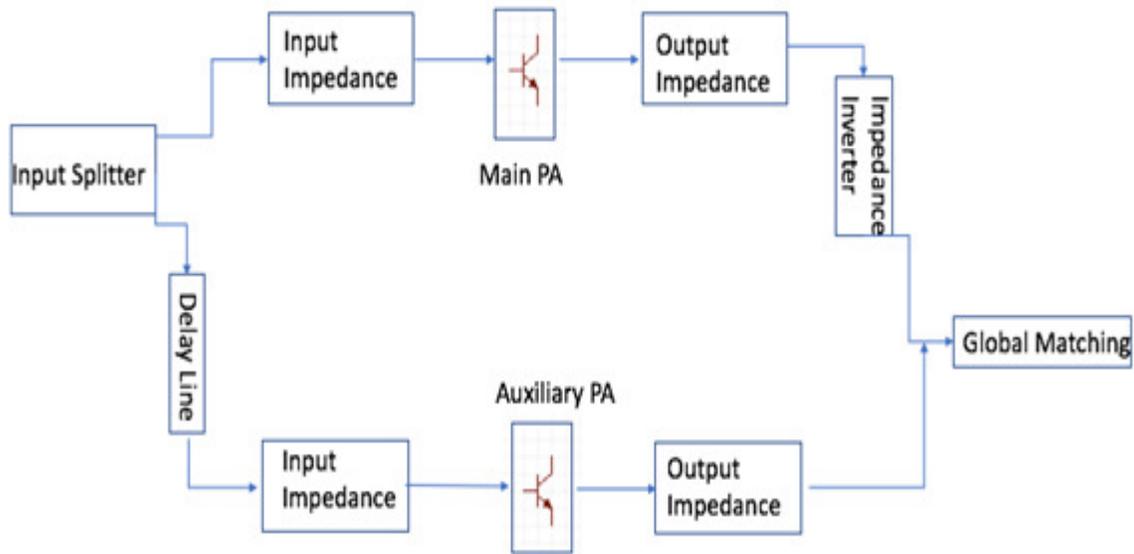


Figure2. DPA basic topology

The Doherty amplifier shown in Figure 2 has two PAs in parallel. The two PAs are both on when the amplifier is at full power. Only one PA is on when the power draw is low. For such a configuration, when the auxiliary PA is off and the total power draw is reduced, the load impedance of the main PA will be increased, allowing it to operate at higher efficiency. Such a topology would provide higher efficiency compared with a single power amplifier. Implementing quarter wavelength lengthscan be done by using lumped element impedance inverters.

3. DESIGN

Cadence RF spectre was used to simulate a two stage DPA design. Each amplifier was simulated first at DC and S-parameters condition, to ensure functional operation. Then harmonic balance simulation was performed to ensure stability conditions. The last step was to combine the two amplifiers and the impedance inverters to form the base control DPA and perform a performance simulation. The input and output impedance inverters and the interstage match between Q_{1hp} and Q_{2hp} were adjusted to improve the phase match between the two amplifiers of the DPA, to optimize power transfer[6]. A base control DPA was analyzed, designed and simulated.

The basic structure of the PA cell is shown in Figure 3[6]. The main PA, which is a carrier amplifier is the low power amplifier. The auxiliary PA, or the peaking amplifier will be referred to as the high-power amplifier. All the devices are connected in series, making the device stronger. The resistors are applied to the bias while also connecting to the base of each device, preventing current hogging. Resistors also improve the device's stability at all frequencies. Capacitors are used to couple with the RF input while also connecting to the base of each cell. Due to the feedback of gate to source this topology can make a stable device at all frequencies.

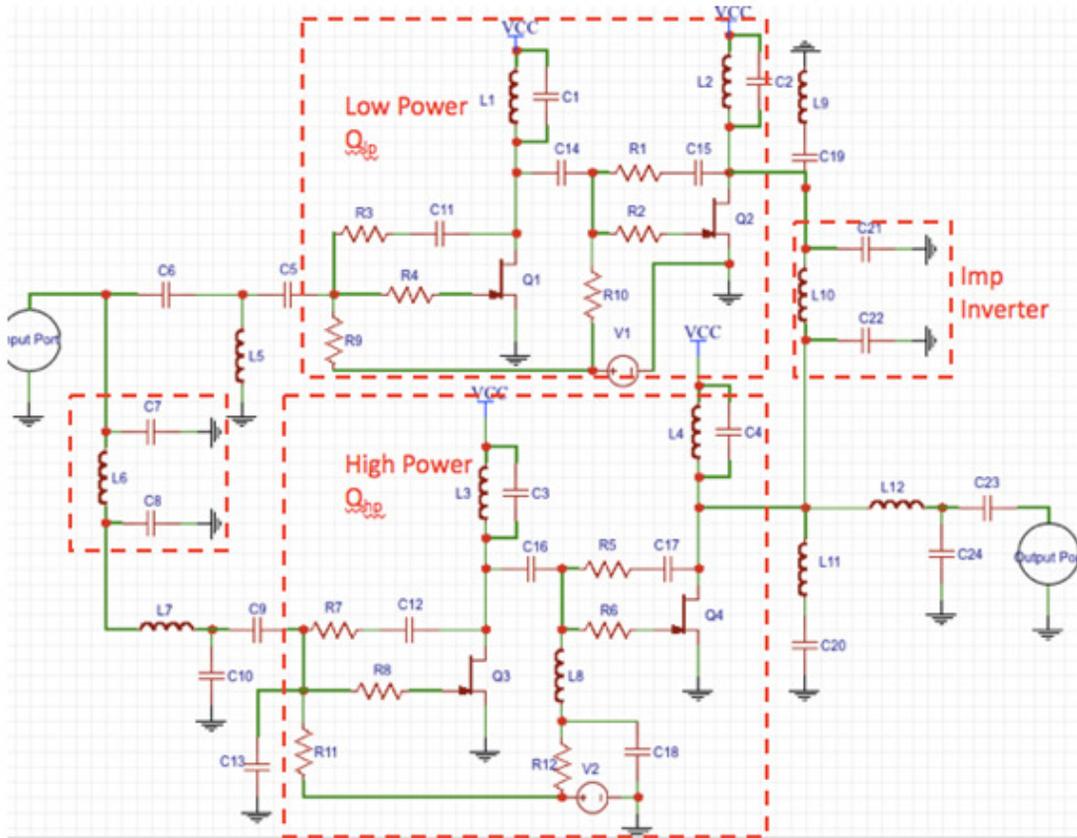


Figure 3. Whole DPA topology.

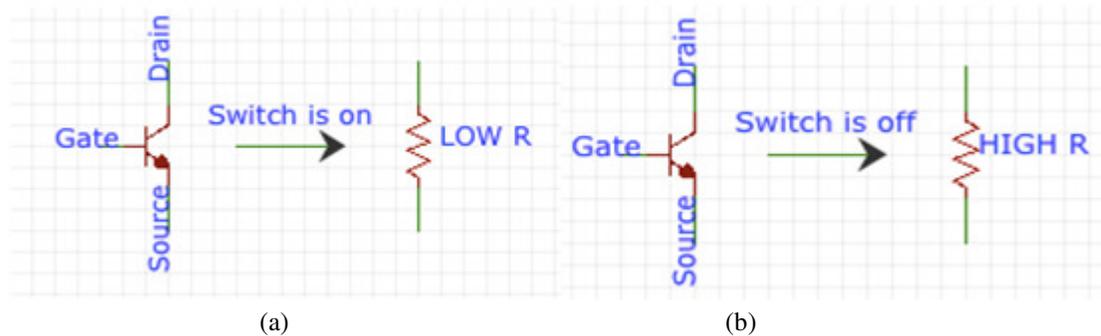


Figure 4: Switch MOSFET working condition (a) Switch on (b) Switch off

As seen in the Figure 4, when the voltage was forward-biased, the switch was on - this can be modeled as a small resistor. When the switch is off, the simplified circuit can be approximated as a large resistor. The phase shifter was designed as a high-pass/low-pass operating phase shifter with switching MESFETs. When a switching MESFET had a forward bias, it was modeled as a low resistor. When it had a reverse bias, it was modeled as a large resistor.

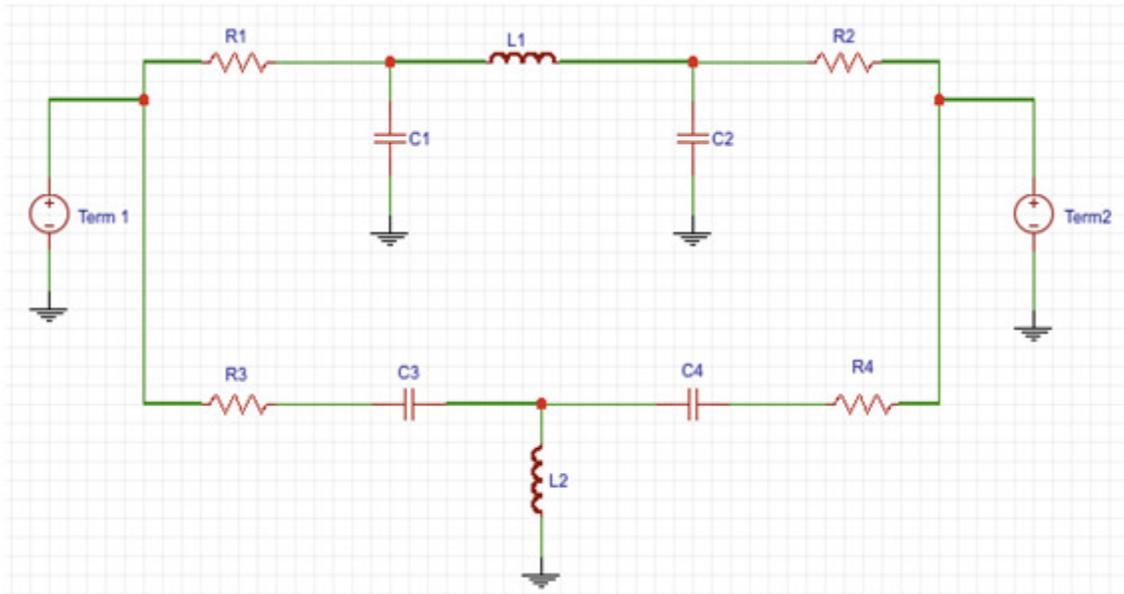


Figure 5: Phase shifter Schematic

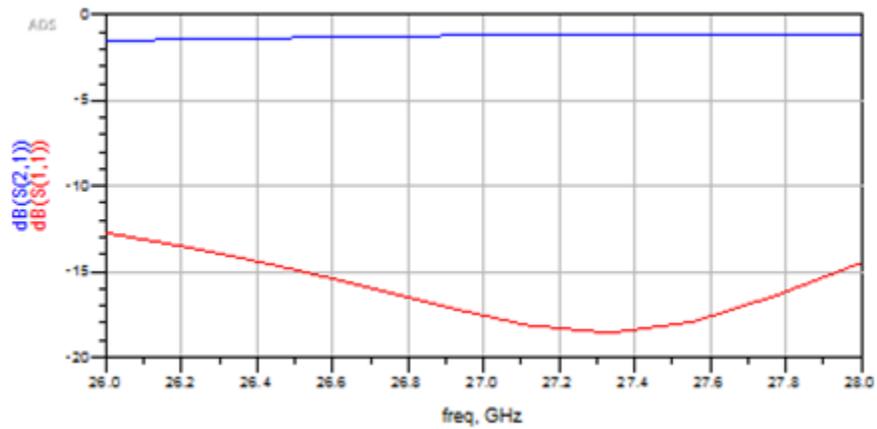
The phase shifter as seen in Figure 5 is using a switched high-pass/low-pass filter topology[1]. High pass filters have better a phase advance compared to low pass filters because it is constant under relatively wide bandwidth. Optimization of the components seeks to get better performance, such as: phase difference with a minimum amplitude difference. The overall better solution is to get lower insertion loss as well as high isolation loss.

A high-performance phase shifter would have a steady amplitude response under some range of phase change. Though there would be always some change limiting the amplitude change leads to better performance. When the reflected waves changes, the phase shifter would also change, more detailed design simulation can be seen in Table 2.

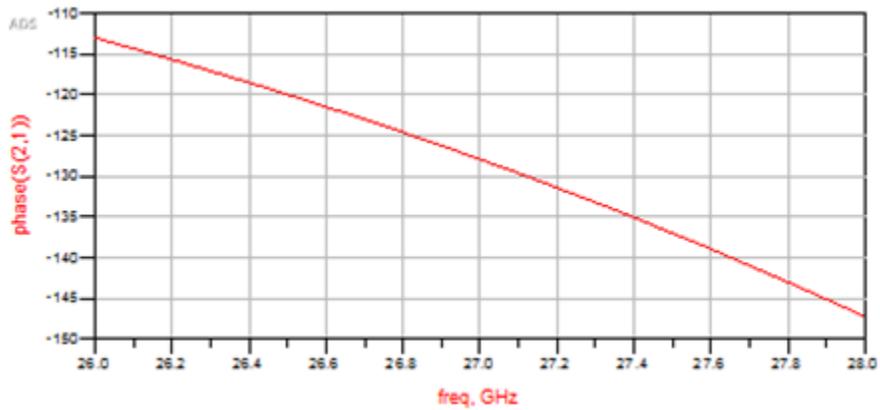
Table 2 Phase Shifter sizesF

Parameter	Size (Unit)
R1, R2	20 ohm
R3, R4	0.05 ohm
L1,L2	0.683 nH
C1,C2,C3,C4	22.6 Ff

4. RESULTS



(a)



(b)

Figure 6. Phase Shifter (a) Magnitude (b) Phase

Figure 6 shows the results for the mmic phase shifter. The S11 and S21 magnitudes achieve -10 dB and -1dB, respectively. The phase difference of the S21 could be -110 to -145 degrees between 26GHz to 28GHz.

5. CONCLUSIONS

Simulation of an RF DPA using cadence software, based on IBM's SI 180nm technology process, is presented. Simulation of an RF phase shifter using ADS software is also presented. This RF health care applications has been realized, but the current design still has room for further improvement for future requirements. To realize this, future improvement is needed.

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