ZIGBEE TRANSMITTER FOR IOT WIRELESS DEVICES

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ABSTRACT

The rapid development in wireless networking has been witnessed in past several years, which aimed on high speed and long range applications. There are different protocol standards used for the short range wireless communication namely the Bluetooth, ZigBee, Wimax and Wi-Fi. Among these standards ZigBee is based on IEEE 802.15.4 protocol can meet a wider variety of real industrial needs due to its long-term battery operation and reliability of the mesh networking architecture. The increasing demand for low data rate and low power networking led to the development of ZigBee technology. This technology was developed for Wireless Personal Area Networks (WPAN), directed at control and military applications, where low cost, low data rate, and more battery life were main requirements. This paper presents Verilog-HDL simulation of the Top level module (Cyclic Redundancy Check, Bit-to-Symbol block, Symbol-to-Chip block, OQPSK block and Pulse shaping) of the ZigBee transmitter for IoT applications.

Keywords

Cyclic Redundancy Check, Bit-to-Symbol, Symbol-to-Chip, Offset Quadrature Phase Shift Keying Modulator and Pulse Shaping.

1. INTRODUCTION

1.1. MOTIVATION

ZigBee standard was specifically developed to address the need for very low cost implementation of low data rate wireless networks with ultra low power consumption. The ZigBee Standard reduces the implementation cost by simplifying the communication protocols at reduced data rate. The minimum requirements to meet ZigBee specifications are relatively relaxed as compared to other standards such as IEEE 802.11 and Bluetooth. This reduces the complexity and cost of implementing ZigBee compliant transceivers. This feature of ZigBee enhances the application in wireless sensor network for gathering information from sensors such as temperature, humidity, pressure and other physical parameters[1]. ZigBee is the only standards-based technology that addresses the unique needs of most remote monitoring and control sensory network applications.

1.2. INTRODUCTION

There are different types of wireless networks such as Bluetooth, Wi-Fi, Wimax and Zigbee[2]. The IEEE802.15.1 protocol is used for Bluetooth. We are using FHSS (Frequency Hopping Spread Spectrum) method in Bluetooth. The advantages of Bluetooth is easy to install, low cost, low power consumption, Data rate is 1Mbps, transmission distance is 30-50mts. The Bluetooth

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disadvantages are system resources requires 250KB, low battery life 1-7 days, Transmission range is 1-10 days and network size is 7.

The IEEE 802.11 protocol is used for Wi-Fi. Wi-Fi stands for Wireless Fidelity. Wi-Fi operating frequency is 2.4GHz or 5.8GHz bands. The Wi-Fi advantages are System resources requires 1MB, transmission range is 1-100mts, bandwidth is 11,000Kb/s. In these Wi-Fi for installation or created with AP(Acess Point) and Speed is 1.3GHz. Disadvantages of Wi-Fi is Higher cost, speed and performance can vary for different devices, Battery life is 5 days and the network size is 32.

The IEEE 802.16 protocol is used for Wimax. Wimax stands for Worldwide interoperability for Microwave Access.In Wimax OFDM(Orthogonal Frequency Division Multiplex) method is used. The advantages of Wimax is high speed data and speed 10Mbps to 10Kilometers with line of site. The disadvantages of Wimax is power consumption more, other wireless equipment could cause interference and weather conditions like rain could cause interrupt the signal.

The IEEE 802.15.4 protocol is used for Zigbee. Zigbee uses DSSS(Direct sequence spread spectrum method). The advantages of Zigbee is low power, low cost, long battery life (1-100mts), unlimited network size(264) and transmission range is 1-100mts.Zigbee operating frequency is868 MHz in Europe, 915 MHz in the USA and Australia, and 2.4 GHz in most jurisdictions worldwide. Zigbee provides a data integrity check and authentication function.AES-128 is adopted.

ZigBee is a wireless networking for a high-level communication protocols using small, low-power and low-cost radios[3]. It is used to create Personal Area Network .Zigbee is an IEEE 802.15.4 based specification. This IEEE standard describes physical and MAC layer only[4]. Data rate of Zigbee is 250 Kbps. Zigbee devices can use System-on-chip solutions with integrated radio and 60-250 flash memory[5]. Zigbee basically operates three frequency bands. In the industrial, scientific and medical(ISM) radio bands; 868 MHz in Europe, 915 MHz in the USA and Australia, and 2.4 GHz in most jurisdictions worldwide. In this operating frequency is 2.4 GHz and data transmission range is from 10 to 100 meters [6]. It operates on 2.4 GHz with data rate of 250 Kbps.

ZigBee supports three types of network topologies; star topology, mesh topology, and combined topology. The ZigBee concentrate on the low data rate and low power consumption, directed towards remote control and military applications. ZigBee uses very low data rate and has a long battery life, which makes it widely useful in monitoring and control applications[7]. Therefore, markets as building automation, industrial control, lighting in smart homes, personal health care, and commercial control are perfect fits. The human interface devices such as keyboards, mice, joysticks etc. and high end remote control for consumer electronics are also good fits.



Figure 1. ZigBee transmitter and receiver

ZigBee devices are now getting more attention towards Internet of Things (IOT). The ZigBee standard is maintained by ZigBee alliance. Fig.1 displays a commercial ZigBee transmitter and receiver pair[3].

IOT: In today's world everything is going smart, smart power grids, smart sensor networks, smart homes, and smart water distribution systems. The common perspective for these systems is usually associated with one single concept, known as Internet of Things (IOT). The IOT make use of intelligently connected devices, and systems to transfer data over a network without requiring human-to-human or human-to-computer interaction. For example, in a smart home, air conditioner can communicate with your car so that when car is nearby, it could automatically switch on or when you enter home the light automatically glows up. For these interconnected networks, Wireless Sensor Networks (WSN) could become the important technology.

2. ZIGBEE TRANSMITTER

2.1 SPECIFICATION

Zigbee digital transmitter in 2.4GHZ band is designed using Verilog for acknowledgement frame (or) architecture. There are two types of layers. (i) Physical layer and (ii) Medium Access Control (MAC) layer.

Physical layer supports 3 frequency bands are 2.45 GHZ band with 16 channels, 915 MHZ band with 10 channels, 868 MHZ band with 1 channel. In these Zigbee transmitter we are using 2.4 GHZ band because it is a world wide band. In these scheme, we focus on 2.4 GHZ band application which has 16 channels with spacing of 5 MHZ and data rate is 250 Kbps.

MAC layer defines two types of nodes they are Reduced Function Devices (RFDs) and Full Function Devices (FFDs).RFDs can only act as end device and are equipped with sensors or actuators like transducers, light, switches and lamps. They may only interact with a single FFDs. FFDs are equipped with a full set of MAC layer functions, which enables them to act as a network coordinator or a network end-device.

Parameter	Specification
Data rate	250Kbps
No.of channel	16
Operating Frequency	2.4 GHz
Channel spacing	5 MHz
Spread spectrum	Direct Sequence Spread Spectrum(DSSS)
Chip rate	2 Mega chips per second
Modulation	OQPSK with pulse shaping

Table 1. Specification

The IEEE 802.15.4 defines four MAC frame structures: beacon, data, acknowledgement and MAC command frames. The beacon frame is used by a coordinator to transmit beacons. The function of beacons is to synchronize the clock of all the devices within the same network. The data frame is used to transmit data. Meanwhile, the acknowledgment frame is used to confirm successful frame reception. The MAC commands are transmitted using a MAC command frame.

International Journal of VLSI design & Communication Systems (VLSICS) Vol.8, No.5, October 2017 The represents the acknowledgment frame format:

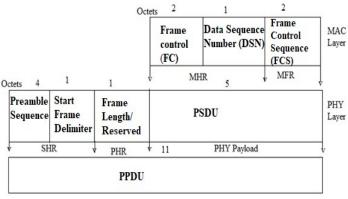


Figure 2. Architecture

The ZigBee standard employs Direct Sequence Spread Spectrum (DSSS) technique to avoid interference. The modulation is done using Offset Quadrature Phase Shift Key (O-QPSK) modulator, which sum the in-phase signal with a half cycle delayed quadrature phase signal. The ZigBee transmitter has been designed for the use of acknowledgment frame format, which is the simplest MAC sub layer frame format without Medium Access Control (MAC) payload. It provides the active feedback from the receiver to sender that the packet has been received without error.

2.2. MEDIUM ACCESS CONTROL (MAC) LAYER

The MAC layer comprises of MAC Header (MHR) and MAC Footer (MFR). The MHR consists of MAC frame control and data sequence number, while MAC Footer (MFR) constitutes Frame Control Sequence (FCS).

2.2.1. FRAME CONTROL (FC)

Frame Control is a 16-bit long field, which gives information about the frame types, source and destination addressing modes. Frame types indicate whether the frame is beacon type, ACK frame, MAC command frame etc. (beacon-starting one)

2.2.2. DATA SEQUENCE NUMBER (DSN)

DSN is an 8-bit value, which is used when stream of data is sent. It acts as a counter that increments itself after each frame.

2.2.3. FRAME CONTROL SEQUENCE (FCS)

It is a 16-bit field which contains 16-bit CRC for detecting errors during transmission. This frame is passed to the Physical (PHY) layer as the Physical Service Data Unit (PSDU), which becomes PHY payload.

2.3. PHYSICAL (PHY) LAYER

The PHY Payload which actually comes from acknowledgment frame (PSDU) is prefixed with Synchronous Header (SHR) and PHY Header (PHR).

2.3.1. SYNCHRONOUS HEADER (SHR)

The SHR has preamble sequence and start of frame delimiter.

The preamble sequence is a 32-bit field used for synchronization between transmitter and receiver. It consists of string of 0s and 1s. After detecting sync field, the receiver starts synchronization with the incoming signal. (Synchronization-two or more things at the same time). The Start of Frame Delimiter is an 8-bit long field which indicates beginning of the frame. (Delimiter-separation).

2.3.2. PHR

It consists only frame length. It is an 8-bit long field, where 7-bits indicate length of PSDU and reserved 1-bit indicates if packet is received or not.

2.3.3. PSDU

It becomes PHY payload which actually comes from acknowledgement frame (PSDU) i.e., MHR and MFR. It is prefixed with SHR and PHR.

2.4. PPDU

It's a data holding one. From the frame which is coming from the PSDU with an additional PLCP preamble and header as a PLCP Protocol Data Unit (PPDU). The PPDU is also called as the PLCP Service Data Unit (PSDU) and is typically referred to as physical layer operation. At last it totally comes under PPDU is 88-bits.

Table: Summarizes the bit length and value of each field employed in this project, which sums up into the total length of PPDU i.e. 88 bits.

Field	Bit Length
Preamble sequence	32(set as logic 0)
Start of Frame Delimiter(SFD)	8(11100101)
Physical Header (PHR)	8(10100000)
Frame Control	16(010001000000000)
Sequence Number	8(1000000)
Frame Control Sequence(FCS)	16(From CRC)
Total	88

Table 2. Bit Length of Each Field in the PPDU

3. BLOCK DIAGRAM OF ZIGBEE TRANSMITTER

ZigBee transmitter comprises of five blocks viz.: CRC, Bit-to-Symbol, Symbol-to-Chip, O-QPSK Modulator and Pulse shaping. Below Fig. shows the basic block diagram of a ZigBee transmitter.

From the PPDU 11 octets are given to CRC. Cyclic Redundancy check is a data transmission error detecting technique. This block calculates 16 bit CRC, which is appended at the end of data

bits. The CRC is calculated over the data of MHR and MFR payloads of MAC layer. The output from CRC block is fed to the input of Bit-to-Symbol block.

Bit-to-Symbol block takes 88 bits as input and maps that binary information into symbols. The 4 LSBs (b0, b1, b2, b3) of each octet are mapped into one data symbol (S1) and 4 MSBs (b4, b5, b6, b7) of each octet are mapped into other data symbol (S2). Thus, a total of 22 symbols are taken out from the Bit-to Symbol block and given output to the Symbol-to-Chip block.

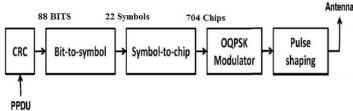


Figure 3. Block diagram of Zigbee transmitter.

In Symbol-to-Chip block, DSSS technique is performed where 32-bit PN sequence is generated for every symbol. The output gets 704 Chips and given the output to OQPSK.

The ZigBee standard uses OQPSK modulating technique. This modulator is used to avoid intersymbol interference and other transmission noises. It will never jump more than 90 degree. But QPSK will jump 180 degree. So, we cause band noise.

Pulse shaping of I-phase and Q-phase data stream is achieved by processing the signal. This helps to reduce side lobes keeping inter symbol interference (ISI) low.

4. CRC, BIT-TO-SYMBOL, SYMBOL-TO-CHIP, OQPSK

4.1. CRC

CRC stands for Cyclic Redundancy Check Codes. Error detecting is a technique of detecting bit errors occurring due to noise or attenuation during data transmission. The error detecting techniques are parity checking, checksum, redundancy checking, and cyclic redundancy checking. The CRC calculation is based on the polynomial arithmetic. The bits of the binary data represent the coefficients of the polynomial. For example, the message 11001001 represents a polynomial of x7+x6+x3+1. The sender and receiver, both have the generator polynomial. The arithmetic involved in CRC calculation is modulo-2 division.

4.1.1. DESIGN METHODOLOGY

The CRC can be implemented using linear feedback shift registers (LFSR) as shown in the fig. 4. In this project, CRCCCITT has been used, which have generator polynomial x16+x12+x5+1. The implemented CRC is serial in nature; therefore output will come only after all the input bits are fed to the CRC block. The CRC is calculated over the data of MHR and MFR payloads of MAC layer.

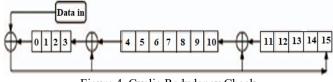
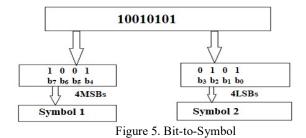


Figure 4. Cyclic Redudancy Check

The algorithm used for this CRC calculation is given below: (1) Initialize all linear feedback shift registers to zero. (2) Enter the data (LSB first) into registers of the divider. (3) After the last bit entered in the divider, the remainder consists of FCS of 16-bit. (4) The FCS is then appended at the end of data bits to obtain the transmitted frame.

4.2. BIT-TO-SYMBOL

Bit to Symbol block maps bits into symbols. This 88 bits data is passed through Bit-to-Symbol block sequentially, starting with the preamble field and ending with last octet of the PPDU i.e. FCS which is generated by CRC. Fig. shows how one octet is divided into corresponding symbols. Therefore, it takes 11 octets as input, where the 4 LSBs (b0, b1, b2, b3) are mapped into one data symbol (S1) and the 4 MSBs (b4, b5, b6, b7) are mapped into next data symbol (S2). Thus, 11 octets maps into 22 symbols.



Digital signal of data bit '1' and '0' inside the PHY Protocol Data Unit(PPDU) is encoded as per the spreading function. Here binary inputs are mapped to data symbols. For four bit symbol there are sixteen possible symbol starting from 0000 to 1111 are mapped to data symbol. Thus there are sixteen symbol to chip mapping as presented in following section.

4.3. SYMBOL-TO-CHIP:

The process of Symbol-to-chip mapping is present in the below fig.

Data symbol (decimal)	Data symbol (binary) (b ₀ b ₁ b ₂ b ₃)	Chip values (C ₀ C ₁ C ₂ C ₂₉ C ₃₀ C ₃₁)
0	0000	11011001110000110101000010101000101110
1	1000	11101101100111000011010100010
2	0100	0010111011011001110000110101010
3	1100	00100010111011011001110000110101
4	0010	01010010001011101101100111000111000011
5	1010	00110101001000101110110110011100
6	0110	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 1 0 1
7	1110	10011100001101010010001011101101
8	0001	10001100100101100000011101111011
9	1001	10111000110010010110000001110111
10	0101	0111101110001100100101001000000111
11	1101	0111011110111000110010010100000
12	0011	00000111011110111000110010010110
13	1011	01100000011101111011100011001001
14	0111	10010110000001110111101110001100
15	1111	11001001011000000111011110111000

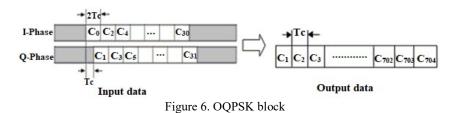
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Table 3. Symbol-to-Chip

In this block each data symbol of 4 bits are mapped to 32 bit chip PN sequence as prescribed in the ZigBee standard. The output which has come from bit-to-symbol as taken input of symbol-to chip. They are mapping and converting the output of chip as 704. The process of mapping is presented in the DSSS sequence for mapping is presented at Table.

4.4. **O-QPSK**

OQPSK modulator is the improved version of QPSK. The Chip sequences representing each data symbol are modulated on to the carrier using OQPSK with half sine pulse shaping. The fundamental OQPSK method is to sum the in-phase signal delayed by half a cycle is order to avoid the sudden phase shift change. It will never jump more than 90 degree. But QPSK will jump 180 degree. So, we cause band noise.



Each data symbol is represented by 32 bit chip sequence which increases the chip rate by 32 times of symbol rate, and produces a 2 Mbps (1024) DSSS signal. To perform offset between I-phase and Q-phase data stream, the Q-phase chip is delayed by chip period(Tc).

5. DESIGN METHODOLOGY

The behaviour of the Zigbee digital transmitter can be modelled using Verilog through Xilinx ISE. The VHDL module for each transmitter can be combined, then synthesized, simulated, and implemented on Spartan3E FPGA.

The input data comprise 22 symbols. Each data symbol from the bit-to-symbol block is append onto a 32-chip PN sequence using the DSSS method. The output data are 704 chips in total with the frequency of 2 MHz. The numbers of chips produced are based on [88 bits/4] symbols x 32 = 704 chips Based on this equation, each even chip of output data is registered as C0, C2 C704, and each odd chip is registered as C1, C3 ...C703, which is totally 352 chips each for Iphase and Q-phase.

6. SIMULATION RESULT

6.1. TOP LEVEL MODULE SIMULATION RESULT

The above input signal is applied to the ZigBee Transmitter for IOT Wireless Device. input enable,clk,rst,data in;

wire [7:0]crc out;

wire[3:0]sym1,sym2,sym3,sym4,sym5,sym6,sym7,sym8,sym9,sym10,sym11,sym12,sym13,sym1 4,sym15,sym16,sym17,sym18,sym19,sym20,sym21,sym22; it takes bits as the input and produces symbols as the output.

wire[31:0]c1,c2,c3,c4,c5,c6,c7,c8,c9,c10,c11,c12,c13,c14,c15,c16,c17,c18,c19,c20,c21,c22; it gives the chip as the output.

		2/101/97/18
Name	Value	1,000 ns 1,500 ns 2,000 ns 2,500 ns
🔓 enable	1	
🔓 cik	1	
🔓 rst	0	
🔓 data_in	1	
្រៃ final_out	1	
▶ 🍓 crc_out[7:0]	01010000	
🕨 👹 sym1[3:0]	1010	/11/01/00/11/01/00/00/1111/10/10/ 1010 /01/00/00/0000 /11/
▶ 🔩 sym2[3:0]	0000	/11/01/01/01/01/10/10/1101 /01/10/01/01/0000 /10/01/01/0101/00/
🕨 😽 sym3(3:0)	1010	/11/01/00/11/01/00/00/1111/10/10/ 1010 /01/00/00/0000 /11/
🕨 式 sym4[3:0]	0000	/11/01/01/01/01/10/10/1101 /01/10/01/01/0000 /10/01/01/0101/00/
🕨 😽 sym5(3:0)	1010	/11/01/00/11/01/00/00/1111/10/10/ 1010 /01/00/00/0000 /11/
▶ 式 sym6[3:0]	0000	/11/01/01/01/01/10/10/1101 /01/10/01/01/0000 /10/01/01/0101/00/
▶ 🏹 sym7[3:0]	1010	<u>11 01 00 11 01 00 00 1111 10 10 10 01 00 00</u>
▶ 🔣 sym8[3:0]	0000	
▶ 🔣 sym9[3:0]	1010	1101001101000011111010
▶ 駴 sym10[3:0]	0000	(11, (11, (01, (01, (01, (01, (01, (01,
		X1: 2,161.454 ns

Figure 7. Top level Zigbee Transmitter

From the simulation result the output signal of ZigBee Transmitter for IOT Wireless Device. Output: final out;

it gives the pulse shaping.

6.2. INDIVIDUAL BLOCKS SIMULATION RESULTS

The individual blocks simulation results are given below:

Name	Value		200 r	s	400 ns	600 ns	800 ns	1,000 r
la enable	1			<u></u>				
l clk	1							-
L rst	1							
1 data_in	0							
crc_out[1:8]	11110011	00000 1	1100	11 X		0000000		
Iength[31:0]	00000000000				000000000000000000000000000000000000000	00000000 1000		
initial_state[7:0	10010001				100 1000	1		
▶ 📑 tap_coefficient	11001111				1100111	1		
		X1: 242.736 ns						

Figure 8. Cyclic Redudancy Check

					271.	704 ns			
Name	Value			200 ns		300 ns	400 ns	500 ns	600 ns 700
🕨 式 sym10[3:0]	0111	0000	\langle				0111		
🕨 式 sym11[3:0]	1000	0000					1000		
▶ 式 sym12[3:0]	0011	0000					0011		
🕨 式 sym13[3:0]	0100	0000					0100		
🕨 式 sym14[3:0]	0111	0000					0111		
🕨 式 sym15[3:0]	0101	0000					0101		
🕨 式 sym16[3:0]	0101	0000					0101		
🕨 式 sym17[3:0]	1010	0000	(10	po X			1010	0	
🕨 式 sym18[3:0]	1001	0000					1001		
🕨 式 sym19[3:0]	0110	0000					0110		
▶ 🔩 sym20[3:0]	0101	0000					0101		
▶ 式 sym21[3:0]	0001	0000	00	10 🔨			000	1	
▶ 📲 sym22[3:0]	0100	0000					0100		
🔚 clk	1								
16 rst	0								
🕨 📷 din[87:0]	00000010001	0000000	00110	0000001000	1 10 10	10100001101111000	1010111100000110	1000111010101011	0 10 100 10 1 100 10 1000 10 .
		X1: 271.	704 ns						

Figure 9. Bit-to-Symbol

Objects ↔ □ & ×	Ð			412.478708333 ms
Simulation Objects for t				
16 16 16 16 »	P	Name	Value	0 ms 200 ms 4 <mark>0</mark> 0 ms 600 ms 800 ms 1,000 ms
	8	▶ 📑 sym5[3:0]	1010	1010
Object Name ^	, , , , , , , , , , , , , , , , , , , ,	sym6[3:0]	0100	0 000
⊳ 📲 c1[31:0]		sym7[3:0]	1001	1001
▷ → c2[31:0]	ă	sym8(3:0)	1000	1000
C3[31:0]	-	sym9(3:0)	0100	0100
▷ → c4[31:0] ▷ → c5[31:0]	12	sym10[3:0]	0101	0101
c6[31:0]	T	> sym11[3:0]	0111	0111
⊳ 💐 c7[31:0]		sym12[3:0]	1001	1001
⊳ 式 c8[31:0]	5			0011
⊳ 💑 c9[31:0]	1	▶ 📑 sym13[3:0]	0011	
▷ → c10[31:0] ▷ → c11[31:0]	<u></u>	▶ 📑 sym14[3:0]	0101	0101
c11[31:0]		▶ 📑 sym15[3:0]	0011	0011
c13[31:0]	21	▶ 📑 sym16[3:0]	0111	0111
⊳ 式 c14[31:0]		▶ 📑 sym17[3:0]	1001	101
⊳ 式 c15[31:0]	: ==	▶ 剩 sym18[3:0]	0100	¢000
c16[31:0]		▶ 📑 sym19[3:0]	0010	0010
c17[31:0]		sym20[3:0]	1001	1001
c18[31:0]		sym21[3:0]	0111	0111
c20[31:0]		▶ 📑 sym22[3:0]	1011	1011
c21[31:0]				
▷ 20 c22[31:0]				X1: 412.478708333 ms
16 clk				

Figure 10. Symbol-to-Chip

		2.978290 us	
Name	Value	3 us 4 us	5 us 6 us
l <mark>u</mark> cik	1		
🔓 reset	1		
l <mark>la</mark> x	1		
l <mark>la</mark> y	1		
cnt[2:0]	101	000000000000000000000000000000000000000	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>
▶ 📑 x_x[1:0]	11		11
Carriers[3:0]	0011	0011001100)1)0)1)1)0)0)1)1
🕨 📷 y_y[1:0]	11		11
		· · · · · · · · · · · · · · · · · · ·	
		X1: 2.978290 us	

Figure 11. Offset Quadrature Phase Shift Keying Modulator

6.3. DESIGN SUMMARY

evice utilization summary:					
elected Device : 3s500eft256-5					
Number of Slices:	7	out	of	4656	0%
Number of Slice Flip Flops:	11	out	of	9312	0%
Number of 4 input LUTs:	12	out	of	9312	0%
Number of IOs:	4				
Number of bonded IOBs:	4	out	of	190	2%
Number of GCLKs:	1	out	of	24	48
artition Resource Summary:					
artition Resource Summary: No Partitions were found in this	design.				
	design.				
No Partitions were found in this	design.				
	design.				

7. CONCLUSION

This paper describes the design a wireless transmitter based on zigbee transmitter. In this five blocks such as CRC block, Bit-to-Symbol block, Symbol-to-Chip, OQPSK and Pulse shaping as a part of the ZigBee transmitter for 2.4 GHz frequency band. CRC was employed to detect the errors during transmission of data. The binary data was sent to CRC and CRC codes were generated. The output of CRC block was fed to Bit-to-Symbol block, where 88 bits were mapped into 22 symbols. The output of Bit-to-symbol block is fed to the symbol-to-chip block and output 704 Chips. The symbol-to-chip output is fed to OQPSK. The fundamental O- QPSK method is to sum the in-phase signal with a quadrature phase signal delayed by half a cycle in order to avoid the sudden phase shift change. The pulse shaping block will detect the ISI(Inter-Symbol-Interference).

ZigBee is the ideal choice of protocol for home automation and smart energy, because different ZigBee devices can be connected. As more ZigBee devices are linked, communication paths between devices multiply, eliminating the risk of single-point signal failure. ZigBee is an open, global standard for wireless communication between IoT devices. With ZigBee, IoT devices can easily be connected to other IoT devices. The ZigBee protocol is secure and stable, which is one of the reasons why it has become one of the world's most widely adopted protocols.

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