IMPLEMENTATION OF LOW POWER ADIABATIC SRAM

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ABSTRACT

In the featuring VLSI era, compact electronic devices are popular. The reliability and durability of such compact devices relies on low power utilization. The purpose of this project was to implement a low power adiabatic Static Random Access Memory (SRAM), with the following objectives - To reduce the power waste by means of stepwise charging using tank capacitors which is an adiabatic way of generating power clock. This method is capable of recuperating the electrical energy back to the source. Further to examine the Static Noise Margin (SNM) – a parameter which gives detailed information about the cell stability – in contrast with conventional 6T, 7T and 8T topologies of SRAM under 180 nm technology. Finally, SNM variations with respect to process parameters are also discussed. All the implementations and analysis were made using CADENCE tool and MATLAB tool.

KEYWORDS

SRAM, Adiabatic, CMOS, Stepwise Charging, SNM and Process variations.

1. INTRODUCTION

In the contemporary times, in ubiquity of device minimization is in demand – one of the prime mottos of low power VLSI. As per Moore's law, in every 18 months the number of transistors gets doubled in an Integrated Circuit (IC) [1]. Because of this, the small sized devices face durability and reliability issues. Main reason for these kinds of issue, is the power dissipation. Usually in a CMOS IC, half of the power consumed is dissipated in the form of heat. In order to overcome this, heat sinks were introduced which increases the area of the device, failing to serve the prime motto.

The main sources of power dissipation in a CMOS circuit are static power dissipation – due to leakage currents during inactive states, dynamic power dissipation – due charging and discharging of capacitances and short circuit power dissipation – due to slow rise and fall times. The total power dissipation is the summation of all the three sources. The majority is due to dynamic switching activity - to reduce this, various low power design techniques were used. Many of them were based on clock signals and complement form, which are outdated for the present day technologies. So, the researches came across a new class of logic called "Adiabatic logic". This logic is one of the finest low power design technique.

Usually in a circuit, during the charging and discharging of capacitor half the energy which is given by $0.5CV^2$ is wasted, in other words all the energy drawn isn't converted into useful work. But in case of adiabatic logic the energy is recuperated back to the source without being

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discharged to the ground. Adiabatic logic also uses the method of slow charging instead of fast charging to reduce the power waste.

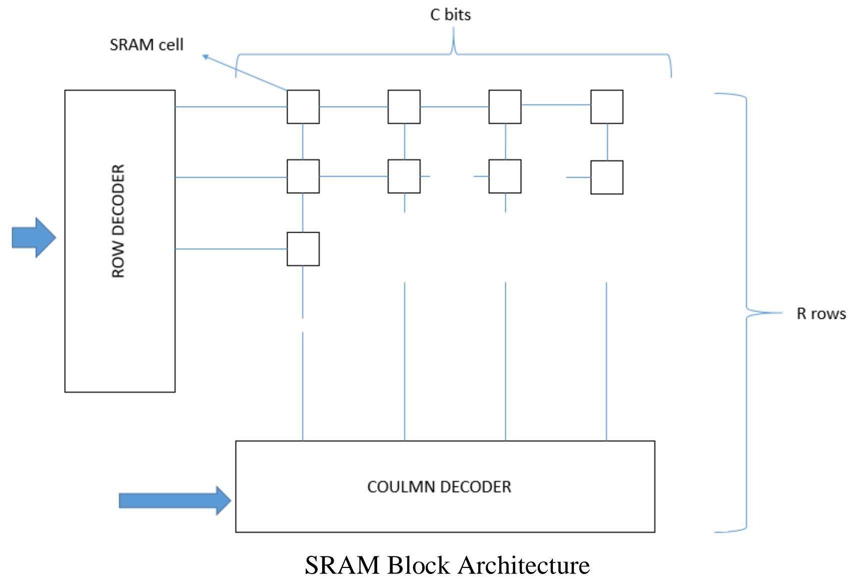
2 LITERATURE SURVEY

[1] This book provides a detailed information on MOS – transistors, static and dynamic operating fundamentals, relevant topics on CMOS low power circuit design. It also provides information about the design methodologies in VLSI and in-depth presentation of semiconductor memory [1]. It also offers BiCMOS digital circuit design. The book also covers topics such as chip I/O design, Design for manufacturability and testability [1]. From this book we understood the basics of a semiconductor memory and adiabatic circuits. [2] It gives an overview of SRAM circuit design and testing. It offers a detailed understanding for the readers on topics of cell stability and its testing techniques. This book helped me in understanding how to measure the cell stability and the factors affecting the cell stability. [3] The document provided a detailed description of SRAM which was used to design an 8 X 8 SRAM IC. SRAM IC was developed using the CDS IC446, cadence IC design environment. The design was based on the AMI 0.6-micron process [3]. This report assisted me in designing the peripheral circuits required for a single read and write operation of AN SRAM cell. It also provided an idea to build an array of required size. [4]. It furnishes a systematic and a complete view of SRAM bit cell circuits, architectures, and design and analysis techniques [4]. This book is indeed a great help for VLSI design engineers to design SRAM and cache architecture reasonably [4]. This book aided me in understanding the theoretical background of all the peripherals of an SRAM and also came across the different topologies of low power SRAMs and their classifications based on the robustness. [5] It aids the readers with the benefits of adiabatic logic and generation of power clocks to reduce the energy consumption. This book also deals with the basic fundamentals and the future trends. With the help of this book the concept of adiabatic logic was much clearer. [6] It was mainly based on the power clock generation using step charging concept. The authors stated that their work wasn't compared with any of their referral records. The concept was to recover the energy in an efficient manner through step charging the concerned circuit. [7] The author proposed a new and stable way to generate a power clock using asymmetric tank capacitors. Later the same concept was applied to develop a low power SRAM. [8] In this paper a design procedure for driver to minimize power [8]. [9] In this paper, the design and functionality of a novel ultra-low power stable SRAM cell is discussed which addresses power minimization as well as stability against large variation in temperature which is ideally suited for space applications. This paper explores a novel circuit level approach to reduce power in the SRAM cell during active mode of operation as well as standby mode by incorporating NMOS-PMOS pair in each pull down path. [10] In this paper an analytical method to analyse the stepwise charging of adiabatic circuits was suggested by the authors. From this paper a detailed study on stepwise charging is obtained.

3 SRAM CELL DESIGN AND OPERATION

3.1 SRAM BLOCK ASSEMBLY

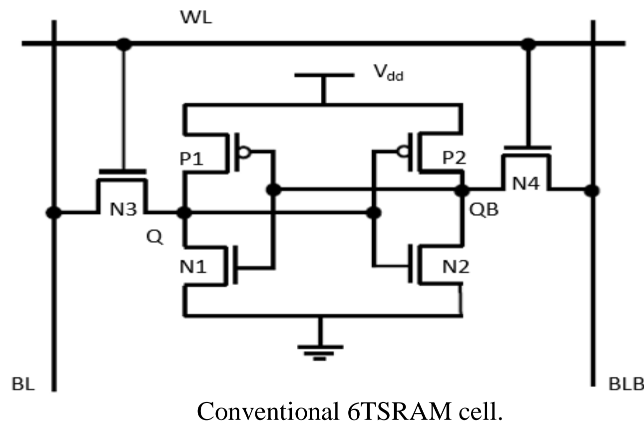
The following is an example of a basic SRAM block. It consists of RxC array of SRAM cells, where R is the number of rows and C is the number of bits. With the help of a row decoder, a particular row of interest can be selected, this is possible by decoding the address to select one of the word lines W1 to WN. Usually the SRAM arrangement is either bit aligned or word aligned. If it is bit aligned then each address retrieves a single bit, else retrieves a word of *s* bits where *s* includes 8, 16, 32 or 64. A single sense amplifier can be distributed to more than one column with the assistance of a column decoder.



SRAM Block Architecture

3.2 6T SRAM

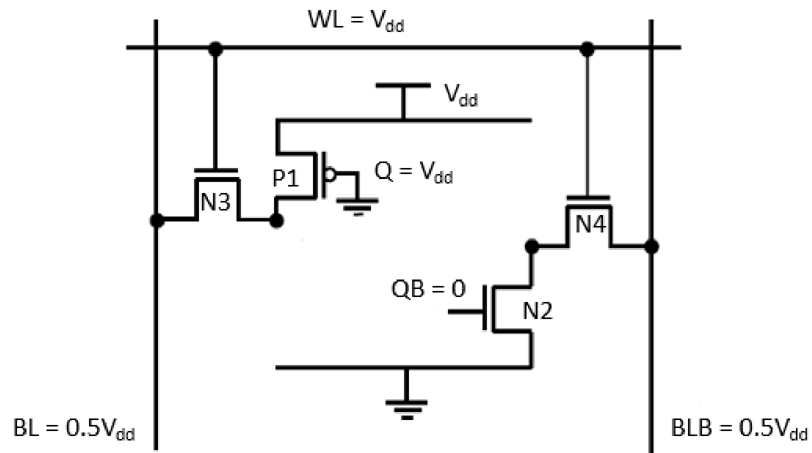
The conventional circuit of one bit SRAM cell consists of 6 transistors or MOSFETs, the arrangement consists of two inverters which are connected back to back in a cross manner (i.e., the output of 1st inverter is connected to the input to the 2nd and vice versa). It is same as a flip flop - a b is table element. In a SRAM cell not only the data bit but its compliment is also stored. The data bit is stored and retrieved from the bit cell with the help of word line (WL) and bit lines (BL and BLB). The transistors (P1, P2), (N1, N2) and (N3, N4) are load, driver and access transistors respectively. The word line is connected to the gate of the access transistor and the bit lines carry the bit voltage that is to be stored in the cell.



Conventional 6TSRAM cell.

A. READ OPERATION

1. Precharge the bitlines up to $0.5V_{dd}$ using a precharge circuitry.
2. For the read operation to begin the word line goes high.
3. Based on the data stored at node Q charging and discharging of the capacitances happen. If Q=0 then the charge is discharged else it is charged.
4. The sense amplifier senses the data bit by converting the differential signal to logic level.
5. Word line is made low.

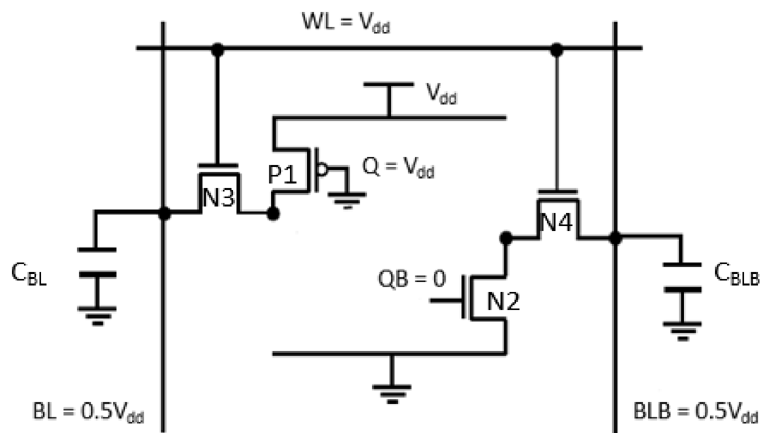


6T SRAM during read operation.

During read operation with Q = V_{dd}, the corresponding schematic diagram is as shown in the figure. When the voltage at node QB reaches the threshold voltage of the NMOS- N1, the voltage at Q starts to decrease and the renewal action of the coupled inverter will force the bit stored to overturn.

B. WRITE OPERATION

1. Initially the word line is made low.
2. Precharge the bitlines up to V_{dd} /2 using precharge circuitry.
3. For the write operation the bit lines are connected from the V_{dd}
4. Word line is made high.
5. The data to be written is placed on the bitlines (BL and BLB)
6. Once the Q and QB overturns its state, word line is made low.



6T SRAM during write operation.

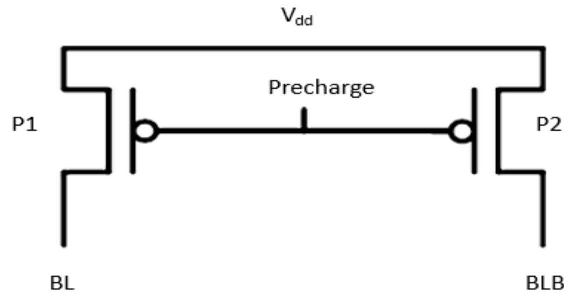
3.3 PERIPHERAL CIRCUITS

For the read and write operation of SRAM peripheral circuits such as precharge circuit, sense amplifier, mux for BLB and mux for BL are necessary.

A. PRECHARGE CIRCUIT

It consists of 2 PMOSFETs, the sources of the MOSFETs are connected to the supply voltage - for the project a voltage=2.5V was preferred. The gates of the transistors are connected to the precharge control stimuli. The drains are connected to the bitlines (BL and BLB) which as shown in the figure.

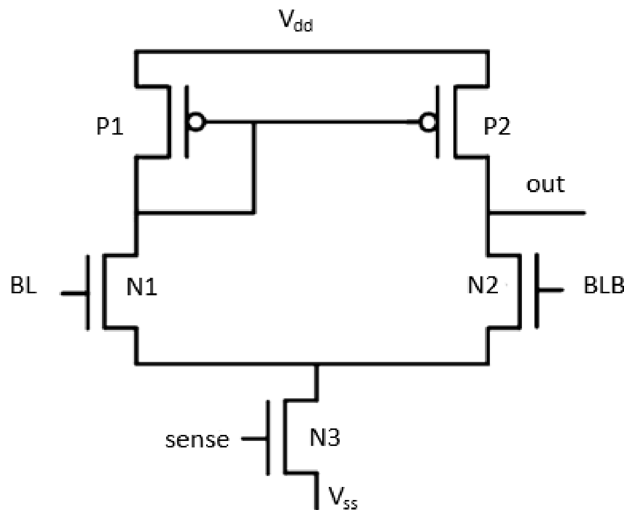
The purpose of using this circuit is to maintain the uniformity of the bitlines before the read and write operation. The bitlines are pulled to V_{dd}.



Precharge circuit

B. SENSE AMPLIFIER

It is the most important circuit during the read phase, it is used to sense the bit voltage by converting the differential signal on BL and BLB to a digital signal. A current mirror differential sense amplifier [2] was used for the project. The configuration consists of 2 PMOSFETs and 3 NMOSFETs which are in contact accordingly, as seen in the figure.



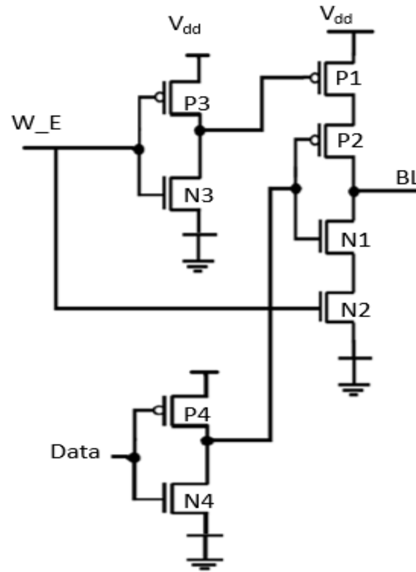
Current mirror differential sense amplifier

C. MUX FOR BITLINES

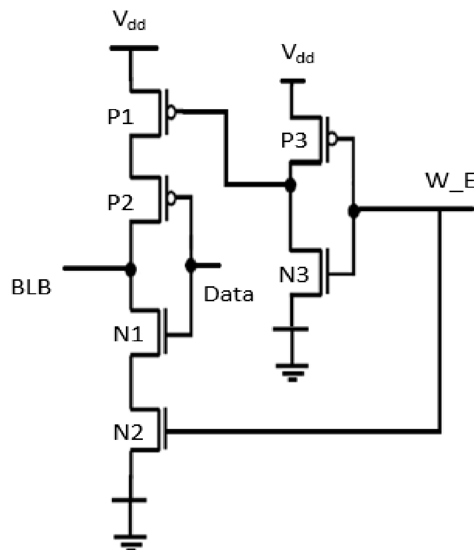
It is also an important peripheral circuit, which is engaged in the write phase. The following figures represent the mux circuits for BL and BLB respectively. The data is not written into the cell unless and until the W_E (Write Enable) signal is made high [3]. The right mux is connected

to BLB and left mux is connected to BL, it can be connected the other way around also. The main difference between the left mux and right mux is the inverter which is used to invert the data. The data and inverted data are sent to the bitlines BL and BLB.

The following figures shows the detailed connection of all the transistors forming the multiplexers.



Mux for bit line BL

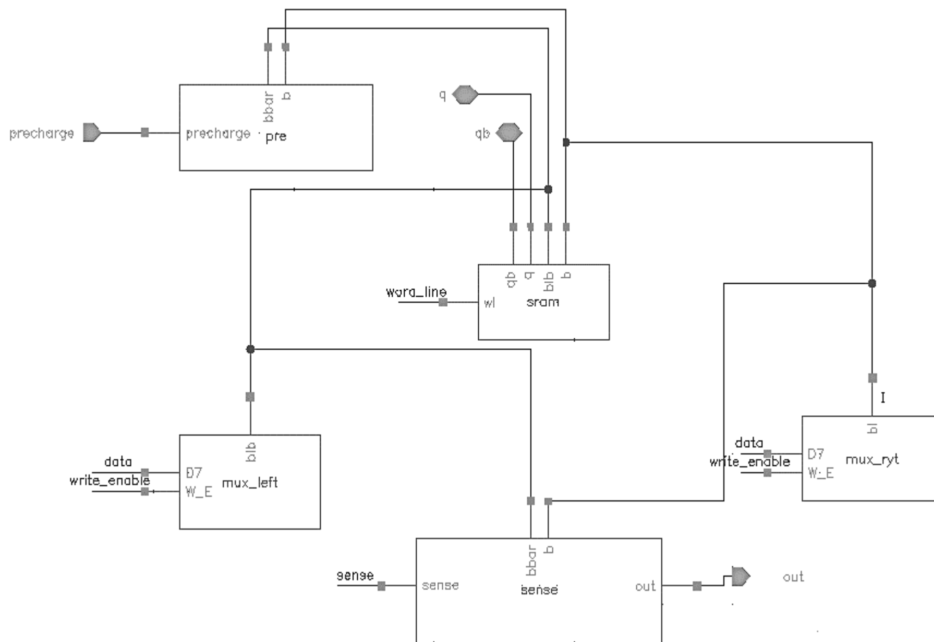


Mux for the bit line BLB.

3.4 SINGLE READ AND WRITE SRAM CELL

Merging all the above peripheral circuits with SRAM, single read and write cell is configured. The following figure shows the configuration, the stimuli given to the circuit are as follows 1-precharge, 2-data (bit 0 or 1), 3-write_enable (it gives the authority to write the data into the cell),

4-sense (it validates the bit which is stored in the cell) and 5-word_line (resolves at which address the bit is registered) [3].



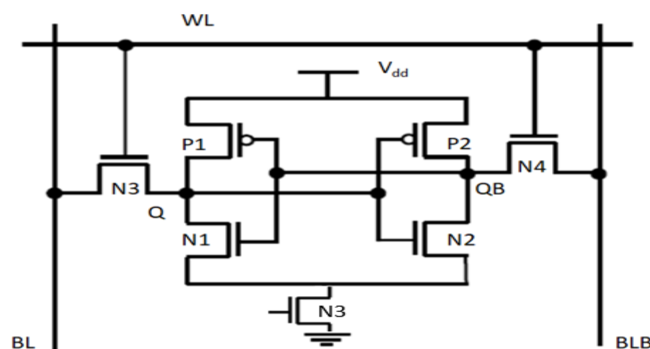
Single read and write SRAM cell.

4 Various Configurations Of SRAM

There are two more configurations that are discussed in this project, they are 7T and 8T SRAM. Concentrating on the fundamental factors of the low power VLSI design, these configurations were depicted to reduce the power consumption, improve the cell stability, efficiency and the performance.

4.1 7T SRAM

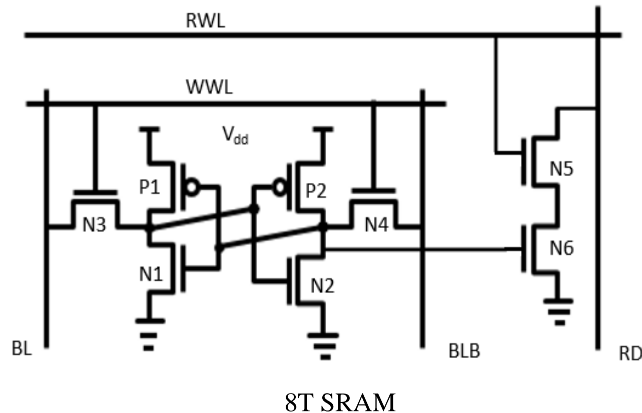
The figure below shows the configuration of the 7T SRAM, it was designed to reduce the power consumption and to have a better read accessed SNM. It is similar to the 6T structure with an extra NMOS whose gate is connected to the word line. The read and write operations are similar as that of 6T SRAM.



7T SRAM

4.2 8T SRAM

The structure slightly varies from 6T and 7T, because it uses control signals such as RWL (Read Word Line) and RD (Read signal). It is same as that of 6T SRAM cell with two extra transistors connected to the control signal RD which is used only and mainly during the read operation along with RWL=1. During write operation BL and BLB along with WWL =1 is used.



8T SRAM

5 ADIABATIC LOGIC

Adiabatic is a Greek word which signifies that it is impassable to heat, in other words no trade of heat between a system and the neighbouring environment. The fundamentals of adiabatic logic are as follows

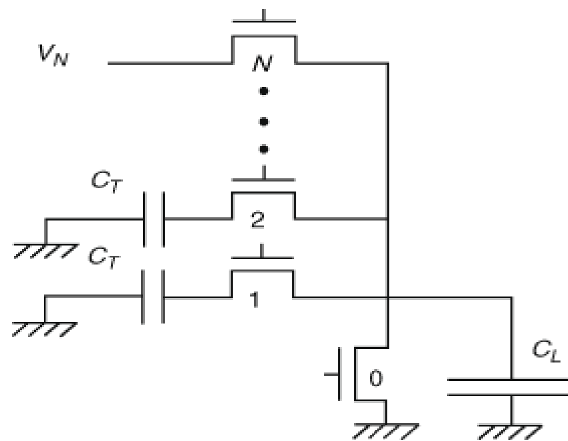
1. When there is no voltage between the nodes, the switches are ON.
2. The switches are OFF, when there no current run across the nodes.
3. Use an active element that is able to recuperate the energy in the form of charge.

All the above fundamentals are attained by a time varying current source instead of a voltage source. Customarily, the designers underplay with the events, the node capacitances or the voltage swings to reduce the power waste.

Adiabatic switching ciruits require non-constant, non-standard power supply with time-varying voltage. This power supply is known as “Pulsed power supplies” or “power clock”. These power supplies use circuit components capable of restoring the energ. Inverting the current supply causes the energy to flow from the load capacitance back into the power supply. So, the power supplies must be designed to retrieve the energy fed back to it.

5.1 REALIZATION OF POWER CLOCK

The following circuit is capable of creating a power clock by charging the load capacitor in a stepwise manner using tank capacitors, the steps may vary from 2 to n-1, the switches 1 to N are closed in an incresing order.The charge at the load capacitor varies from 0 to V_{dd} insteps of 0 to V_{dd}/n, V_{dd}/n to $2V_{dd}/n$ and so on. The overhead limits the practical number of steps to 10, but larger the number of steps greater is the reduction in power waste.



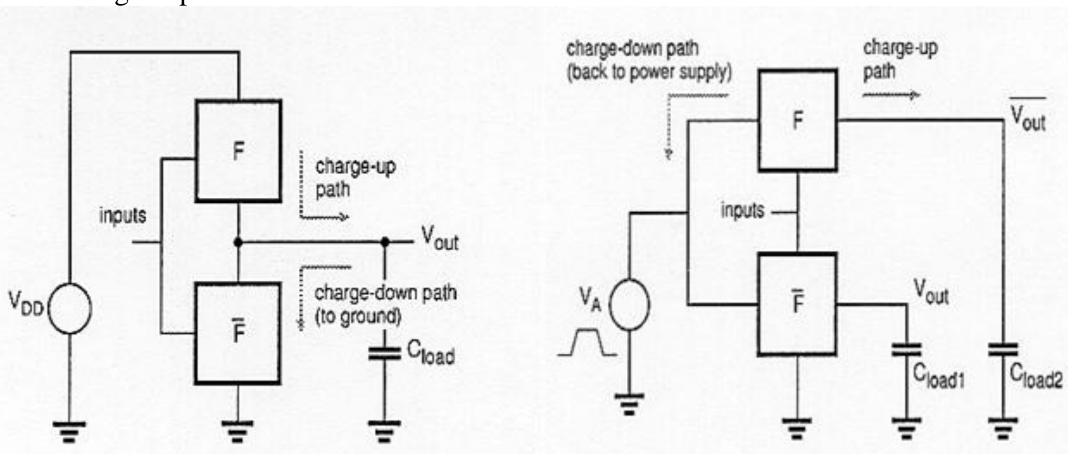
Stepwise Charging using tank capacitors

5.2 REALIZATION OF ADIABATIC GATES

Adiabatic logic can be realized for any conventional CMOS logic just by replacing each pMOS and nMOS devices in the pull-up and pull-down networks respectively with interdependent transmission gates (T-gates).

As all the stimuli must be available in complementary form, both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitances. We can use expanded pull-up and pull-down networks to drive true and inverse output respectively.

Replace DC source V_{dd} by a pulse power supply with varying voltage to allow adiabatic operation.The pulsed power supply or the power clock is capable of recovering the energy backto source reducing the power waste.



Conventional and Adiabatic Logic

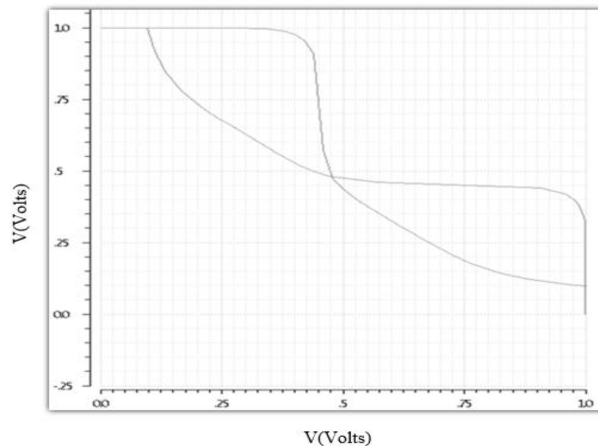
6 STATIC NOISE MARGIN

Static Noise Margin (SNM) is a stability metric of an SRAM cell interpreted by the Voltage Transfer Characteristics (VTC) of the back to back connected inverters of the SRAM. The measurements can be made for read accessed, write accessed and stable/hold SRAMs. On the whole the Noise Margin is an acceptable signal by the device still maintaining the correctness of

the operation. If it is a dc or static signal, then it lasts long affecting the correctness. It can be controlled by latching the signal. It is generally used to find a weak SRAM cell by adding a noise voltage source which is as shown in the figure below.

A. READ ACCESSED SNM (RSNM)

Usually the RSNM presents the worst case SNM of the SRAM cell. RSNM is given by side length of the largest square inscribed inside the lobes of the butterfly curve, which is formed by the VTCs of the inverter of the SRAM. This approach was depicted by Hill in the year 1968[2]. This method is for ideal SRAMs, but in real the squares inscribed aren't equal, so the side length of a smaller square is considered. The nature of graph is as shown below



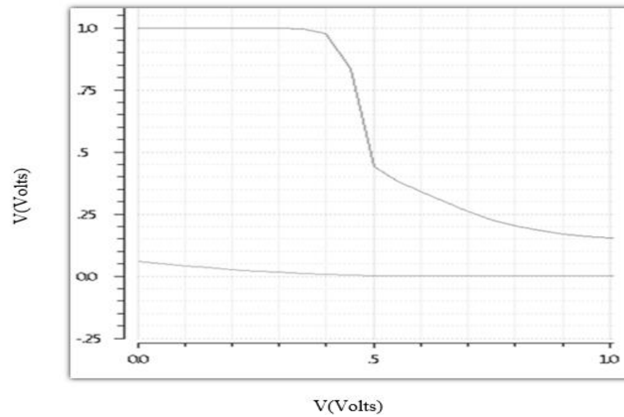
Nature of graph of RSNM

PROCEDURE TO FIND THE RSNM

Connect a noise voltage X=0 at the output of one of the inverters. Both the bitlines are precharged to $V_{dd}/2$ and the word line is enabled. Plot the VTC of both the inverters to form a butterfly plot. Now fit a largest square into the eye lobes of the butterfly plot. Higher the value of RSNM better the read stability of the SRAM cell.

B. Write Accessed SNM (WSNM)

WSNM depicts the write stability of the SRAM cell. It is given by side length of the largest square inscribed between the VTC of the inverters of SRAM cell. The nature of graph is as shown below



Nature of graph of WSNM

PROCEDURE TO FIND WSNM

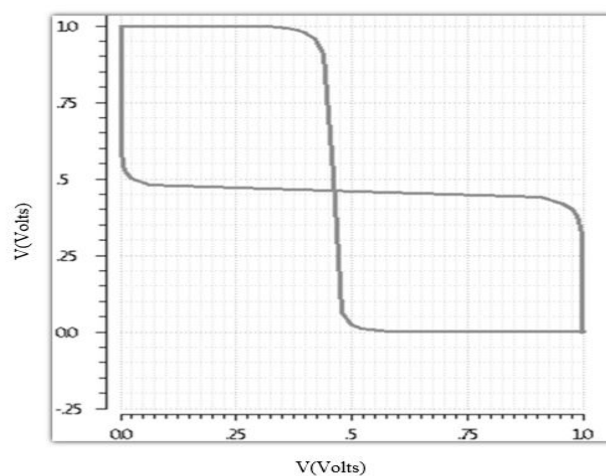
The two inverters of the SRAM are broken apart to find the WSNM, the bitlines BL and BLB consists of the bit and its complement (say 0 and 1 or 1 and 0) respectively. Once the word line is enabled, plot the VTC of the both inverters. Now fit a largest square in the region between the characteristic curves.

C. Hold SNM

It depicts the stability of the cell in standby mode or idle (i.e. when it is holding a value). The nature of the graph of hold SNM is same as that of read accessed SNM. It is a perfect butterfly plot.

PROCEDURE TO FIND HOLD SNM

The procedure is same as that of RSNM, except for the word line to be disabled.



Nature of graph of Hold SNM.

6.1 SRAM SNM AND PROCESS PARAMETER VARIATIONS

To get an intense intuition of the reactivity of SNM due to process variables - such as temperature, supply voltage, Cell Ratio (CR) and Pull-up Ratio (PR) - simulations are performed by varying the process variables.

Cell Ratio is the ratio of W/L of driver transistor to the W/L of the access transistor. It is mainly concerned during the read operation. CR is directly proportional to SNM.

$$\mathrm{CR} = \frac{(\mathrm{W/L})\mathrm{driver}}{(\mathrm{W/L})\mathrm{access}}$$

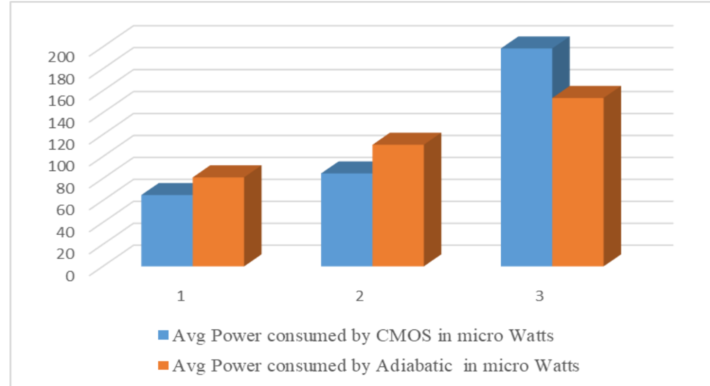
Pull-up Ratio is the ratio of W/L of load to W/L of access transistors. It is of concern during the write operation. SNM increases as it increases.

$$\mathrm{PR} = \frac{(\mathrm{W/L})\mathrm{load}}{(\mathrm{W/L})\mathrm{access}}$$

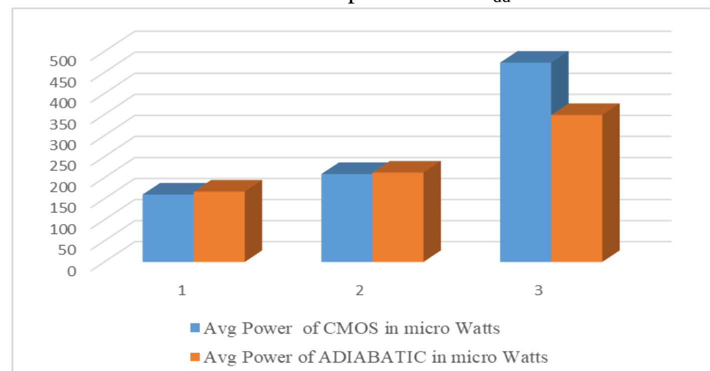
The dependence of SNM on process variables is clearly seen in the results and discussion chapter of the report.

7 RESULTS AND DISCUSSION

The following graphs depict the average power consumed during read write operation by CMOS and Adiabatic SRAM topologies, under 180nm technology with voltages 1.8 V and 2.5 Volts.



Power consumption when V_{dd}=1.8 V



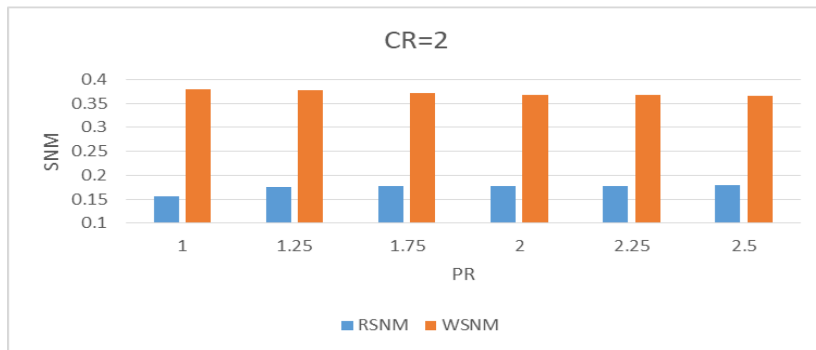
Power consumption when V_{dd}=2.5V

7.1 INFLUENCE OF PROCESS PARAMETERS ON SNM OF CMOS SRAM.

With different process variations such as temperature, supply voltage, CR and PR the SNM calculations were made in all the modes.

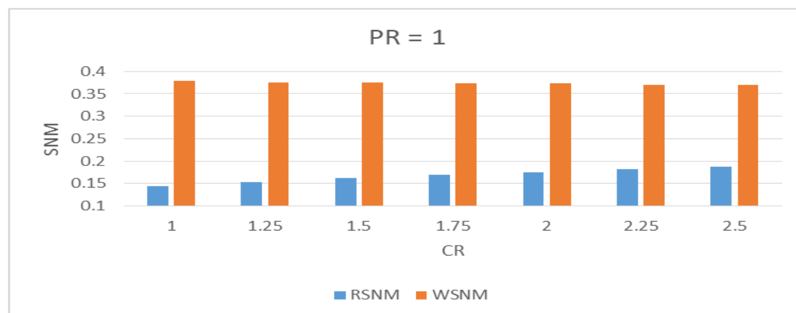
A. 6T SRAM

Variation of Pull-up Ratio keeping the Cell ratio constant i.e. equal to 2 is as shown in the figure. The WSNM varies accordingly with the PR from 1 to 2.5 with equal steps of 0.25 but the RSNM does not vary.



Contrast of RSNM and WSNM of 6T SRAM with CR=2

Now keeping the PR=1 and varying the CR from 1 to 2.5 in steps of 0.25 at a time we observe that, RSNM varies accordingly with CR and WSNM remains almost constant.



Contrast of RSNM and WSNM of 6T SRAM with PR=1

HOLD (Temp=27)		HOLD (Vdd=1)	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.3145	-140	0.2365
1.45	0.255	-70	0.225
1.8	0.2873	0	0.22
2.15	0.2355	70	0.213
2.5	0.216	140	0.2083
READ (Temp=27)		READ (Vdd=1)	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.195	-140	0.183
1.45	0.225	-70	0.186
1.8	0.218	0	0.179
2.15	0.2075	70	0.17
2.5	0.2	140	0.163
WRITE (Temp =27)		WRITE (Vdd=1)	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.398	-140	0.375
1.45	0.39	-70	0.37
1.8	0.435	0	0.367
2.15	0.327	70	0.365
2.5	0.324	140	0.359

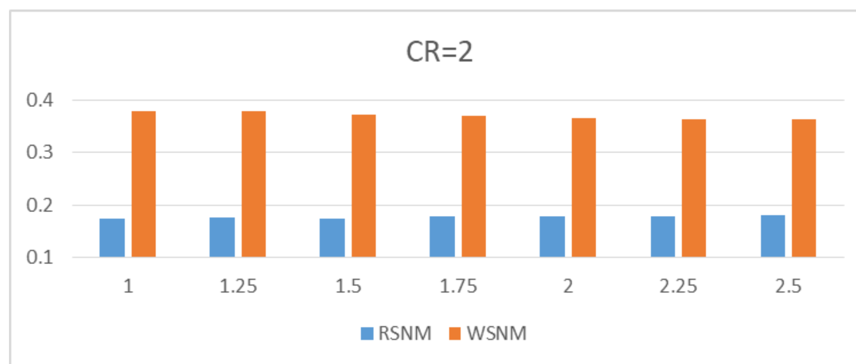
SNM values of 6T SRAM in all the modes

The variation of RSNM with respect to temperature and power supply is observed now, variation in temperature ranges from -140 to 140 degree Celsius with V_{dd} = 1 V and supply voltage from 1.1 to 2.5 in 5 steps at room temperature equal to 27 degree Celsius.

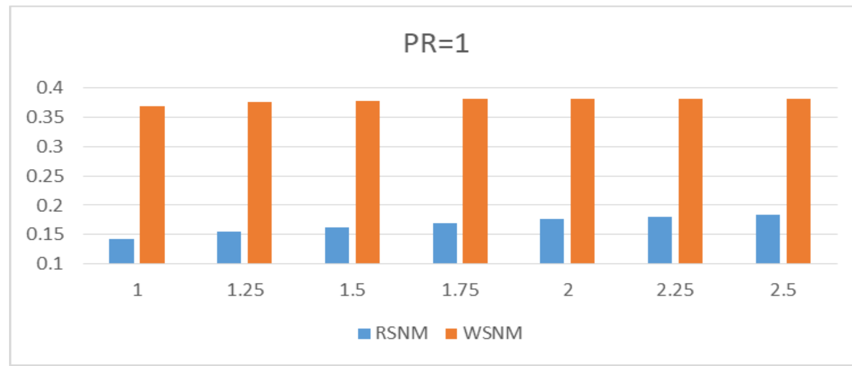
From the above graph we see that the RSNM decreases as the temperature increases. Hence the RSNM is more stable at less temperature. More the SNM more is the stability. From the table we observe that the RSNM, WSNM and Hold SNM values of 6T SRAM decreases as the voltage and temperature increases.

B. 7T SRAM

Variation of RSNM and WSNM according the PR and CR values is seen in the subsequent graphs. The behaviour is same as that of 6T SRAM.



Contrast of RSNM and WSNM of 7T SRAM with CR=2



Contrast of RSNM and WSNM of 7T SRAM with PR=1

The WSNM varies when CR is constant and remains the same for constant PR.

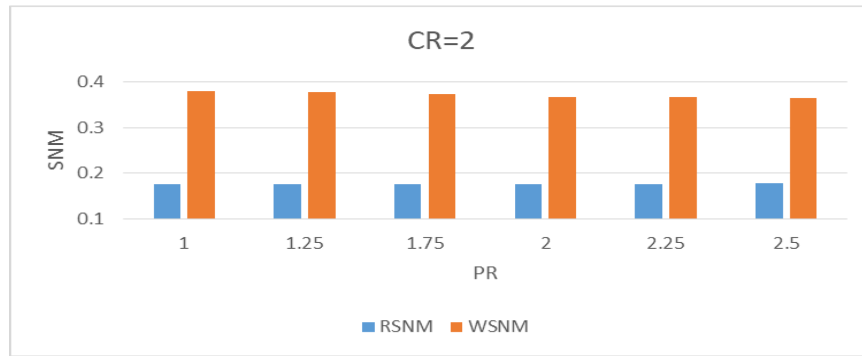
The variation of SNM with respective to temperature and supply voltage is given by the table 2

READ		READ	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.193	-140	0.188
1.45	0.28	-70	0.178
1.8	0.25	0	0.176
2.15	0.205	70	0.165
2.5	0.195	140	0.155
HOLD		HOLD	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.307	-140	0.34
1.45	0.28	-70	0.335
1.8	0.25	0	0.18
2.15	0.232	70	0.3
2.5	0.215	140	0.295
WRITE		WRITE	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.365	-140	0.385
1.45	0.348	-70	0.383
1.8	0.338	0	0.38
2.15	0.32	70	0.375
2.5	0.305	140	0.37

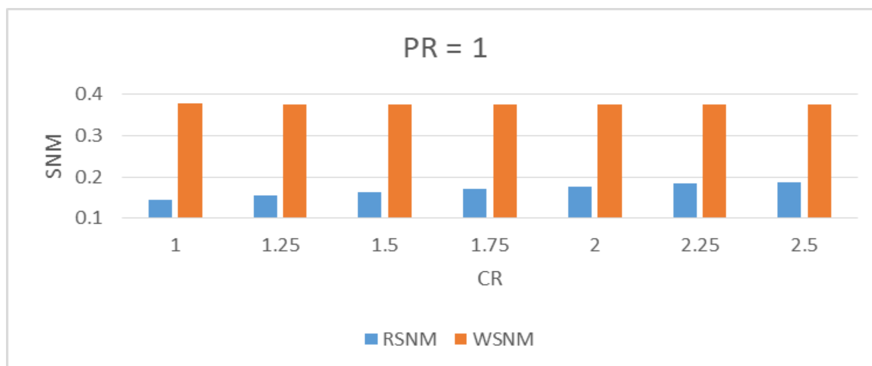
SNM values of 7T SRAM in all the modes

C. 8T SRAM

The SNM results of 8T SRAM are discussed below.



Variation of RSNM and WSNM of 8T SRAM with CR=2



Variation of RSNM and WSNM of 8T SRAM with PR=1

The behaviour of SNM in all the modes with respect to the process parameters such as supply voltage and temperature.

READ		READ	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.198	-140	0.195
1.45	0.223	-70	0.184
1.8	0.218	0	0.1745
2.15	0.205	70	0.168
2.5	0.195	140	0.16
HOLD		HOLD	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.307	-140	0.34
1.45	0.28	-70	0.335
1.8	0.25	0	0.18
2.15	0.232	70	0.3
2.5	0.215	140	0.295
WRITE		WRITE	
Vdd (V)	SNM (V)	Temp (°C)	SNM (V)
1.1	0.365	-140	0.385
1.45	0.348	-70	0.383
1.8	0.338	0	0.38
2.15	0.32	70	0.375
2.5	0.305	140	0.37

SNM values of 8T SRAM in all the modes.

CONCLUSION

A low power adiabatic SRAM has been implemented using the stepwise charging process with the help of tank capacitors. From the results and discussion, we conclude that the stepwise charging method is appropriate for 8T cell, because the power consumption was reduced by 22.72 and 26.27 percent for V_{dd}=1.8V and V_{dd}=2.5 V respectively.

From the detailed analysis of RSNM, WSNM and Hold SNM of 6T, 7T and 8T SRAM cells we conclude that the stability of 6T SRAM and 8T SRAM cell is better than the 7T SRAM cell. Hence 8T cell is more appropriate for low power applications with good SNM at different process variations. Thus from all the implementations and analysis, the project concludes that the 8T SRAM cell with step charging method is the low power adiabatic SRAM.

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