PERFORMANCE EVALUATION OF LOW POWER CARRY SAVE ADDER FOR VLSI APPLICATIONS

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ABSTRACT

This report examines the subject of sub threshold leakage on carry save adder. When the gate to source voltage reduces to the threshold voltage at that place is yet some amount of current flow in the circuit and that is undesired. As the process technology advancing much rapidly the threshold voltage of MOS devices reduces very drastically, and it must be applied in lower power devices since it contributes to low amount of leakage current which confine increases the power consumption of the devices. Adders are the basic building blocks for any digital circuit design and used in almost all arithmetic's. The CSA proves efficient adders due to its quick and precise computations. Hence this paper performs sub threshold analysis on CSA and the scrutinize results that the total average power is around 4.93µW, the propagation delay for complete operation is 16.3ns and since this design uses GDI cell so there is a reduction in area with 37%.

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KEYWORDS

Sub threshold Leakage, Gate Diffusion Input (GDI), Carry Save Adder (CSA), Leakage current, Transistor Modeling.

1. INTRODUCTION

Arithmetic circuits are basic building blocks of any digital IC design. The major offices such as summation, subtraction, multiplication, and variance are used oftentimes in an arithmetic and logic unit of any digital IC. Since the addition and multiplication are nearly shared similar functionality so it is possible to design adders which perform both the functions very efficiently [1]. A carry save adder (CSA) is distinguished from other types of adders by the fact that the carry bits and half-sum bits which result from each addition are not immediately combined or consolidated but instead are saved separately from each other for subsequent use in the next addition performed by the CSA, the inputs to which will comprise the saved carry and half-sum bits (the latter hereinafter referred to simply as "sum bits" for convenience) and the bits of an operand which is being added to, or in some instances being effectively subtracted from, the value jointly represented by these saved carry and sum bits.

Carry save adders commonly are employed in high-speed multipliers, where they generally are able to function more rapidly than "carry propagate" or "ripple carry" adders because a carry save adder does not completely perform the relatively time-consuming process of combining carries with sum bits between successive additions in the multiplication process but instead defers this task until the final cycle of the multiplying operation. This work design the CSA in such a manner that it should consume less silicon area and perform efficient operations; to achieve this the GDI methodology is used to design the 4-bit CSA. The subthreshold leakage of CSA is measured and optimized by adjusting the MOS process parameters such as oxide thickness, channel length/width, junction depth and so forth reduce the leakage current of the device [4]. The basic

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logical operation of 4-bit CSA can be realized by the following fig 1. By using CSA not only the focal ratio of the computation increases, but as well it sustains the power since the carry propagation is saved between previous and next state if generated any In this paper a 4-bit CSA is designed using GDI methodology and its performance is examined with respect to subthreshold leakage.

This work is organized in the following sections: Section 2 provides a necessary existing work related to the CSA circuit. This section also deals an existing work with its pros and cons. Section 3 details the architecture, including the CSA design and explication of results. Section 4 provides the comparative results based on prior work and section 5 their conclusion

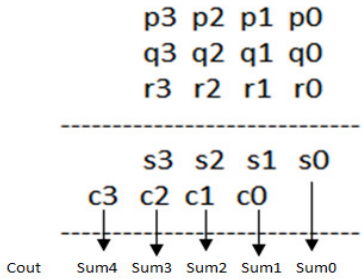

Fig. 1 Logical Operation of 4-Bit CSA

2. LITERATURE SURVEY

Tooraj Nikoubin [3] proposed three inputs xor/xnor circuit using a systematic cell design methodology (SCDM) in hybrid CMOS logic style. Their design shows, full swing and balanced outputs; even with supply voltage scaling they perform well and in the critical path they contain two transistors. It was shown that the proposed circuits exhibit 27% - 77% decrease in average energy delay product and also 26% - 32% improvement in the field.

Ramyanshu Datta [6] present a 4-to-2 CSA using dynamic logic and limited switch dynamic logic (LSDL) circuit family. The operation of the adder is improved as per the results. Further, they used a latching element which contains the ability of dynamic circuit. The LSDL methodology shows significant improvement with regard to power dissipation, leakage and area.

Adarsh Kumar Agarwal, S.Wairya [7] employed high speed and low power performance of single GDI adder, its speed performance is degraded when cascaded within a long chain because it is equivalent to a RC ladder network. As it is well known that the delay of single topology chain is a quadratic function of the number of Full Adders so for the long single topology chain the delay becomes unacceptably high. To limit this problem mixed topology strategy is adopted. This strategy includes the interruption of inverters (static gate) within the chain. proposed GDI Full Adder based on inverter is a better one as compared to existing topologies as far as delay, power and PDP is concerned. On the basis of simulation results obtained it is culminated that the proposed topology is suitable for high speed low power arithmetic circuits.

R. Mahalakshmi and T. Sasilatha [9] made some major advances in the design of CSA using CMOS technology. This works mainly focus on power using up and overall chip area since for an older structure these are the two primary parameters to be worried about. Their design uses 250nm and 65nm process technology, respectively, and their report shows a good quantity of reduction in power and expanse.

Amuthavalli. G and Gunasundari. R [12] proposed a power aware design for ripple carry adder (RCA). The proposed circuit also helps in cutting down the leakage current of the adder. This paper also analyzes the subthreshold leakage and it was proven that power due to subthreshold leakage reduces significantly as compared to conventional RCA design. They also employ the multi-Threshold CMOS (MT-CMOS) in the design for maintaining low power performance.

Ravikumar A. Javeli [15] design, CSA by using carry look ahead adder (CLA) instead of RCA, and the design approach represents the improvement in speed of the increase. The proposed design compared with regard to area, power and timings and it was established that the CSA using CLA improves the speed of calculation with minimum effect on area and the power of the pattern cell.

3. PROPOSED ARCHITECTURE

As MOS integrated circuit technology has evolved to exploit smaller and smaller device structures, it has become increasingly important in recent years to look more closely at the minority carriers present under the gate when the gate voltage is less than threshold, i.e. in what is called the "sub-threshold" region. These carriers cannot be totally neglected, and play an important role in device and circuit performance. At first they were viewed primarily as a problem, causing undesirable "leakage" currents and limiting circuit performance. Now it is recognized that they also enable a very useful mode of MOSFET operation, and that the sub threshold region of operation is as important as the traditional cut-off, linear, and saturations regions of operation. [3]-[5].

It consists of seven full adders and single half adder. The various ties and signal flow are shown in the design. The transistors cells are utilized in the design of CSA are GDI cells. GDI method is a low power design technique, by using this technique the various parameters such as power waste, delay, and sweep of digital IC is reduced much extent with very less complexity in the logic pattern. 4-bit CSA block diagram is shown in fig. 2. Circuit diagram of 4-bit CSA with equivalent GDI cells is shown in fig. 3. A proposed 4-bit full adder using GDI cell is shown in fig.4. This carry save adder uses only 10 transistors to perform both sum and carry operations.

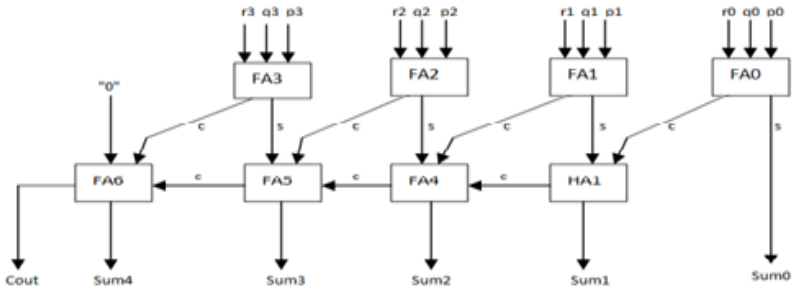

Fig.2. 4-bit CSA Block Diagram

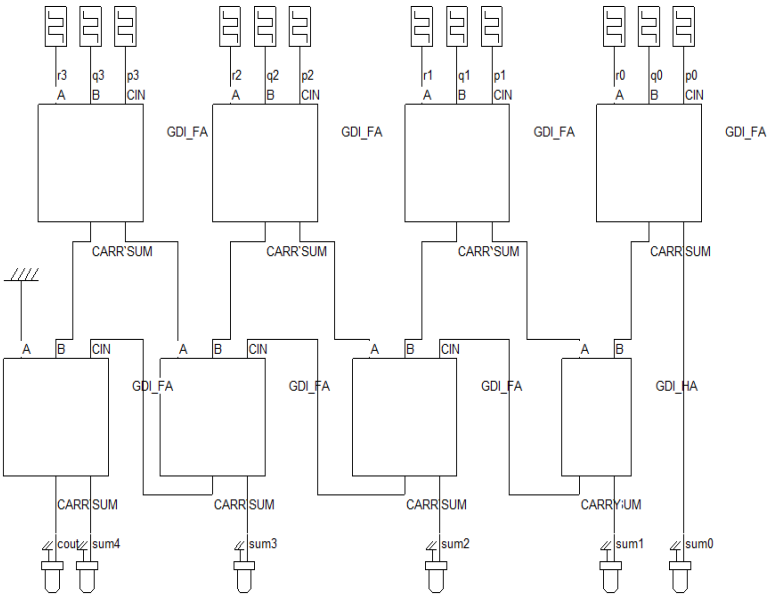

Fig.3. Circuit diagram of 4-bit CSA with equivalent GDI cells

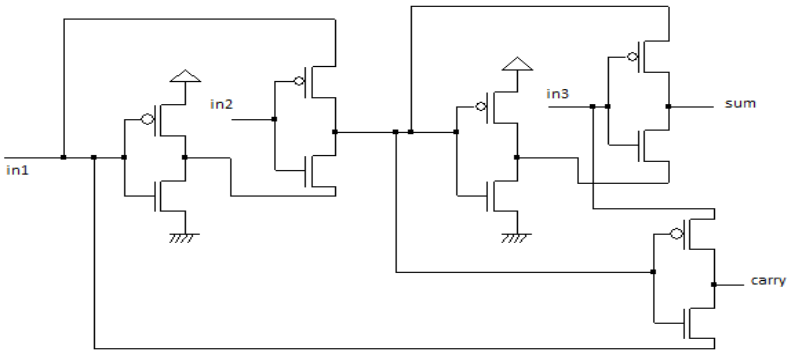

Fig.4. 4-bit CSA Block Diagram

4. SIMULATIONS AND RESULTS

The proposed carry save adder design is simulated using HSPICE and by taking 32nm CMOS nano technology. The functionality of the CSA is verified by writing HDL code. The mentor graphics modelsim used for the HDL modeling of the proposed CSA. The design of CSA is done using three level hierarchy, i.e. first the basic cell is designed and then using that cells the various subsystems are designed, and finally using these subsystems 4- bit CSA is designed. To design subsystems the GDI cells are applied to cut the power and area of the device. The pulse signal is chosen for input to the CSA. Fig.5 shows the input signals to the CSA.

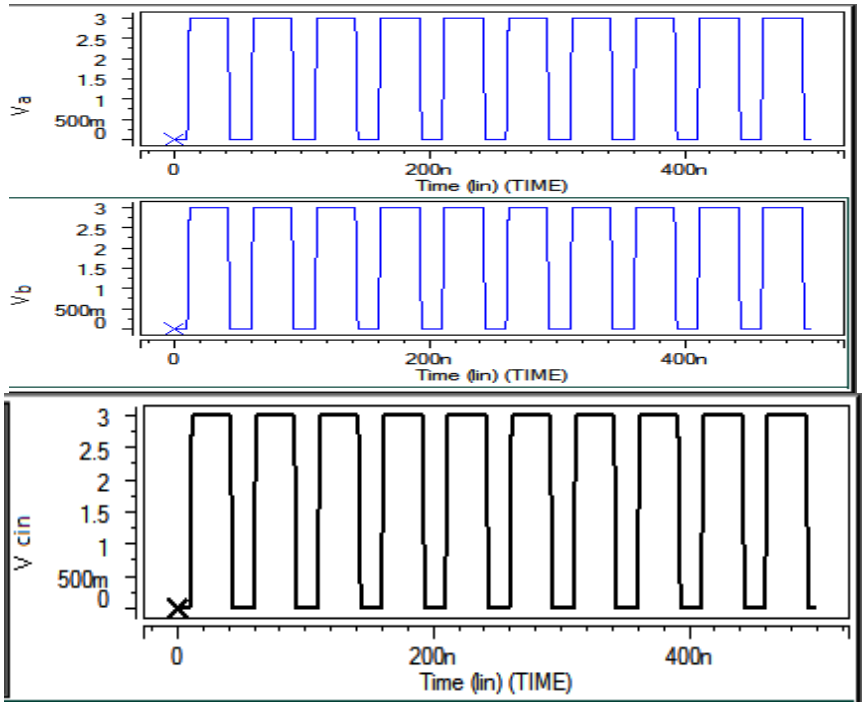

Fig.5. Input waveform of CSA

The output simulation results demonstrate the proper operation of the 4-bit CSA, and the behavior of various signals involved in the design is expressed beneath. The fig. 6 shows the output response of the CSA. HDL simulation can be done only to accomplish a high degree of trust in its correctness before commencing design, and may simulate one to one orders of magnitude quicker than a gate level description. An HDL specification for a part can perform the basis for a simulation model to verify the operation of the part in the wider system context; this depends on how accurately the specification handles aspects such as timing and initialization. The fig.7 shows the HDL model of CSA.

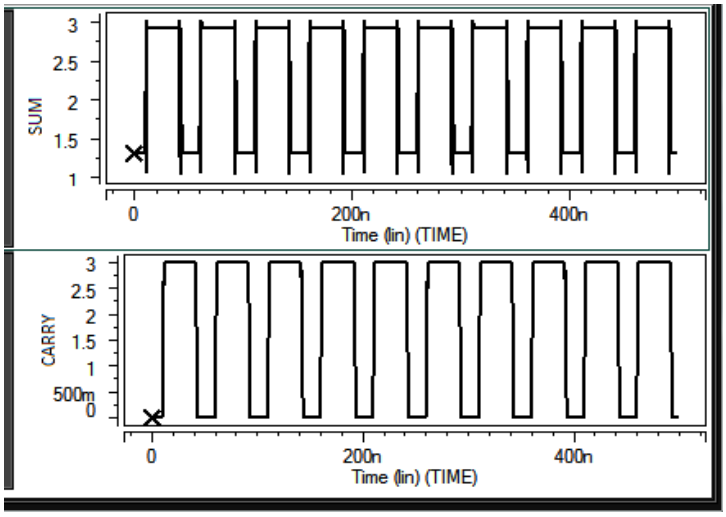

Fig.6. Output waveform from CSA

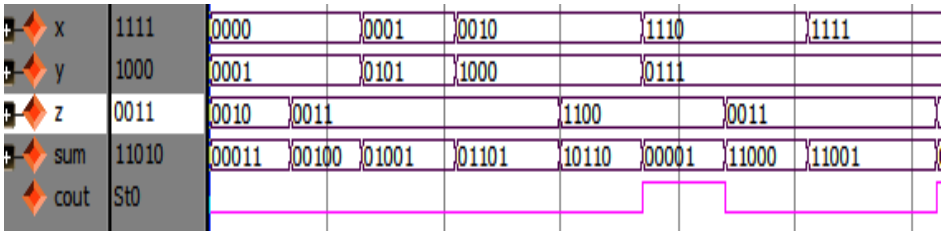

Fig.7. HDL Model of CSA

The fig. 8 shows the DC characteristics of the CSA. Fig. 9 and 10 shows the relationship between I_{ds} vs V_{ds} and I_{ds} vs V_{gs} respectively. Granting to the DC characteristic it can be reasoned that the MOS is not biased from its normal operation and the subthreshold effect is also negligible so the low power operation is required.

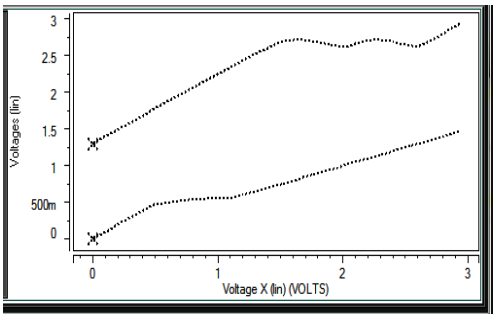

Fig.8. DC Characterstics of CSA

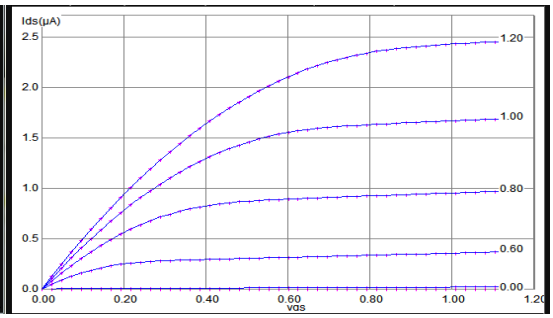

Fig.9. I_{ds} vs. V_{ds}

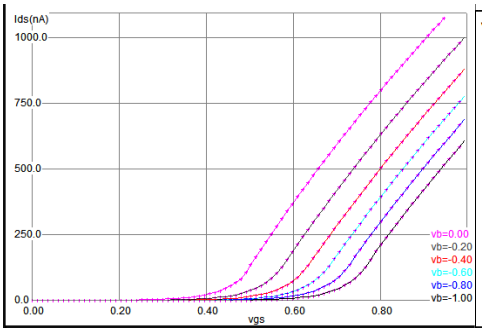

Fig.10. I_{ds} Vs V_{gs}

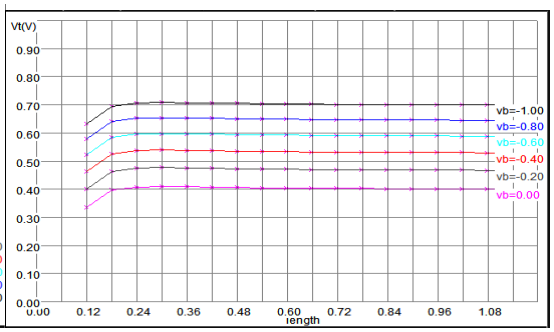

Fig.11. V_T wrt Channel Length

Fig.11 shows the relationship between channel length and the threshold voltage, after a certain limit is turned over for short channel the threshold roll off is well determined from the graph which will serve in the deciding the proper channel length of the device and it improves the device operation. The various optimized parameters related to the simulation are listed in Table – 1.Fig.12 shows the two major parasitic capacitances of the one bit full adder. However, these capacitances are optimized in such a fashion that it will not affect the circuit performance. The final optimized simulation layout is shown in figure – 13.

Table.1.Result of proposed design

Parameters	Values
Total Average Power	4.93 µW
Cgd	0.89 fF
Cgs	1.12 fF
Propagation Delay	16.3 ns
Area Optimized (Using GDI Cell)	37%

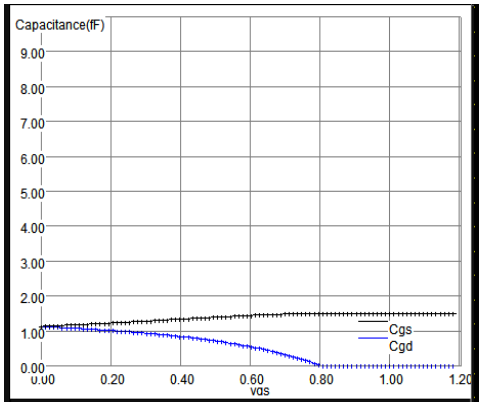

Fig.12. Parasitic Capacitances

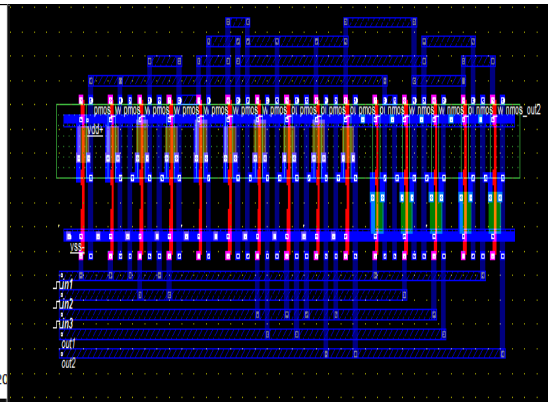

Fig.13. Optimized Simulation Layout

5 CONCLUSION

The 4-bit CSA is designed and related waveforms are plotted. By optimizing the operation parameters, it is noted that the CSA performs as it should and in subthreshold it consumes very less power since its static leakage current is cut. The switching also reduced by reducing carries propagation to the subsequent stages which ultimately result in a decrease of power dissipation of the gimmick. The results also bring out that the GDI cell requires less area as compared to conventional CMOS and it also improves the speed of operation of the device. Hence this paper performs sub threshold analysis on CSA and the scrutinize results that the total average power is around 4.93µW, the propagation delay for complete operation is 16.3ns and since this design uses GDI cell so there is a reduction in area with 37%.

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