STATIC NOISE MARGIN OPTIMIZED 11NM SHORTED-GATE AND INDEPENDENT-GATE LOW POWER 6T FINFET SRAM TOPOLOGIES

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ABSTRACT

This paper investigates the leakage current, static noise margin (SNM), delay and energy consumption of a 6 transistor FinFET based static random-access memory (SRAM) cell due to the variation in design and operating parameters of the SRAM cell. The SRAM design and operating parameters considered in this investigation are transistor sizing, supply voltage, word-line voltage, temperature and PFET and NFET back gate biasing. This investigation is performed using a 11nm FinFET shorted gate and low power technology models. Based on the investigation results, we propose a robust 6 transistor SRAM cells with optimized performance using shorted gate and independent gate low power FinFET models. By optimizing the design parameters of the cell, the shorted-gate design shows an improvement of read SNM of 261.56mV and an improvement of hold SNM of 87.68mV when compared to a shorted-gate cell with standard design parameters. The low-power design shows an improvement of read SNM of 146.18mV and a marginal decrease in hold SNM of 22.84mV when compared to a low-power cell with standard design parameters. Both the cells with the new optimized design parameters are shown to improve the overall SNM of the cells with minimal impact on the subthreshold leakage currents, performance and energy consumption.

KEYWORDS

SRAM, Leakage Power, Write Delay, Read Delay, FinFET, Static Noise Margin, SNM, Back Gate Biasing.

1. INTRODUCTION

Technology scaling in bulk-Si MOSFETs presents a growing concern toward the stability of Static Random Access Memories (SRAM) [1]. As the feature size of the technology decreases, the process and operating parameter variations can negatively impact the reliability of the memory to retain data [2]. Higher static noise margin (SNM) during read, write, and hold operations are required for low-voltage low power SRAM designs to mitigate the effects of process and operating parameter variations on data stored in SRAM cells. In single supply voltage integrated circuits (ICs), the supply voltage (Vdd) is typically defined by the SRAM's static noise margin [3]. To improve the electrostatic characteristics of the gate, a multi-gate device structure can be utilized, as they provide improved electrostatic control of the gate [3].

Unlike conventional MOSFETs, FinFETs employ a three-dimensional gate structure, which allows for better electrostatic control of the gate. By raising the channel above the surface of the wafer, the gate wraps around the channel to provide greater control over the channel as shown in Figure 1. The self-aligned gate straddles a narrow silicon fin (channel), therefore current flows parallel to the wafer surface. The major obstacle when moving from bulk CMOS to multi-gate devices lies within the manufacturing. However, FinFETs offer a geometry that is compatible with current manufacturing techniques [4]. This presents a distinct advantage in the cost of production and has helped to facilitate the use of FinFET technology in the sub-20nm regime.

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This paper focuses on bridging the gap between the research performed to transfer from 6T CMOS SRAM memory cells to 6T FinFET SRAM memory cells, and analyze the tradeoffs of varying cell ratio, pull-up ratio and word line voltage effect on the stability of a shorted-gate (SG) and independent-gate low-power (LP) 6T FinFET SRAM memory cells.

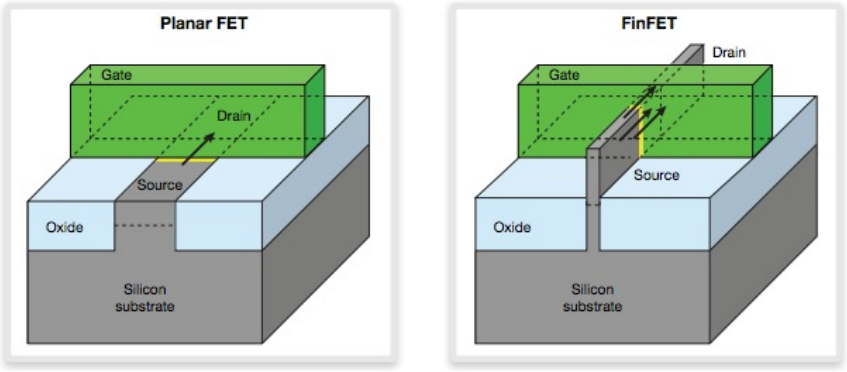

Figure 1: 2-d Planar MOSFET (left), 3-d FinFET (right) [5].

The rest of this paper is organized as follows. Section 2 describes the tools and methodologies used for the simulations of the SRAMs. Section 3 presents the results and discussions of the variations in the design and operating parameters such as cell ratio, pull-up ratio, supply voltage, word-line voltage, temperature and back gate biasing on the SRAM subthreshold leakage currents, SNM and delays for SG and LP schemes. Section 4 describes the optimization of the design parameters for the SRAM cell using SG and LP models. Finally, conclusions are presented in section 5.

2. TOOLS AND METHODOLOGIES

In this research, simulation of the SRAM cells utilizes the University of Florida's Spice-3-UFDG fully-depleted (FD) silicon-on-insulator (SOI) FinFET model [6]. This FinFET model accounts for the short channel effects based on the process and physics of the compact model. Simulations are performed using Ngspice simulator which is a mixed mode-mixed level circuit simulator. The SRAM cells are simulated using shorted-gate and independent-gate mode FinFET models. The parameters of the FinFETs used in this research are summarized in Table 1.

TABLE 1: 6T FinFET design parameters

Parameter	Value
Orientation	<110>
Gate Length	1.07 nm
Fin Height	1.8 nm
Oxide Thickness	0.59 nm/cm3
Source & Drain Doping	1E15/cm3
Vdd,Word Line	0.68 V
Cell Ratio, Pull-Up Ratio	1:1, 1:1
PFET Back-Gate Biasing	0.88 V
NFET Back-Gate Biasing	-0.2 V

The design parameters considered in the simulations of the SRAM are transistor sizing (cell ratio and pull-up ratio), supply voltage, word-line voltage, temperature, PFET and NFET back-gate biasing.

The cell ratio (β_C) and load ratio (β_L) are given by equations (1) and (2) respectively.

$$\beta_C = \frac{W_{M1}/L_{M1}}{W_{M2}/L_{M2}} = \frac{W_{M4}/L_{M4}}{W_{M5}/L_{M5}} = \frac{W_{M1}}{W_{M2}} = \frac{W_{M4}}{W_{M5}} \quad (1)$$

$$\beta_L = \frac{W_{M3}/L_{M3}}{W_{M2}/L_{M2}} = \frac{W_{M6}/L_{M6}}{W_{M5}/L_{M5}} = \frac{W_{M3}}{W_{M2}} = \frac{W_{M6}}{W_{M5}} \quad (2)$$

where $W_{Mi}$and L_{Mi} are the width and length of the i^{th} transistor. Because the channel length of all the transistors in the cell are the same, only the width is considered in the ratio. For non-destructive read and write operations, appropriate βC and βL must be selected.

Subthreshold leakage, hold SNM, read SNM, read delay and write delay are measured by varying one of the above-mentioned design parameters while keeping the other design parameters constant. After analysing the results, an optimized SRAM cell with maximum SNM, lower subthreshold leakage and delay is proposed for both SG and LP 6T FinFET SRAM cells.

SNM calculations were performed by modelling the SRAM cell as two cross-coupled inverters with noise sources inserted between them [7], shown in Figure 2(a). Both the noise voltages are equal and opposite in direction, which represents the worst-case scenario for noise margins [2]. To measure the SNM, the "butterfly curve" method was employed [8]. In this method, the voltage transfer curve (VTC) of one inverter is plotted with the inverse of the VTC of the other inverter transposed onto it. This creates a "butterfly curve", as seen in Figure 2 (b). The SNM of the SRAM cell is the length of the diagonal of the maximum square that can fit in the butterfly curve [8]- [12]. The back-gate biasing simulations are performed only for LP models which has two independent gates (front and back gates) while the gates are shorted for SG models.

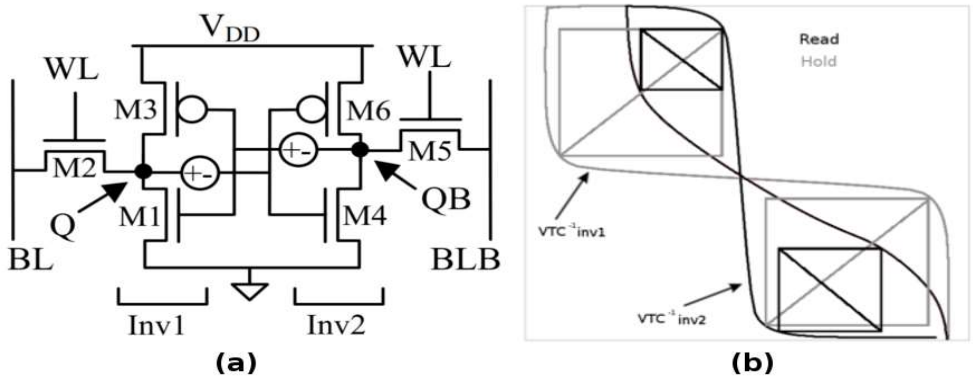

Figure 2: (a) Schematic diagram for finding SNM [1], (b) Butterfly diagram for finding SNM.

3. SIMULATION RESULTS AND DISCUSSIONS

The SRAM cell using SG and LP FinFET models are simulated with one of the design parameters mentioned in the previous section varies while the other parameters are static. For each simulation run, the subthreshold leakage current, hold SNM, read SNM, read and write delays are measured, plotted and analyzed. In the following section we discuss the simulation results and observations in detail.

3.1. SRAM CELL RATIO VARIATION

The cell ratio is defined as the ratio of the width over length (W/L) of the NFET pull-down transistors to the NFET access transistors. The cell ratio contributes to the performance and stability of the SRAM during a read operation. With a larger cell ratio, there is a reduced risk of data loss during a read operation. This stability has a performance penalty, because of the negative impact on the read current [5]. Typically, the cell ratio is chosen to be between 1.3-2x to provide a sufficient ratio for read stability for CMOS designs [3]. Both the SG and LP design schemes were simulated with a cell ratio of the width of the inverter NFET pair to the width of the access transistor NFET pair of 1:1 to 8:1.

3.1.1. SUBTHRESHOLD LEAKAGE CURRENT

When varying the cell ratio, the subthreshold leakage current increased with the increase in the cell ratio which is increased by the size of the NFET transistors, as shown in Figure 3. Compared to the use of SG transistors, the LP transistor SRAM had two orders less leakage current. The increase in cell ratio did show the greatest increase in subthreshold leakage current when increasing the inverters NFET transistors from a 1:1 ratio up to a 2.5:1 ratio. Both schemes show an increase of over 700% from 1:1 to 8:1. This indicates that the cell ratio needs to be kept around 2.5:1 to maintain adequate cell performance.

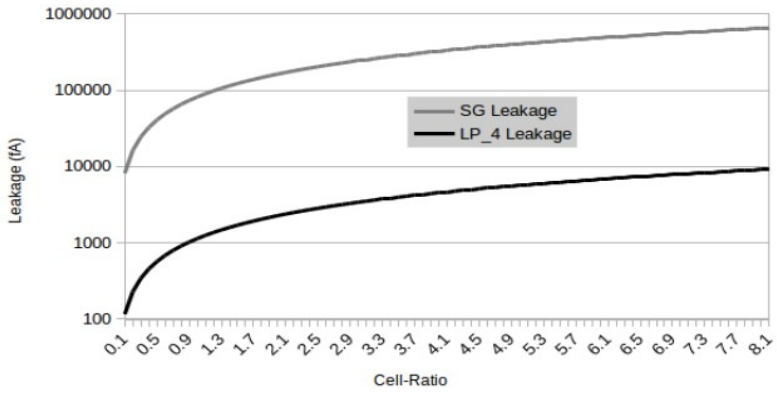

Figure 3: Leakage current dependence on Cell ratio variation.

3.1.2. HOLD SNM

By increasing the cell ratio, the hold SNM decreased for both SG and LP models as shown in the Figure 4. The SRAM cell using LP model had 70 mV lower noise margin compared to the SG model for a cell ratio of 1:1and the difference remained constant with varying cell ratio. At a ratio of 2.5:1, the hold SNM was reduced by 2.4% and 3.6% for the SG and LP schemes respectively. From a ratio of 1:1 to 8:1, the SNM was only reduced by 19.79mV (6.6%) for the SG scheme, and 21.1mV (9.3%) for the LP scheme. For each cell ratio, the hold SNM of the LP scheme remained around 75% of the SG scheme's hold SNM. From a hold SNM perspective, the cell ratio does not significantly impact the hold noise immunity.

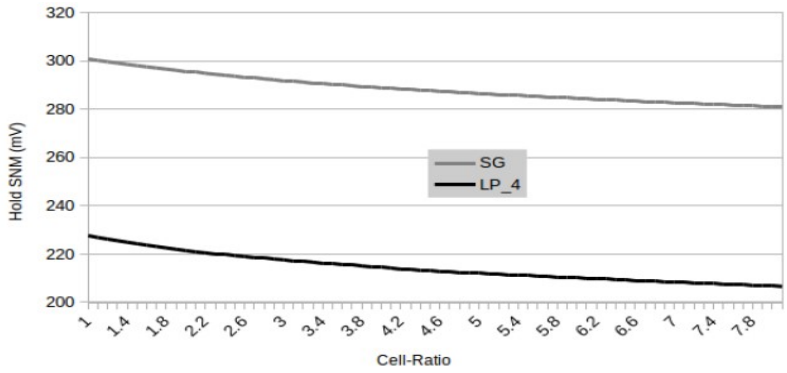

Figure 4: Hold SNM dependence on Cell ratio variation.

3.1.3. READ SNM

By increasing the cell ratio, the ratio of the pull-down current IPD to the access current IACCESS (β) increases. This increases the noise immunity during read operations [3]. Having a sufficient β ensures that the inverter storing a logical "0" will not be pulled up to "1" because of the bit-line pre-charge voltage. For the SG scheme, increasing the cell ratio from 1:1 to 8:1 increased the read SNM from 140 mV to 178 mV as shown in the Figure 5. However, for the LP scheme, increasing the cell ratio decreased the read SNM from 177 mV to 169 mV. At a cell ratio of 8:1, the SG scheme's read SNM has an increase of 27.3% while the for LP scheme it decreases by 4.3%. For a cell ratio of 2:1, an 8.5% increase for the SG scheme, and 1.1 % decrease for the LP scheme is observed for read SNM.

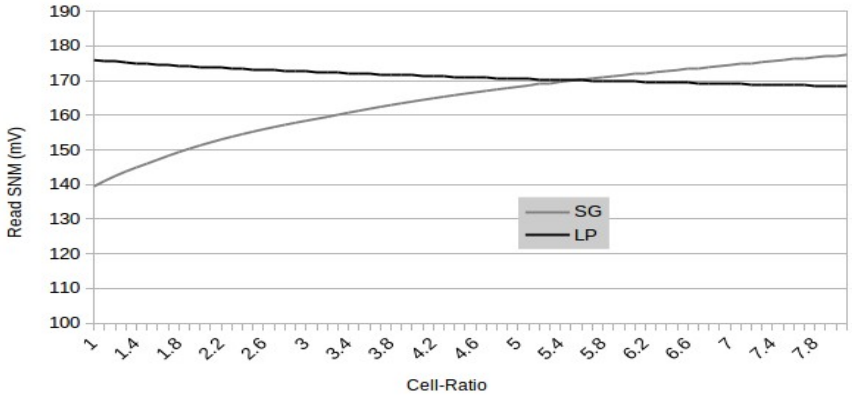

Figure 5: Read SNM dependence on Cell ratio variation.

3.1.4. READ AND WRITE DELAY

The read and write delay of the SG scheme are less severely affected by the cell ratio as shown in Figure 6 and Figure 7 respectively. The read delay for LP scheme increased with the cell ratio till it reached a ratio of 3:1, having a read delay of 103.5ps and then it decreases with the increase in cell ratio. For cell ratio from 1:1 to 8:1, the LP scheme had an overall reduction of the read delay of 29%, from 72.5ps to 51.5ps. The write delay for SG increased slightly from 2.56ps to 7.5ps. The shorted-gate scheme shows the most resilience to cell ratio increase in the both delays. The write delay of the LP scheme increases with increasing cell ratio from 1:1 to 8:1 of 27.9%.

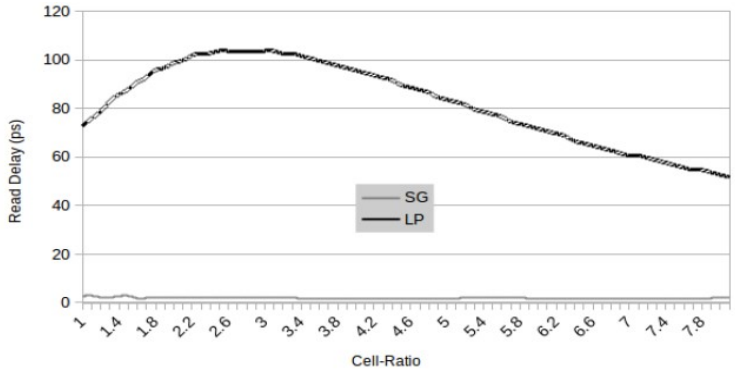

Figure 6: Read delay dependence on Cell ratio variation.

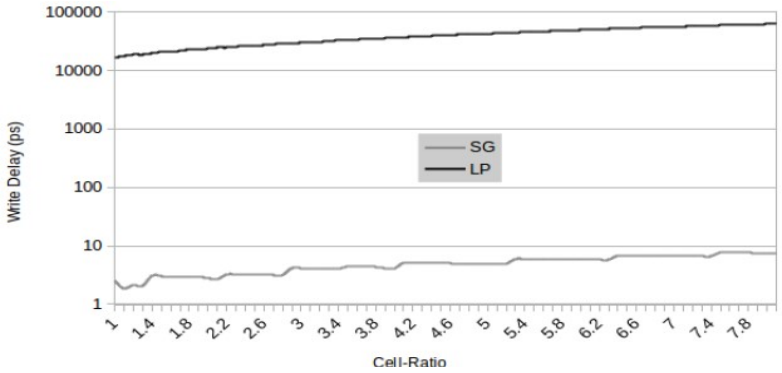

Figure 7: Write delay dependence on Cell ratio variation.

3.2. SRAM PULL-UP RATIO VARIATION

To improve the SNM during writing, the ratio of the width over length (W/L) of the NFET access transistors to the PFET pull-up transistors can be adjusted. The access transistor must be strong enough to overcome the PFET when writing a logical "0" to the inverter [5]. Therefore, to improve the write SNM of the SRAM, one must either increase the width of the access transistors to increase the drive strength or decrease the width of the PFET transistors. Since reducing the size of the NFET transistors would inhibit the write SNM, the PFET transistors were adjusted for testing. The pull-up ratio was varied from 1:1 to 8:1 for all the following simulations to observe its dependence on the cell characteristics.

3.2.1. SUBTHRESHOLD LEAKAGE CURRENT

Our simulation studies revealed that, increasing the pull-up ratio leads to increase in subthreshold leakage current as shown in Figure 8. The leakage associated with the LP scheme remained at 1.35% of the leakage associated with the SG scheme. The leakage current increased from 2 fA to 6 fA for LP scheme and 102 fA to 170 fA for SG scheme for pull-up ratio from 1:1 to 8:1.

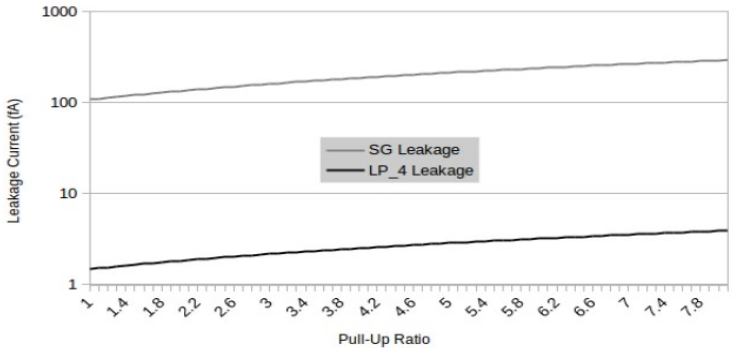

Figure 8: Leakage current dependence on Pull-Up ratio variation.

3.2.2. HOLD SNM

It was observed that, increasing the pull-up ratio has little effect on the hold SNM for the SG scheme, as seen in Figure 9. The hold SNM increases by just 0.4 mV over the simulation. The LP scheme has a decrease in hold SNM by 9.8% for the simulation range. The hold SNM of the LP scheme decreases from 239.85mV to 216.3mV. The simulation results indicate that the pull-up ratio has little effect on the hold SNM.

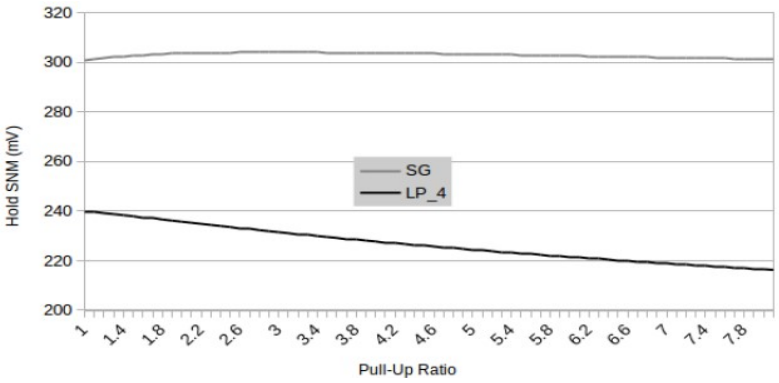

Figure 9: Hold SNM dependence on Pull-Up ratio variation.

3.2.3. READ SNM

Increasing the pull-up ratio improves the read SNM, as shown in Figure 10. The LP scheme shows a greater increase in RSNM compared to the SG scheme. At 2.5:1, the read SNM of the LP scheme improves by 19.8mV, while the SG improves by 7.1mV. At the maximum ratio, the SG scheme's read SNM improved by 10.3%, while the LP scheme's read SNM improved by 28.5%.

3.2.4. READ AND WRITE DELAY

Figure 11 and Figure 12 shows the read and write delay dependence of the 6T SRAM cell on the pull-up ratio. Increasing the pull-up ratio of the SRAM cell increases the read delay and write delay for LP and SG schemes respectively. From a cell ratio of 1:1 to 8:1, the SG scheme had negligible change in read delay, while for the LP scheme the read delay increased from 86.5ps to 270.5ps. Conversely, the pull-up ratio had almost no effect on the LP scheme write delay, and an increase in write delay from 2.9ps to 11.3ps for the SG scheme.

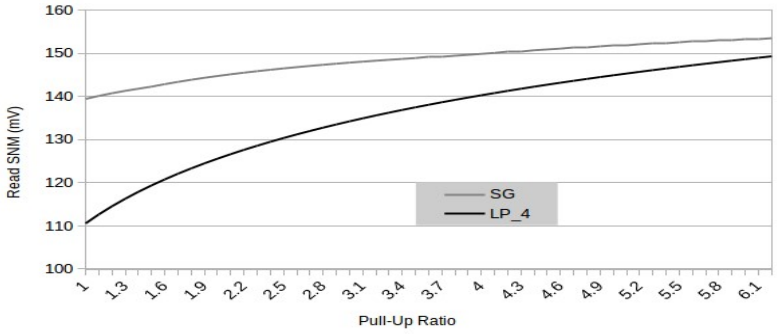

Figure 10: Read SNM dependence on Pull-Up ratio variation.

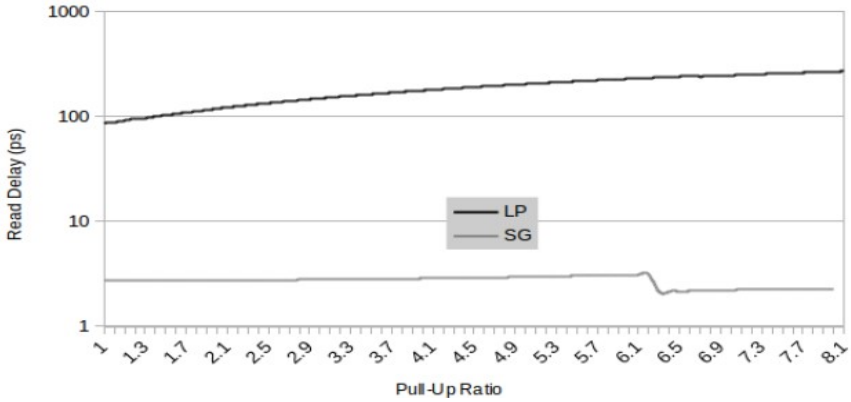

Figure 11: Read delay dependence on Pull-Up ratio variation.

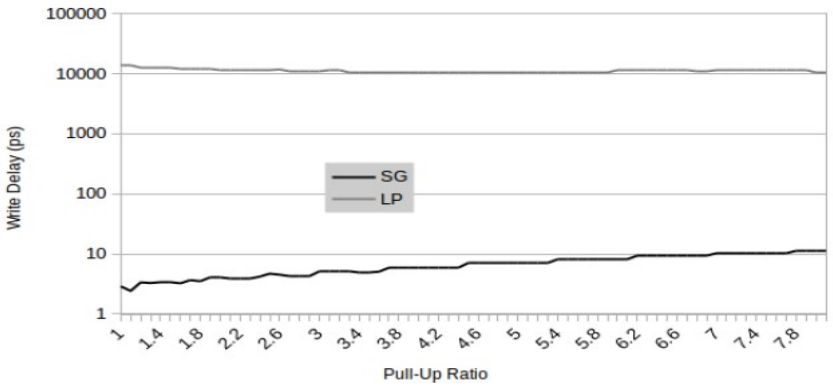

Figure 12: Write delay dependence on Pull-Up ratio variation.

3.3. SUPPLY VOLTAGE VARIATION

3.3.1. SUBTHRESHOLD LEAKAGE CURRENT

The effect of supply voltage on the cell characteristics is investigated by varying it from 0V to 1.2V. The leakage current for SG and LP schemes are plotted in Figure 13. It can be observed that the leakage current of SG scheme is higher than LP schemes up to 1V. Supply voltage beyond 1V, LP scheme has higher leakage currents. This leakage currents are tabulated in Table 2.

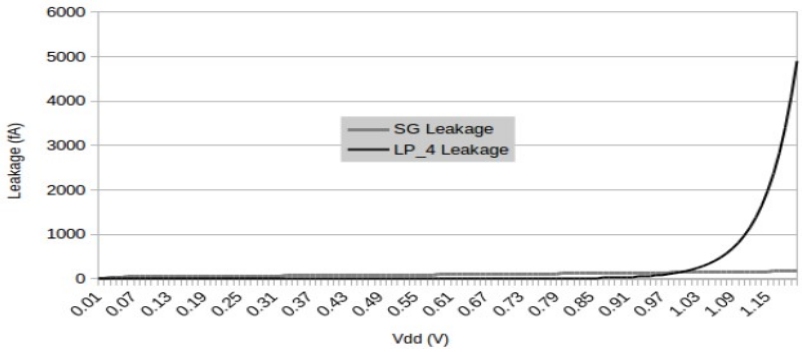

Figure 13: Leakage current dependence on Vdd variation.

Table 2: Supply voltage vs Leakage current

Vdd(V)	SG Leakage (fA)	LP Leakage (fA)
0.1	53.62	0.004
0.2	61.67	0.051
0.3	70.18	0.466
0.4	79.30	0.835
0.5	89.05	0.951
0.6	99.47	1.12
0.7	110.59	1.67
0.8	122.45	5.30
0.9	135.09	36.28

3.3.2. HOLD SNM

Increasing Vdd improves the hold SNM as shown in Figure 14. For a supply voltage of less than 0.3V, the LP hold SNM remains close to 0V. Below this voltage, SRAM cannot hold the data. The hold SNM for the SG scheme is linear from 0.1V to 1V. For supply voltage of 1.2V, SG and LP schemes have a hold SNM of 500mV and 325mV respectively.

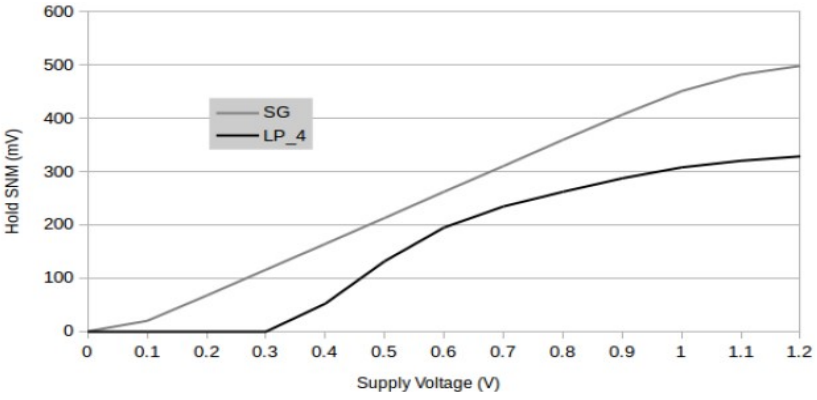

Figure 14: Hold SNM dependence on Vdd variation.

3.3.3. READ SNM

Similar to the hold SNM, the read SNM increases with Vdd as plotted in Figure 15. The SG scheme has a linear increase in read SNM from 0.5V to 1V. For a supply voltage of 1.2V, SG and LP schemes have a read SNM of 460mV and 325mV respectively.

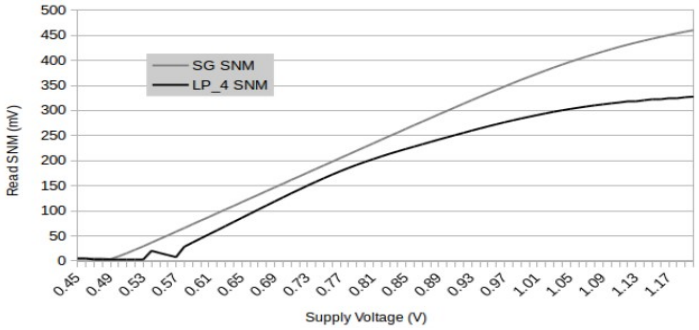

Figure 15: Read SNM dependence on Vdd variation.

3.3.4. READ AND WRITE DELAY

The read and write delay of the 6T SRAM cell decreased exponentially with increasing voltage as shown in Figure 16 and Figure 17 respectively. For supply voltage of less than 0.4V, both the SG and LP had larger read delay as the transistors are operating in subthreshold region and the read fails for lower supply voltages. Write delay was four orders larger than read delay and the write failure occurred at a supply voltage of less than 0.5V.

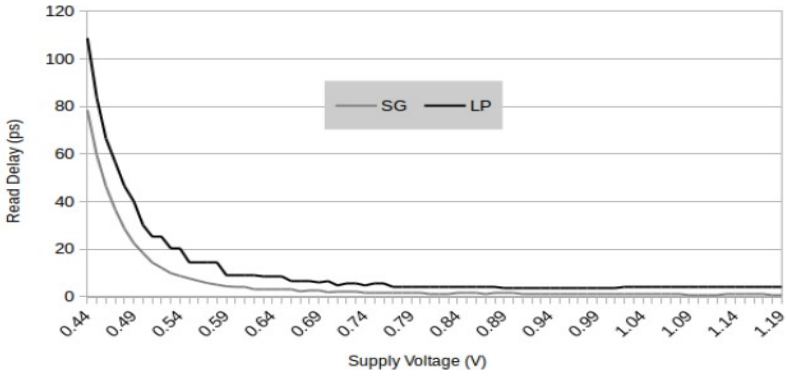

Figure 16: Read delay dependence on Vdd variation.

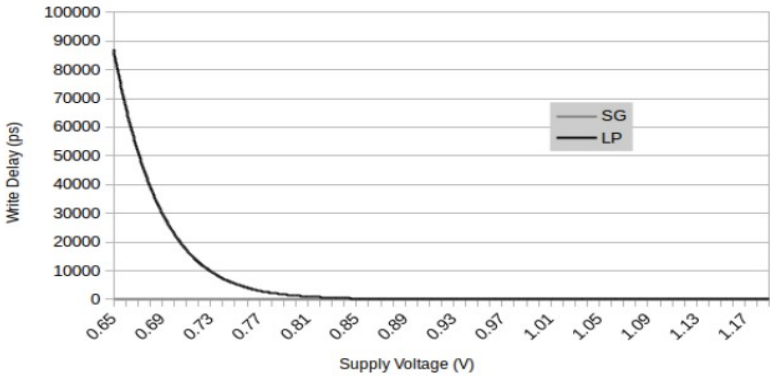

Figure 17: Write delay dependence on Vdd variation.

3.4. WORD-LINE VOLTAGE VARIATION

The word-line voltage is varied from 0V to 1.2V. The subthreshold leakage current and hold SNM show no change as the WL voltage should be 0V during hold operation.

3.4.1. READ SNM

Increasing the word line voltage beyond the threshold voltage results in a linear decrease of read SNM as shown in Figure 18. For the SG scheme, the read SNM starts to decrease from 300 mV for WL of over 0.25V. For the LP scheme, the read SNM starts to decrease from 165 mV for WL of over 0.4 V. For WL of 1V and above, the SG and LP schemes have read SNM of 0V.

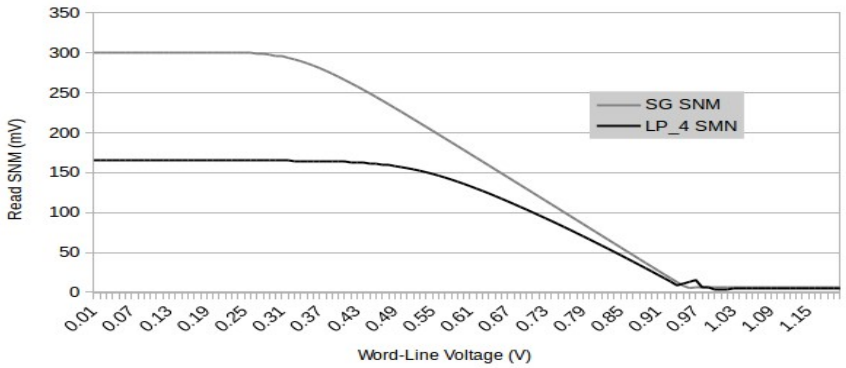

Figure 18: Read SNM Dependence on Word-Line Voltage variation.

3.4.2. READ AND WRITE DELAY

The read and write delay decreases exponentially for LP schemes as shown in Figure 19 and Figure 20 respectively. The SG scheme has lower read and write delays. The read and write delay could not be measured for world line voltages less than 0.8V and 0.6 V respectively. For the word line voltage of 0.85V to 1.2V, the read delay for the LP scheme reduced by 87.7ps. The read delay remained constant at 5ps for word line voltage greater than 0.95V. The LP scheme showed the reduction in write delay from 633.2 ns to 74.1 ps for word line voltage from 0.65V to 1.2V.

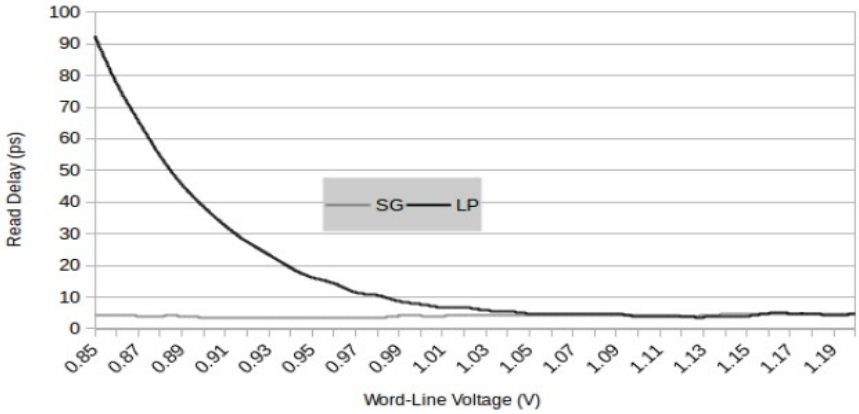

Figure 19: Read delay Dependence on Word-Line Voltage variation.

3.5. TEMPERATURE VARIATION

3.5.1. SUBTHRESHOLD LEAKAGE CURRENT

Even though it is well known that the leakage current increases with temperature, we investigated the temperature dependency on subthreshold leakage current by varying the temperature from 0°C to 100°C. Similar to supply voltage variations, the subthreshold leakage current increases exponentially with the increase in temperature as shown in Figure 21. At higher temperatures, LP scheme had relatively lower leakage currents. Comparing the leakage currents at 0°C to leakage

current at room temperature (27°C), the leakage current increased from 0.11 fA to 10.8 fA and 0.0001fA to 1.48 fA for SG and LP schemes respectively. At 100 °C the subthreshold leakage current was 10.04pA and 0.334fA for SG and LP schemes respectively.

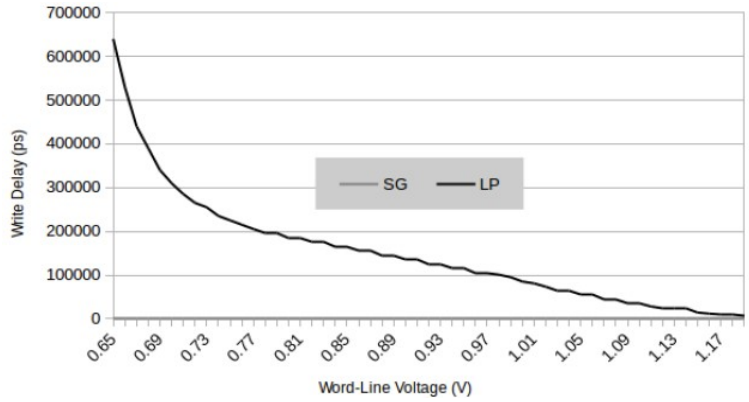

Figure 20: Write delay Dependence on Word-Line Voltage variation.

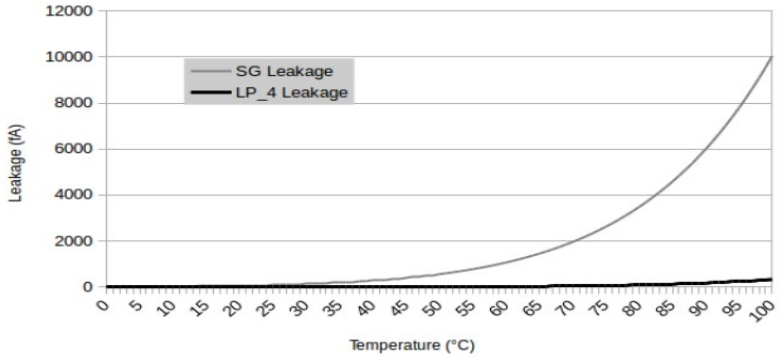

Figure 21: Leakage current Dependence on Temperature Variation.

3.5.2. HOLD SNM

As shown in Figure 22, for temperature from 0°C to 100°C, the hold SNM for SG scheme decreased from 303.5 mV to 292.83 mV and for LP scheme the hold SNM decreased from 232.72 mV to 212.49 mV which corresponds to about 9% decrease in the SNM. At room temperature, the hold SNM was 300.84mV and 227.66mV for SG and LP schemes respectively.

3.5.3. READ SNM

Simulation results show that the Read SNM has similar trend as hold SNM as shown in Figure 23. For temperature variation from 0°C to 100°C, the read SNM for SG scheme decreased from 141.62 mV to 132.75 mV and for LP scheme the read SNM decreased from 114.85 mV to 95.12 mV. At room temperature, the hold SNM was 139.46 mV and 110.6 mV for SG and LP schemes respectively.

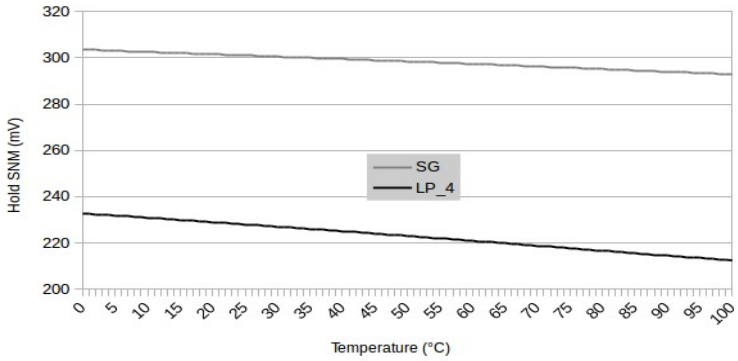

Figure 22: Hold SNM Dependence on Temperature Variation.

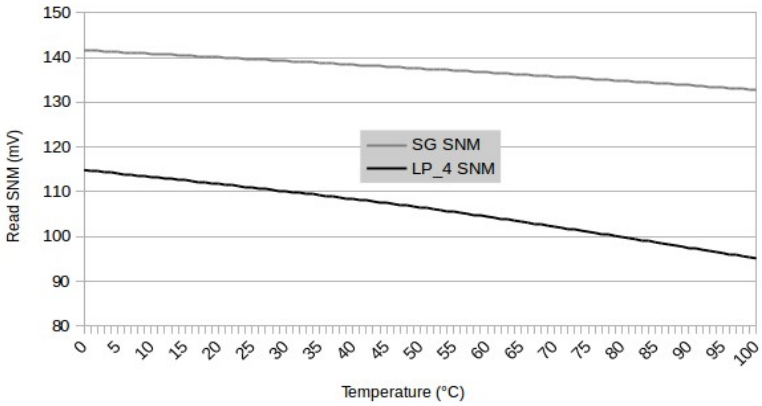

Figure 23: Read SNM Dependence on Temperature Variation.

3.5.4. READ AND WRITE DELAY

Figure 24 and Figure 25 shows the read and write delay plots of the 6T SRAM cell with varying temperature respectively. With the increase in temperature, the delay decreased. The read delay for the LP scheme reduces by 68.4ps as the temperature increases from 15°C to 100°C and the read delay of the SG scheme decreased only by 0.92ps. the write delay decreased by 1.46 ps for temperature variation from 15°C to 100°C for SG scheme. The LP scheme shows a linear reduction of write delay from 81.2 ns to 3.3 ns for increasing temperature from 15°C to 100°C.

3.6. PFET BACK-GATE BIASING VARIATION

Only independent gate LP FinFET models were investigated in this research. The SRAM inverter PFET back-gate voltage is incremented from 0V to 1.2V, while the NFET's back gate voltage is held at -0.2V. The results are discussed in the following sections.

3.6.1. SUBTHRESHOLD LEAKAGE CURRENT

The leakage current reduces exponentially as the back-gate bias increases as shown in Figure 26. For a back-gate biasing of 0V, the leakage current is high at 63.2nA. As the back-gate bias decreases to 0.25V, the additional inversion of the channel results in a subthreshold leakage current of 0.21nA, a reduction of 99.67%.

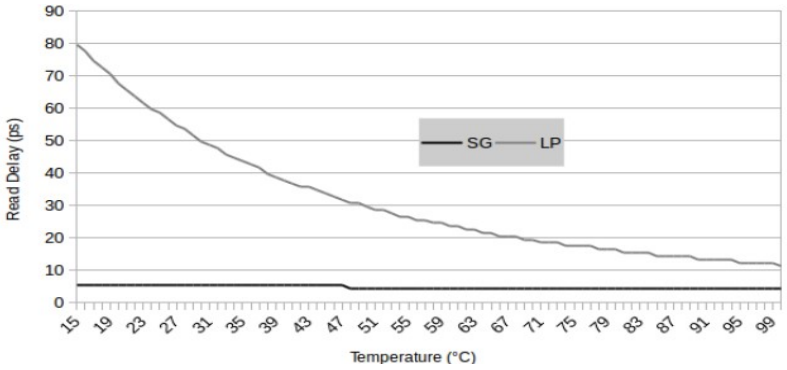

Figure 24: Read delay dependence on Temperature Variation.

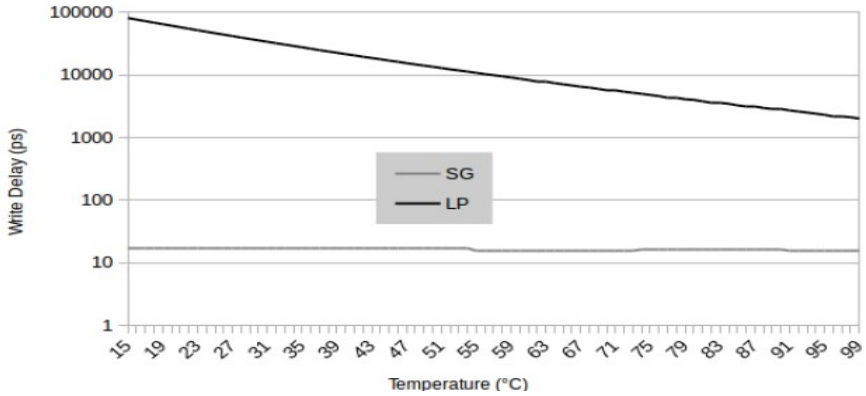

Figure 25: Write delay dependence on Temperature Variation.

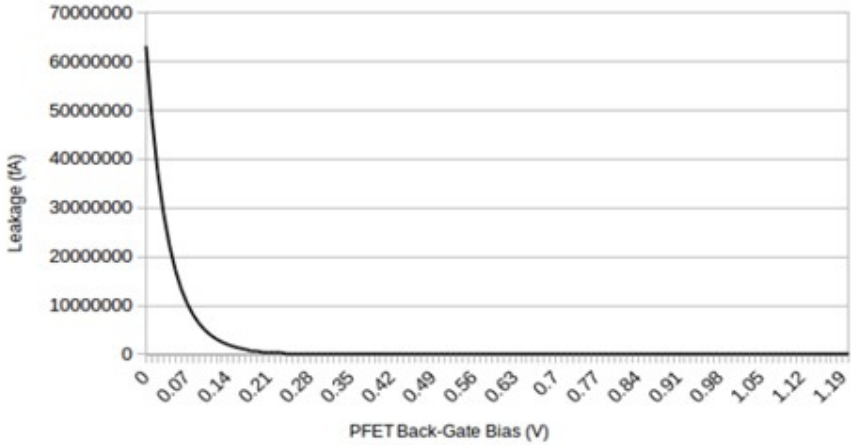

Figure 26: Leakage current dependence on PFET Back-Gate biasing.

3.6.2. HOLD SNM AND READ SNM

Figure 27 shows the read and hold SNM for PFET back gate biasing from 0V to 1.2V. for back gate bias of 0.73V, the maximum hold SNM of 241.2 mV is observed and a maximum read SNM is 192.94mV is achieved at back-gate bias voltage of 0.57V.

3.6.3. READ AND WRITE DELAY

Figure 28 shows the read delay plot for varying PFET back-gate bias voltage respectively. As the back-gate bias of the inverter PFETs increases from 0V to 0.5V, the read delay increases in steps from 44ps to a maximum delay of 54.7ps which remains constant for back gate bias voltage greater than 0.5V. Figure 29 gives write delay plot for varying PFET back-gate bias voltage. The write delay increases exponentially with the increase of PFET back-gate bias after 0.77V. At this voltage, the write delay increases from 8.7ns to 41.1ns. Write delay is four orders larger than read delay.

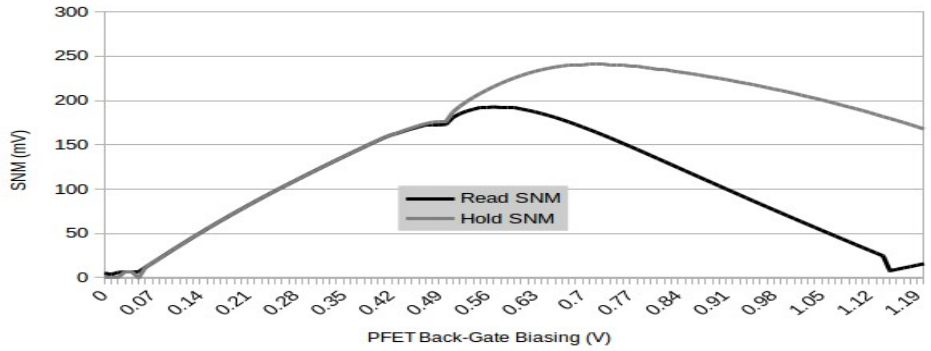

Figure 27: Read and Hold SNM dependence on PFET Back-Gate biasing.

3.7. NFET BACK-GATE BIASING VARIATION

The back-gate bias for the SRAM inverter NFET transistors is simulated for a back-gate voltage from -0.65V to 0V, while the PFETs back-gate bias voltage is held at Vdd+0.2V (0.88V) for the LP scheme. The results are discussed in detail below.

3.7.1. HOLD SNM AND READ SNM

The hold SNM shows a greater increase for increasing back-gate bias with a maximum of 269.7mV at a back-gate bias of -0.03V. The read SNM peaks at 175.93mV at -0.2V. The read and hold SNM is plotted in Figure 30.

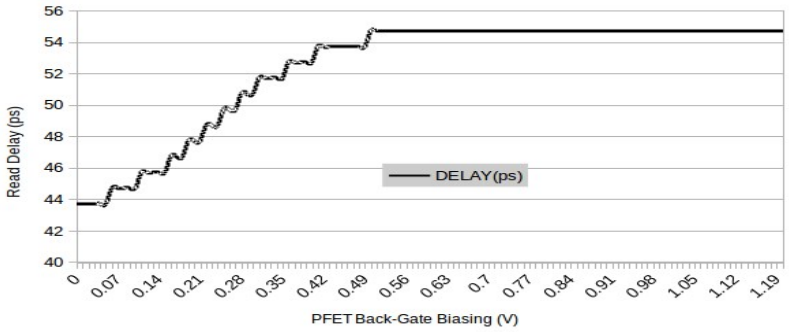

Figure 28: Read delay dependence on PFET Back-Gate biasing.

3.7.2. SUBTHRESHOLD LEAKAGE CURRENT

When varying the NFET back-gate biases, the leakage current reduces exponentially as the back-gate bias decreases, as shown in Figure 31. For a back-gate bias of 0V, the leakage current is 84.7fA. For a back-gate bias of -0.25V, the additional inversion of the channel results in a subthreshold leakage current of 3.25fA. For the back-gate bias that has the highest read SNM (-

0.2V), the subthreshold leakage current is 4.16fA. For the back-gate voltage that produced the best hold SNM (-0.03V), the subthreshold leakage is 35.98fA. Unlike the PFET back-gate biasing, the NFET back-gate biasing that produced the best read and hold SNM did not reduce the leakage current when compared to the subthreshold leakage current for a back-gate bias of 0V. However, the subthreshold leakage current reduction is minimal when back-gate is biased beyond -0.2V.

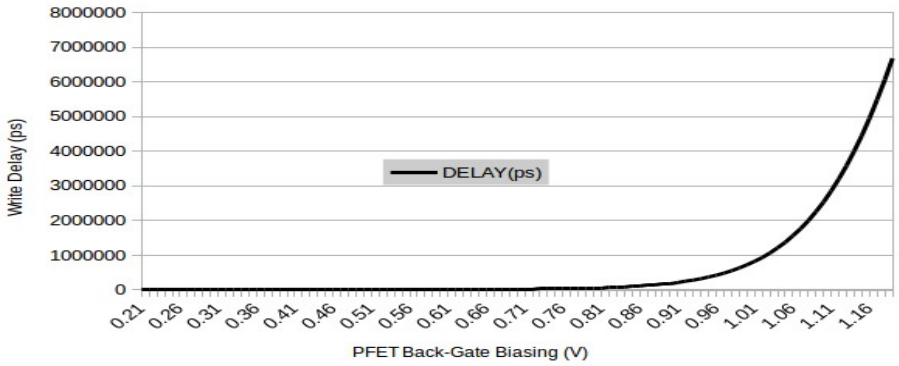

Figure 29: Write delay dependence on PFET Back-Gate biasing.

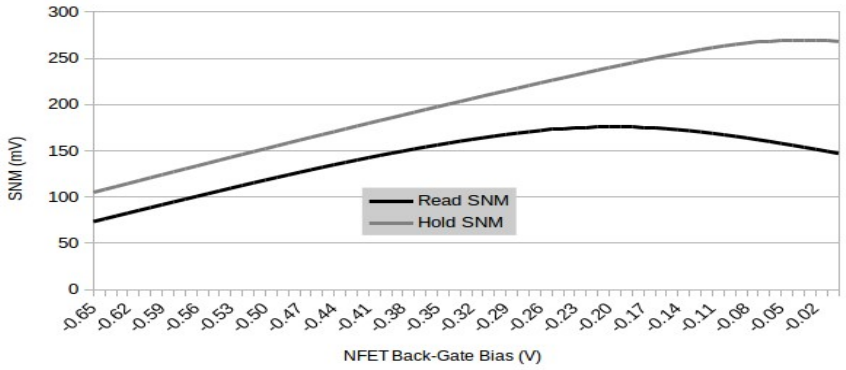

Figure 30: SNM dependence on NFET Back-Gate biasing.

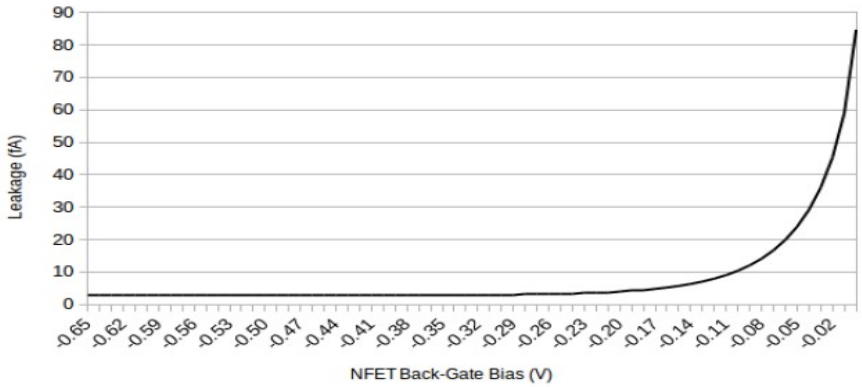

Figure 31: Leakage current dependence on NFET Back-Gate biasing.

3.7.3. READ AND WRITE DELAY

It was observed that back-gate biasing the SRAM cell's NFET transistors from -0.68V to 0V, both the read and write delay decreased exponentially as shown in Figure 32 and Figure 33

respectively. Increasing the back-gate bias voltage from -0.24 to 0V reduces the read delay from 85.8ps to 8.7ps. Similarly, reducing the back-gate bias from -0.68V to -0.24V reduces the write delay from 555.3ps to 155.3ps. Further reduction from -0.24V to 0V reduces the write delay to 95.3ps.

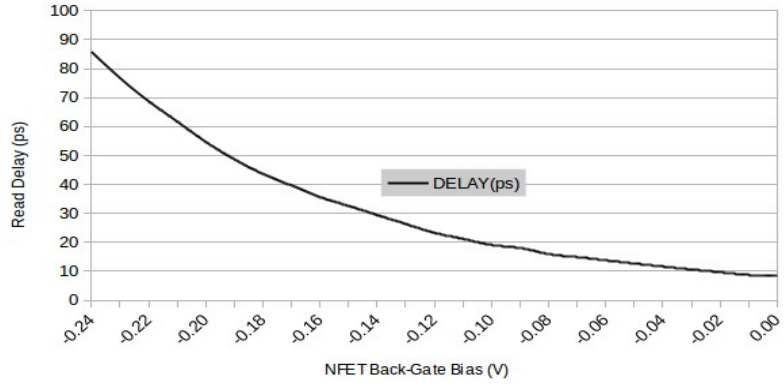

Figure 32: Read delay dependence on NFET Back-Gate biasing.

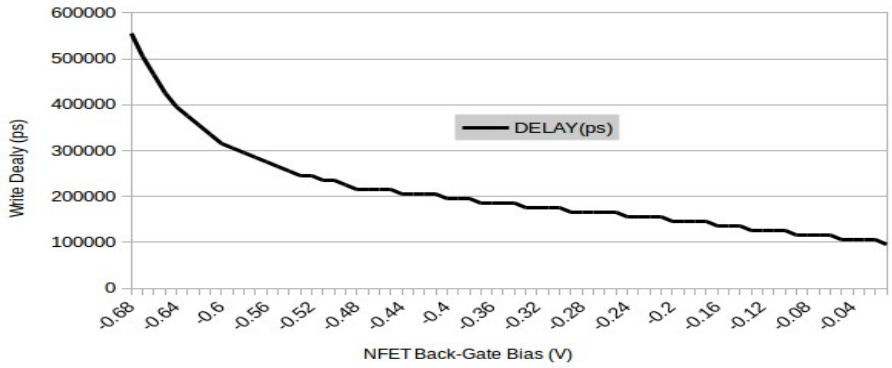

Figure 33: Write delay dependence on NFET Back-Gate biasing.

4. OPTIMIZED DESIGN PARAMETERS

By carefully analyzing the simulation results, optimum parameters for both the SG and LP FinFET SRAM cells were selected. Table 3 shows the chosen design metrics for SG and LP design schemes for optimum SNM and power-performance in comparison to the original design metrics. Using these new design metrics for both SG and LP, 6T FinFET SRAM cells are simulated and analyzed. The cell ratio of 2:1, which was selected based on the original simulation, increases the read margins. Increasing the NFET dimensions improves the read SNM for SG scheme while it slightly decreases the hold SNM and increases leakage currents. The pull-up ratio increases the write margin and the pull-up ratio of 2:1 is selected which marginally decreases hold SNM and increases the leakage currents. Increasing the supply voltage increases both read and hold SNM but at the cost of increased subthreshold leakage currents. A supply voltage of 0.6V is chosen which increases the SNMs while minimizing the increase in the leakage currents. The word-line voltage of 0.6V is chosen which only increased the read SNM. PFET back-gate bias selected was 0.6V and NEFT back-gate bias was -0.2V which provided a balanced tradeoff between stability and subthreshold leakage currents. This back-gate bias combination in LP scheme increased the read SNM as compared to the SG scheme. The simulation results using the new design metrics are tabulated in Table 4 and Table 5 for SG and LP schemes respectively which is compared with the original design metric simulation results.

Table 3: Simulation Design Metrics

Design Parameter	*Original*	*Optimized*
Cell Ratio	1:1	2:1
Pull-Up Ratio	1:1	2:1
Supply Voltage (V)	0.68	0.6
Word Line Voltage (V)	0.68	0.8
PFET Bias (V)	0.88	0.6
NFET Bias (V)	-0.2	-0.2

Table 4:Shorted Gate Design Metrics Results

Scheme	*SG*	*SG Modified*	*Percentage increase (%)*
Subthreshold Leakage (pA)	0.1803	0.2372	31.55
Hold SNM (mV)	300.84	388.52	29.14
Read SNM (mV)	139.46	401.02	187.55
Read Delay (ps)	2.782	79.99	2775.2
Write Delay (ns)	1.6	4.014	150.87
Read Energy (fJ)	1.04E-5	5.08E-6	-51.11
Write Energy (fJ)	3.71E-5	7.62E-5	105.39
Average Energy (fJ)	1.57E-5	1.93E-5	22.92

Table 5: Low Power Design Metrics Results

Scheme	*LP*	*LP Modified*	*Percentage increase (%)*
Subthreshold Leakage (pA)	0.001485	0.02633	1673.06
Hold SNM (mV)	279.62	256.78	-8.16
Read SNM (mV)	110.6	256.81	132.19
Read Delay (ps)	1152.1	1300	12.83
Write Delay (ns)	107.58	602.39	459.94
Read Energy (fJ)	7.78E-7	1.73E-6	122.36
Write Energy (fJ)	1.03E-6	2.01E-6	95.14
Average Energy (fJ)	8.28E-7	1.79E-6	116.18

5. CONCLUSIONS

Seven design metrics of 6T FinFET SRAM cells were investigated and their effects on the SNM and the performance for a SG and LP design schemes were analyzed. Based on the simulation results, a 6T FinFET SRAM cell with new design metrics is proposed with optimum SNM and performance tradeoffs.

5.1. SHORTED-GATE DESIGN

Table 4 shows the results for the modified SG configuration. The hold SNM improved by 29.14% and the read SNM improved by 187.55%. This increased noise immunity comes at the cost of both subthreshold leakage and read and write delays. The average energy for read and writes of the modified cell increased by 22.92% when compared with the original cell.

5.2. LOW POWER DESIGN

Table 5 shows the results for the modified LP configuration. The hold SNM decreased by 8.16% margin, while the read SNM improved by 132.19% margin. This increased noise immunity comes at the cost of both subthreshold leakage and read and write delays. The subthreshold leakage current increased by 25fA, the read delay by 12.8%, and the write delay by 459.9%. The average energy for read and writes of the modified cell is 116.18% when compared with the original cell.

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