IMAGE WAFER INSPECTION BASED ON TEMPLATE MATCHING

Massimiliano Barone

STMicroelectronics, Agrate Brianza, Milano, Italy

ABSTRACT

This paper presents a template matching technique for detecting defects in VLSI wafer images. This method is based on traditional techniques of image analysis and image registration, but it combines the prior art of image wafer inspection in a new way, using prior knowledge like the design layout of VLSI wafer manufacturing process. This technique requires a golden template of the patterned wafer image under inspection which is obtained from the wafer image itself mixed to the layout design schemes. First a mapping between physical space and pixel space is needed. Then a template matching is applied for a more accurate alignment between wafer device and template. Finally, a segmented comparison is used for finding out possible defects. Results of the proposed method are presented in terms of visual quality of defect detection, any misalignment at topology level and number of correctly detected defective devices.

KEYWORDS

Wafer inspection, template matching, image registration, pattern recognition, VLSI wafer images, Golden template, segmented comparison, space mapping

1. INTRODUCTION

Defects inspection plays a very important role in the very large integrated circuits (VLSI) manufacturing, because it can ensure the correctness during design and production, as well as the reliability of the microchip. The automatic inspection systems, despite of the traditional manual inspection, is mandatory for VLSI manufacturing processes due to high device number per wafer, up to 100.000 devices. Besides, a manual inspection is typically less accurate. The automatic inspection system usually consists on image acquisition and image processing. Image processing and analysis are the key to the automatic inspection system. In this paper, the surface image of VLSI wafer acquisition is made by acoustic scansion microscope, called SAM. A mapping between physical space and pixel space based on contour extraction and radon space is needed before to apply registration. The image registration algorithm based on template matching was used to achieve the alignment of the template image and the detected image in the pixel spatial position. Segmentation processing was applied to obtain the specific defects image. This method was tested by using some real image wafer on a PC.

1.1. Background

Wafer inspection systems are composed by two main stages. The first one is responsible for image registration, while the second one is for the defect detection inside the non-repetitive area found after the registration phase. The first stage can be solved in several different manners. It is possible to distinguish two different approaches: design-rule checking or image-to-image reference [10]. A design-rule system checks for the violation of a set of generic rules everywhere

on the wafer sub-images. A design-rule-based PDI prototype system has been developed by NanYang Technical University, Singapore [7] and [6]. Image-to-image-reference approach compares every pixel in the digital image under inspection with the corresponding pixel in the reference image, therefore a very accurate registration is required. Another strategy is optical spatial filtering [4] used in defect detection on masks and patterns. This method is very fast, but a major disadvantage is that small defects cannot be recognised. Wavelet technique [17] has also been used in wafer inspection. A complete review of the related literature may be found in Babian [2], Newman et al. [11], Moganti et al. [12], [15] and [16]. In addition, there are some techniques without prior knowledge like above mentioned methods. In fact, it is possible to extract the reference image directly from the wafer image. A self-reference technique was developed by Dom et al. [3], in which the comparison is made using the repeating cells in the image. This method was further developed by Khalaj et al. [8] by proposing a technique to extract the building block of repeating patterns from the acquired image. In particular, the ESPRIT algorithm [1], [5] and [9] is used in estimating the frequency components. The last stage can detect and classify defects inside the non-repetitive area with many different algorithms like described in [19-22]. In general, the detection is based on reference image or no referential approaches. Morphological processing [23, 24] and neural network [25] are without references, while methods [26, 27] need the standard image. Finally, image registration based on the SURF algorithm is another way to align the detected image and the standard image. The advantage of this algorithm is that image scaling, rotation and even affine transformation remain invariant [28].

1.2. The Structure of this Paper

In Section 2.1 the context where this solution was applied is described, with some examples of wafer images acquired and defects inside device. The full algorithm is presented in Section 2.2 including all stages of the pipeline. In Section 3, some results are shown. Finally, in Section 4, comments and conclusions about this work are given.

2. TEMPLATE MATCHING

As shown in [12] the template matching is one of possible ways for image wafer inspection. This technique is one of more robust in terms of alignment and minor different details, so it is the best for our options, see inspection algorithm taxonomy Fig. 1.
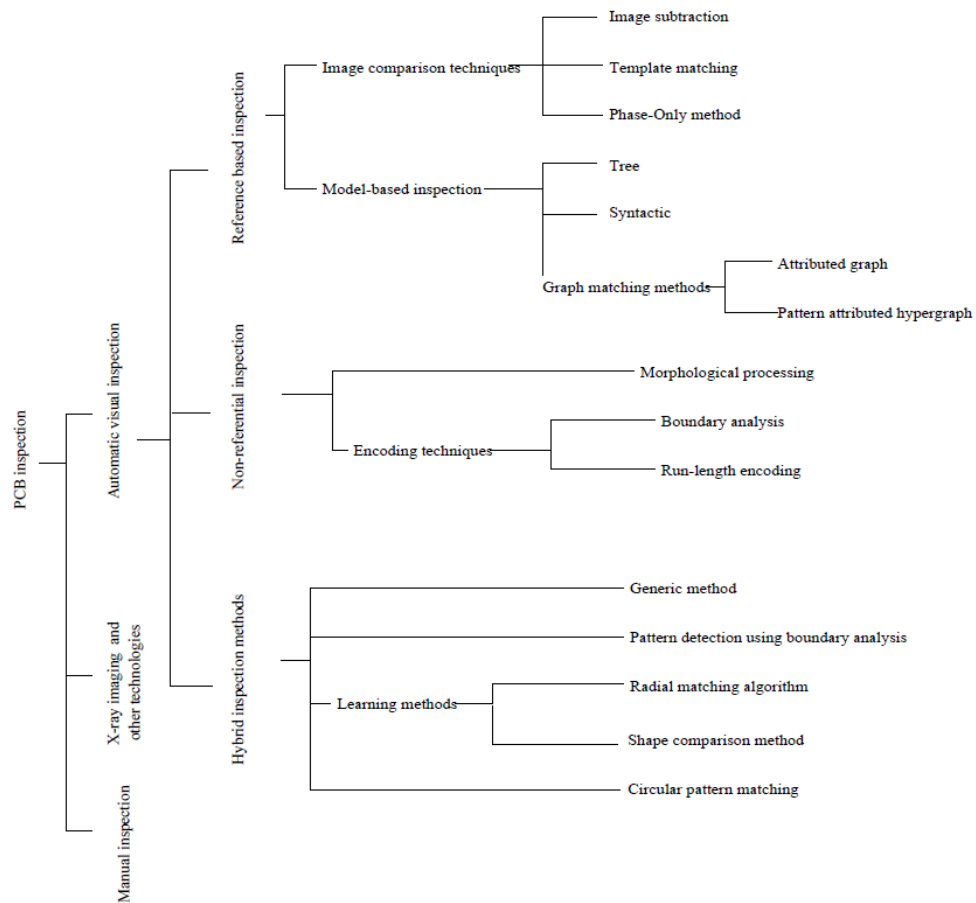
Figure 1. Wafer image inspection algorithm taxonomy.

Template Matching is just the core of this solution; the full method is composed by several stages that will be described in the sections below. The first step is defining the context where it is applied.

2.1. Context

Wafer Inspection in semiconductors field applications is applied in critical steps of the manufacturing processes and it is based on electrical test, mechanics test and image test. Image analysis is typically applied before dicing stage, see Fig. 2. Visual Inspection Technology is based on different physical principles; in particular, image processing is applicable to all following instruments: Infrared sensors, x-rays beam, electronic beam (SEM), laser beam, optical analysis and scansion acoustic microscope (SAM) beam. Machines Inspection of manufacturing processes provides images. The solution described in this paper was applied to SAM images. The devices tested were MEMS bonded; SAM inspection is used to check bonding interface integrity.
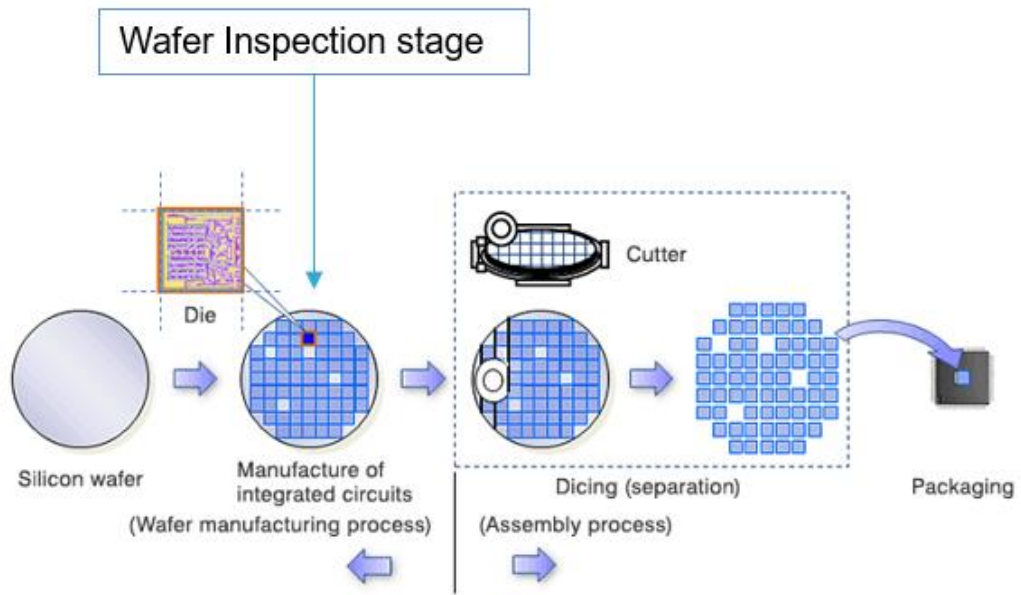
Figure 2. Wafer semiconductor process.

The goal of inspection is to detect the wrong area inside the image wafer. The defect could be large, and it could cover a lot of devices, see Fig. 3 or it could be inside each single device, see Fig. 4.
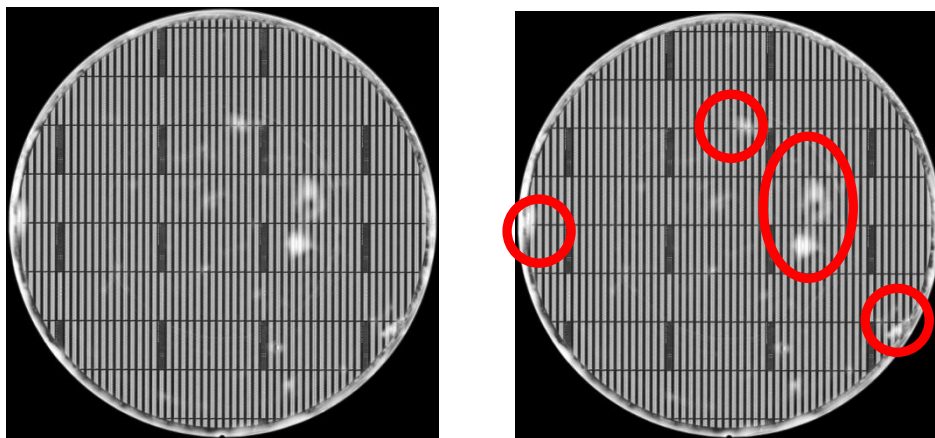

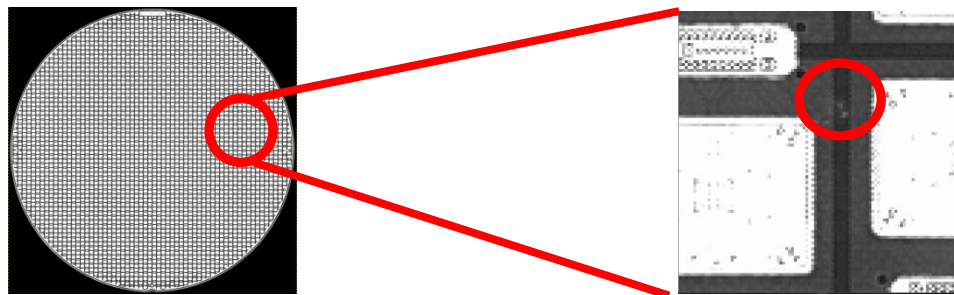Figure 3. Image Wafer by SAM with large defects.

Figure 4. Image Wafer by SAM and defect device zoom.

As we can see, the device could have a different internal shape or alternate orientation and different size like the wafer sizes. Besides the brightness of the whole wafer or of each device could be different. It means to find out a method that is invariant about all possible changes, not only about the type of defect. This requirement needs a solution more complex than a simple template matching. For this reason, there is a pipeline of stages and each of them solves a specific problem.

2.2. Overview of Template Matching Method

The solution is composed by three main stages, see Fig. 5. The first stage is the topology one, it acquires the wafer image containing all devices, then it receives the list of centre device in micron space and the image of template device. Topology is responsible for mapping the list of centre device in micron into pixel space. The next stage is about the segmentation of internal device area. The last stage applies the specific defect test for each device.
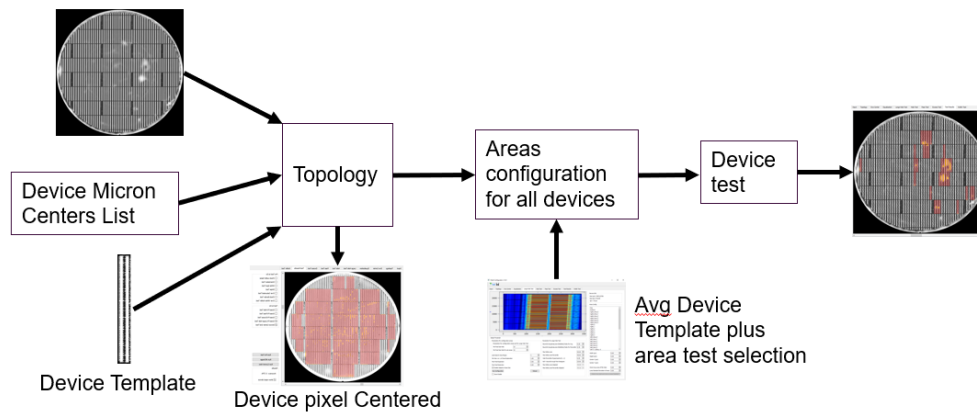

Figure 5. Template Matching Overview.

2.3. Topology

The matrix transform estimation to map centres from micron space to pixel space requires different steps, see Fig. 6. Centre and radius are estimated by Circle Fit (Taubin method) [29] based on pixel detection circumference to find the circle equation with minimum square error, so pixel circle centre and pixel radius are found. The size in micron of radius wafer is known so the scale factor micron-pixel is evaluated. The matrix transform matrix needs also the rotation estimation. Rotation angle is estimated by Radon transform (similar to Hough transform [30]) that uses vertical and horizontal pixel lines (lines detection based on Sobel filter) to count the lines with same slope rate, so the angle is found.

$$\mu mToPix = Rot * \begin{bmatrix} \dfrac{r}{R} & 0 & C_x \\ 0 & \dfrac{r}{R} & C_y \\ 0 & 0 & 1 \end{bmatrix}$$
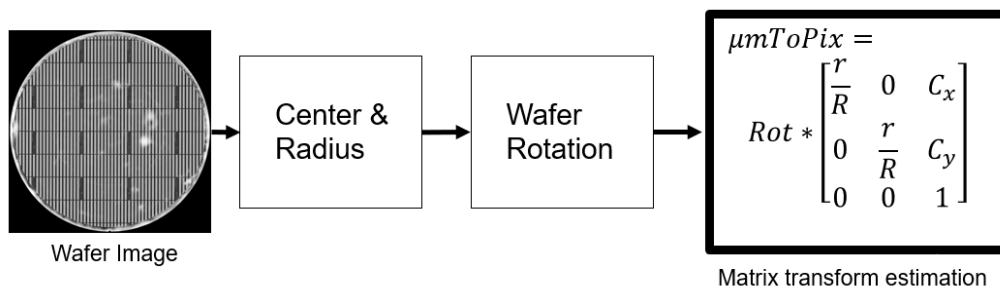
Matrix transform estimation

Figure 6. Matrix transform estimation.

The prior art strategy is different. In fact, it is based only on image wafer input and it extracts the frequency of repetitive pattern device to estimate centre device in pixel space. It does not use other information, but image wafer is the result of a design layout, so some information is known like wafer size in micron and centre device in micron, hence it is possible to re-use this information to simplify the problem.

After matrix estimation, centre device in pixel have been found, but they are not accurate. The image distortion, low resolution and previous estimations are not precise enough, so a refinement is needed. A template matching is applied starting from a sub-set of all device pixel centre using a window search large like the maximum pixel imprecision, see Fig. 7. To save computation due to thousands of devices inside wafer, just a sub-set is taken. There are a lot of possible cost functions used to calculate the similarity between template device and image device. A good cost function is the cross correlation because it does not depend on shape and absolute luminance values. In fact, the template device comes from the layout design and it is a binary image (black/white). It is not the extraction of a golden template from wafer image. In this way, more precise shape device is obtained, no defects and, thanks to scale factor previously estimated, the size in pixel space is gained. The subset pixel centre obtained is more accurate.
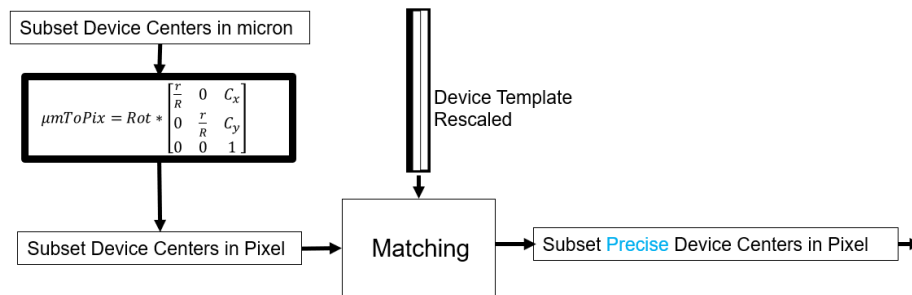
Figure 7. Template matching core.

The sub-set of new pixel centre device and sub-set micron centre device are selected, so a Matrix transform refinement based on Jacobi SVD, singular value decomposition method, is applied. The new matrix transform is more precise, but it is possible to increase precision re-using all device and a better template device for a second template matching, see Fig. 8. The second matching starts from pixel center more precise, so a smaller window search is enough. The new template comes from the average of all sub-set device, so the luminance is very similar to wafer luminance and the values are several levels of gray, no more a simple binary image. Before to calculate the average, all outliers are removed from it to have a gold template without defects. The image device with bad matching and distance between starting center and matched one are discarded. After the second matching, all pixel centers are very accurate.
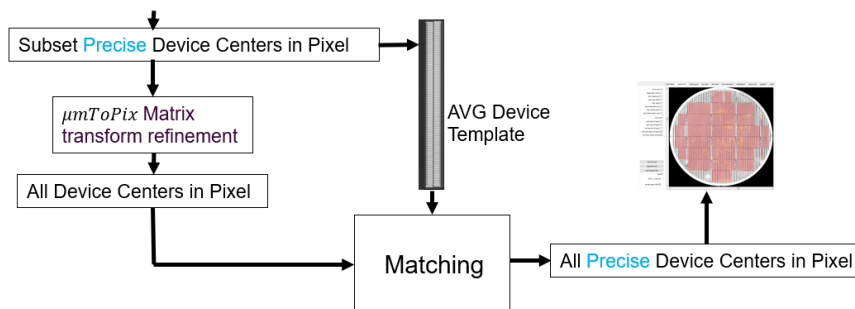
Figure 8. Second full template matching.

The image is acquired by SAM with grey levels, while template coming from design layout, so the image template is binary (black or white). A simulation of grey levels starting from a design layout would be better. A future development to estimate the grey level from design layout requires to know material property of an acoustic scansion and 3D surface shape, but it is not the focus of this paper.

2.4. Segmentation

The next stage is a manual segmentation to explore the device internally in order to find a specific defect. The whole area could be useless or not testable. The manual segmentation is applied to the average image template found. Fig. 9 is an example of manual segmentation. The tool used for inspection allows to define by user the area where to apply the test inside the device (red and blue image). The black area of the created mask isn't used to discover wrong defects and grey levels are proportional to the weights used for defects inside these positions.
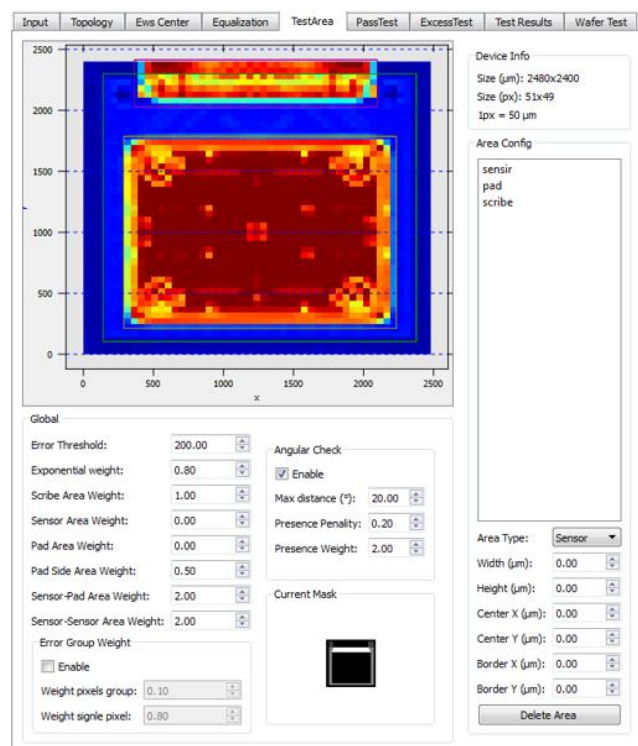

Figure 9. Manual segmentation: inside red circle (black area is ignored by device test).

The goal of above test is to find all blobs whose brightness is excessive in dark areas (blue colour in Fig. 9). For this reason, the almost white part (red colour) of the device is skipped from test.

2.5. Device Test

Before applying a specific test, it is necessary to equalize each device to use the same thresholds test for all devices, see Fig. 10. Equalization is based on a square root minimization of polynomial mapping of luminance.
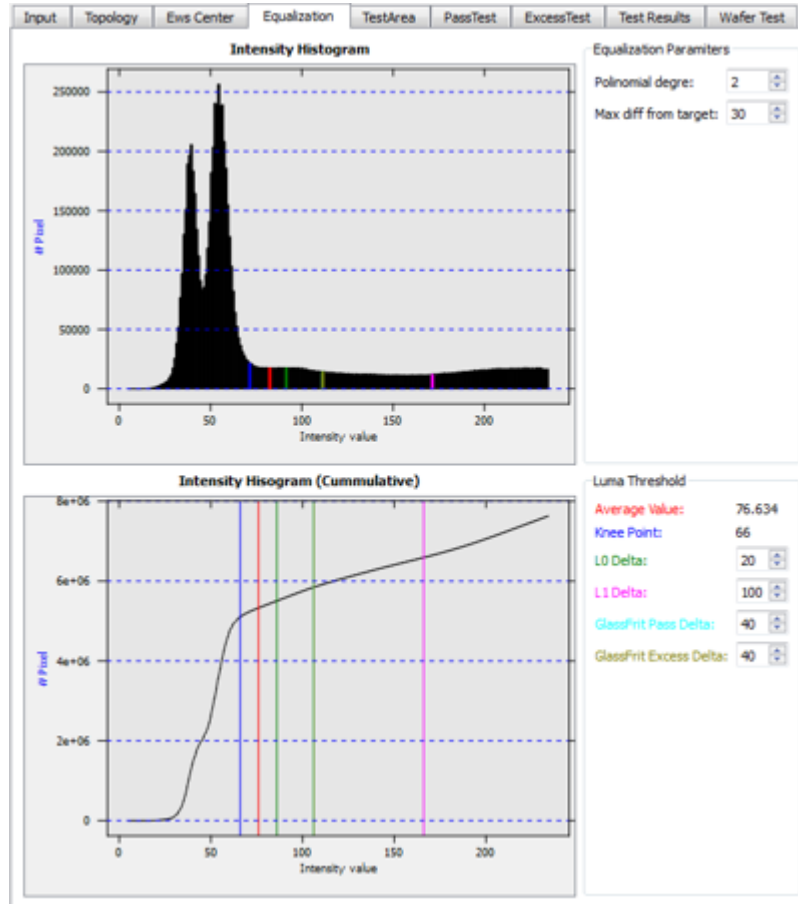
Figure 10. Histogram and cumulation of wafer luminance of all devices with knee point (blue).

Each device pixel colour is re-mapped to be like the Median template image obtained by the median of all devices well matched. The pixel colours of median template are put into a B array vector, while the associated colours of the current device, that are not too different from median one, are computed by power of N degree. So, a rectangular A matrix composed by all N power of all pixel colours of the current device associated is built. The solution consists on finding the common polyonomy of N degree that gives A*X=B. Where X contains all polynomial coefficients. The final solution to minimize the square root difference between re-mapped colours and median colours is X obtained by QR decomposition of A.

There are different types of defect, so for each type a specific test is implemented. In this paper, the focus is on searching too bright blobs inside dark area. The knee of cumulated luminance of all devices is taken as reference value, see cumulation Fig. 10. It is the boundary between dark and bright values. A device is wrong if the weighted sum of bad pixels is above the threshold defectivity level, to do that it is necessary to normalize all values into a range [knee+L0, knee+L1], see equation (1). If a single pixel value is more than knee+L0 then the pixel is classified as bad. After normalization, the weighted values are multiplied by the manual segmentation mask grey levels and finally they are summed.

$$f(x) = \begin{cases} 0 \ if \ x < KneePoint + L0Delta \\ \dfrac{x - KneePoint + L0Delta}{L1Delta - L0Delta} \quad if \ KneePoint + L0Delta < x < KneePoint + L1Delta \\ 1 \ if \ x > KneePoint + L1Delta \end{cases}$$

(1)

3. RESULTS

The results of this method are shown here. As we can see, the results are good as expected. In Fig. 11, the devices with wrong bright colors, inside the manual segmented device area, are detected and marked with a red mask. The tool analysis gives the total device accuracy or wafer yield. In this case was selected the specific test mentioned into above section about wrong bright areas. Fig. 12 and 13 show the details of test result of some wrong devices.
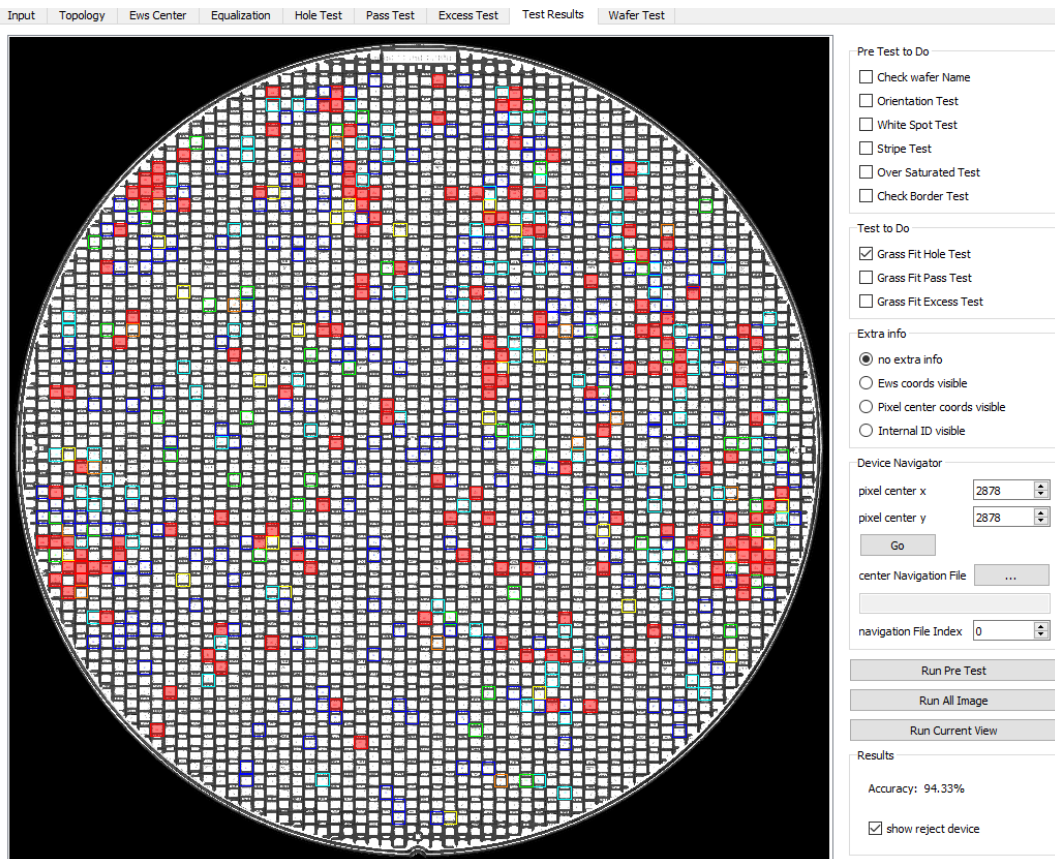

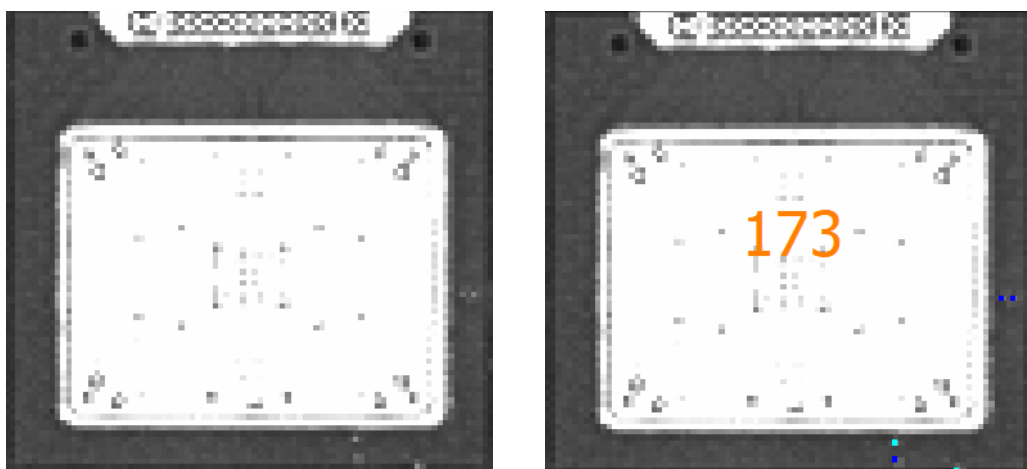Figure 11. Test result of the whole wafer, red devices are wrong.

Figure 12. Left: device before test. Right: test result not enough bad (< 200) with defectivity level printed.
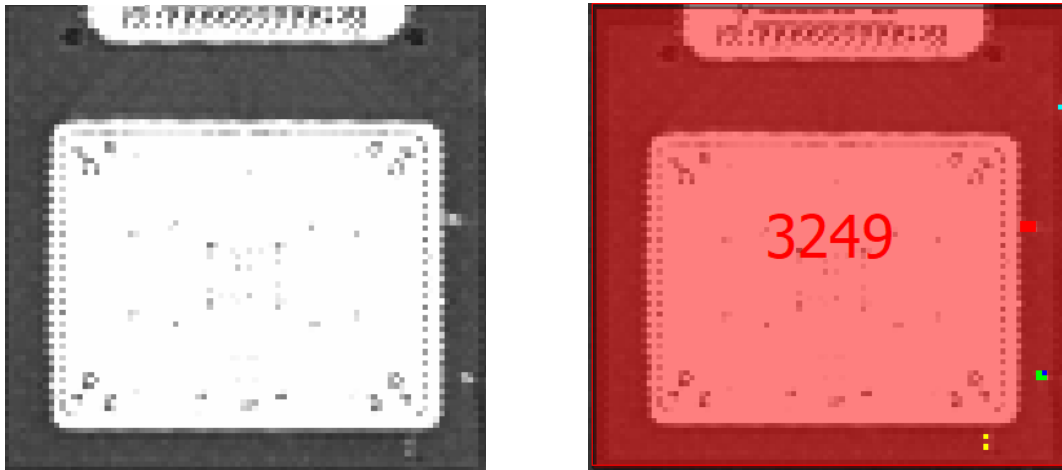
Figure 13. Left: device before test. Right: test result bad (> 200) with defectivity level printed.

In this test, the threshold of defectivity level is set to 200 and only devices with higher values are recognized as wrong. It is possible to see also single bad pixels with coloured pixels, even if the sum is under the threshold.

4. CONCLUSIONS

The worst case for wafer inspection is an image registration failure that moves all centres into a wrong position, so that also manual segmentation is misaligned. If this case happens, all devices may seem defective, but this is not the reality. Tested devices did not show this type of failure, but the shape of all verified device types is very similar, so it is not possible to demonstrate the method robustness for any kind of device shape. In addition, a thorough comparison with other image classification methods is not possible either, because a common data set of wafer images does not exist and because of confidentiality issues in the semiconductors industry. The effectiveness of the proposed method is not easy measurable, because a ground true for each tested wafer does not exist. The method is validated with human visual inspection. A small data set of tens wafers was extracted and all devices were fully manually inspected to have a ground true. Each wafer contains thousands of devices. Thousands of wafers were then analysed without a full device human inspection: only hundreds of randomly sampled devices were manually tested. The method was able to find out several small defects that human inspection could not see. Only 5% of devices were false positive and negative compared to ground true data set, but failures cases were closed to thresholds, so they can easily be classified as ambiguous cases, not real failures. State of art usually measures false positives and negatives in a binary way, but, in this type of defect analysis, the level of confidence about each single defect classification, defined as the distance from thresholds, could be a good indicator as well. If continuous values are not appropriate for failure representation, then a good quantization could be at least based on three states: false/true positive, false/true negative and ambiguous cases, where a specific metric, like the absolute value of distance from thresholds normalised by the threshold as an example, defines the range of ambiguous cases.

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AUTHORS

Massimiliano Barone

Degreed at of Polytechnic of Milan in 1997, He works for STMicroelectronics since 2000. He developed projects about computer graphics, computer vision and image processing. He attended Cammi and Made4in European projects.