DESIGN OF INTERPLANETARY OBSERVATION TERMINAL BASED ON ALL PROGRAMMABLE SYSTEM-ON-CHIP

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ABSTRACT

The drastic changes in the solar wind will cause serious harm to human life. Monitoring interplanetary scintillation (IPS) can predict solar wind activity, thereby effectively reducing the harm caused by space weather. Aiming at the problem of the lack of the ability to observe IPS phenomenon of the 40-meter radio telescope at the Yunnan Astronomical Observatory of China in the frequency band around 300MHz, an IPS real-time acquisition and processing scheme based on all programmable system-on-chip(APSoC) was proposed. The system calculates the average power of 10ms IPS signal in PL-side and transmits it to the system memory through AXI4 bus. PS-side reads the data, takes logarithms, packages it, and finally transmits it to the LabVIEW host computer through gigabit Ethernet UDP mode for display and storage. Experimental tests show that the system functions correctly, and the PL-side power consumption is only 1.955 W, with a high time resolution of 10ms, and no data is lost in 24 hours of continuous observation, with good stability. The system has certain application value in IPS observation.

KEYWORDS

Interplanetary Scintillation, Solar Wind, All Programmable System-on-Chip, AXI4, LabVIEW.

1. INTRODUCTION

Interplanetary Scintillation (IPS) refers to the phenomenon that electromagnetic waves emitted from radio sources outside the solar system are scattered by the solar wind when they pass through the interplanetary space of the solar system, causing random fluctuations in electromagnetic intensity [1]. With the continuous development of human space exploration and aerospace technology, solar wind activity monitoring and space weather forecasting are becoming more and more important [2]. The drastic changes in the solar wind can cause magnetic storms, power transmission facilities to malfunction, interfere with ground shortwave communications, satellite communications, and even threaten the safety of spacecraft and astronauts [3]. Therefore, it is of great significance to predict solar wind activity by monitoring IPS signals.

At present, the common IPS monitoring methods are divided into direct measurement and ground-based measurement. Compared with direct measurement, ground-based measurement has a wider observation scale and is more economical and effective [4]. Ground-based measurement

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modes are divided into single-station single-frequency (SSSF) and single-station dual-frequency (SSDF) and multi-station measurement. SSSF measurement mode obtains the scintillation power spectrum by means of spectrum fitting or characteristic frequency to obtain solar wind speed, such as Ooty Radio Telescope (ORT), located in India [5], and the 25-meter radio telescope in Urumqi, Xinjiang, China [6]. SSDF measurement calculates the solar wind speed by calculating the first zero frequency of the cross-correlation spectrum [7], which is more accurate than SSSF mode, such as Miyun 50-meter in Beijing, China [8]. The multi-station measurement mode can directly obtain the projected solar wind speed, such as STELab in Japan [9]. The 40-meter radio telescope at the Yunnan Astronomical Observatory in China is one of the important observation equipment for radio astronomy signals in China. Compared to Xinjiang 25-meter, Miyun 50-meter and FAST [10], Yunnan Astronomical Observatory 40-meter radio telescope is located in the south with low latitude, and can observe many radio sources that cannot be observed by other radio telescopes. According to the experience of scientists in IPS observations, when the observation frequency of radio telescopes is low, the radio source information is more abundant, such as 327MHz. Therefore, improving the receiving equipment of the 40-meter radio telescope near the 300MHz frequency band of Yunnan Observatory for IPS observation is of great significance to fill the gap in its IPS signal observation capability.

In view of the characteristics of the 40-meter radio telescope of the Yunnan Astronomical Observatory [11], the system designed in this paper is a SSSF mode. The characteristic time scale of the change of IPS signal received by a ground-based single station is from 0.1s to 10s [12]. In order to achieve long-term, stable and high-time resolution IPS signal monitoring, the system needs to have high-speed signal acquisition, high-speed cache, big data storage, high-speed processing and communication capabilities. Xilinx's proposed All Programmable System on Chip (APSoC) benefits from the high-speed interconnection between Programmable Logic (PL) and Processing System (PS) through the AXI4 bus [13]. Compared with the traditional FPGA+ARM/DSP processor architecture, the system has higher bandwidth and lower power consumption. Secondly, the data interface of PS-side is simple to implement and convenient to store. Through the cooperation of software and hardware, the system development cycle can be greatly shortened [14]. In summary, APSoC is very suitable for high-speed acquisition, processing and storage of IPS signals. Therefore, an APSoC based IPS observation scheme is proposed in this paper. The acceleration part of digital signal processing is constructed on FPGA (PL-side) to achieve the purpose of real-time IPS signal processing. A terminal parameter control program is constructed in ARM Cortex-A9 processor (PS-side) to rapidly control the device parameters of IPS observation terminal. The IPS observation data is transmitted to the host computer for display and storage through gigabit Ethernet UDP. Based on the above solution, a flexible, fast, and stable real-time observation terminal for IPS signals is realized through the cooperation of software and hardware, which provides a technical foundation for the Yunnan Astronomical Observatory to carry out subsequent IPS observations and has certain application value.

2. OVERALL SYSTEM DESIGN

2.1. Overall system structure

The system uses Digilent's Eclypse-Z7 hardware platform, and the processor is Xilinx's xc7z020clg484-1 all programmable system-on-chip, which is implemented based on 28nm Artix-7, and has 2 Cotex-A9 ARM processors, which can achieve excellent Performance to power ratio and maximum design flexibility [15], can meet the needs of real-time data acquisition and processing of IPS signals. The ADC data sampling board uses ZmodADC1410 with AD9648 as the core. The sampling frequency of ZmodADC1410 is 100MHz, and it can obtain two 14-bit

signals at the same time. The programmability and high resolution of this device make it a reliable choice for the receiving end of radio astronomy signals, and the program gain control. ZmodADC1410 and Eclypse-Z7 used in this system realize high-speed connection through SYZYGY standard interface. Compared with Pmod, SYZYGY standard interface has higher speed and bandwidth, and is smaller and cheaper than FMC interface. This paper adopts the system structure shown in Figure 1 to realize the IPS observation terminal.

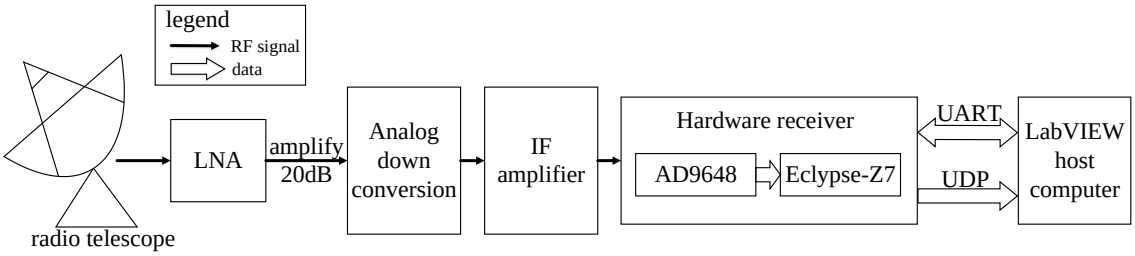

Figure 1. System overall structure block diagram

Firstly, the system uses a low noise amplifier (LNA) to amplify the weak radio signal received by the 40-meter radio telescope. Then, the analog downconversion module is used to downconvert the received 327MHz analog signal to obtain a 10MHz signal. Then, the intermediate frequency amplifier is used to amplify the intermediate frequency (IF) signal. The digital signal is input to PL-side of APSoC through AD9648. Real-time power calculation and superposition of the signal are carried out in PL, and then the superposition power data is averaged and stored in system memory through AXI4 bus for reading by PS-side. When the data is read, PS-side transmits the data to the LabVIEW host computer software in the form of Gigabit Ethernet UDP protocol for real-time display and storage. In addition, the system can also configure the gain, channel and coupling coefficient of the AD9648 in the hardware receiver through serial communication in the host computer application and issue control commands.

3. SYSTEM SOFTWARE AND HARDWARE DESIGN

In this paper, the main functions of APSoC are real-time processing and high-speed transmission of digitalized IPS signals, and flexible configuration of AD9648 parameters, including PS-side and PL-side. The PL-side is developed by Verilog with the HDL integrated development environment Vivado2019.1 provided by Xilinx company, and the PS-side is developed by C language in SDK2019.1.

3.1. PL-side system design

In order to achieve the high-speed acquisition and processing of IPS signals and ensure the stability of the system, the basic framework of IPS signal processing is constructed in the PL-side of APSoC. As the characteristic time scale of IPS signal changes is from 0.1s to 10s, in order to improve the system time resolution, the PL-side is used to calculate the power of signal sampling points within 10ms and calculate the average. Because the data interval between sampling points is very small, reaching nanosecond level, the process of power calculation and superposition needs hardware acceleration at PL-side. Then, the power data is mapped to the memory address through AXI4 bus for subsequent reading by PS-side.

According to the above scheme, this paper designs a Block Design project in Vivado. The overall block diagram of the system is shown in Figure 2. These include: IPS Data Processing module (Math IP), ZmodADC Control IP and AXI ZmodADC IP, Processor System Reset IP, AXI

Interconnect and ZYNQ core modules. In order to make the main signal easily visible, the ARESETN reset signal in the default figure is connected to Processor System Reset IP, and clock signal is also connected by default.

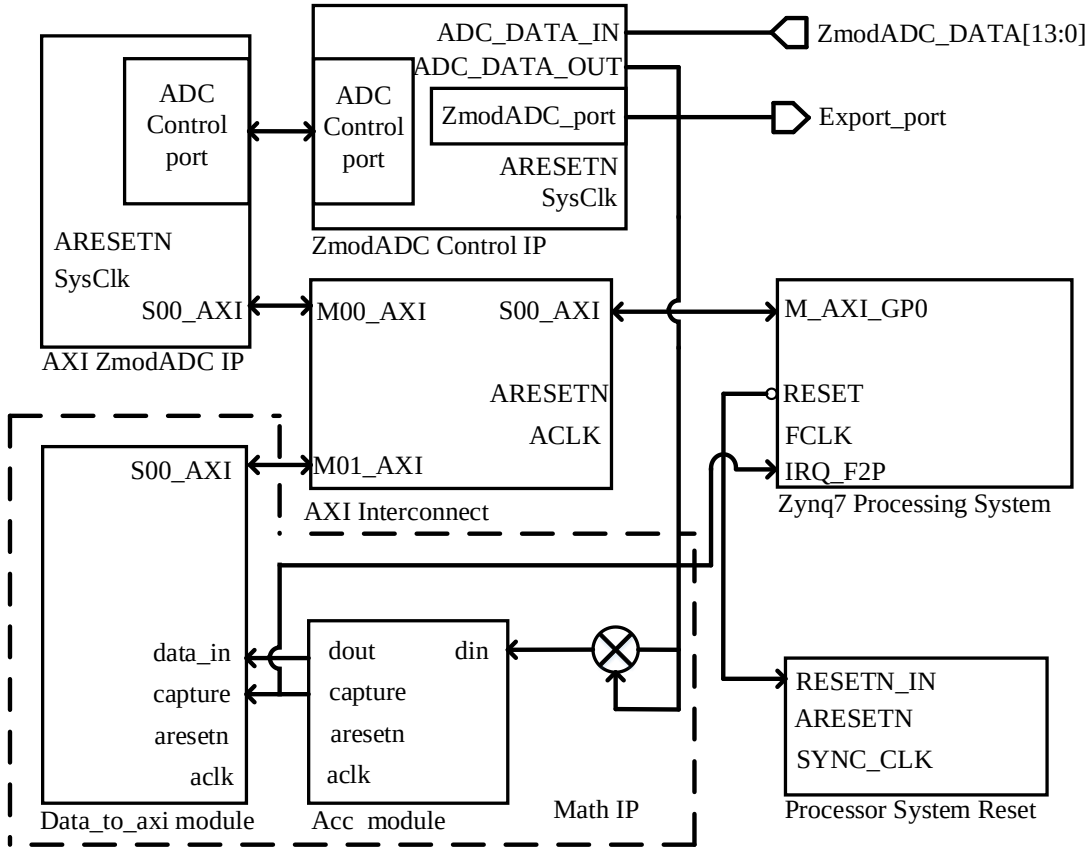

Figure 2. PL-side Block Desigen block diagram

The ZmodADC1410 Control IP core in Figure 2 is an ADC Control module, whose function is to realize data interaction between ZmodADC1410 and APSoC. PS-side can also indirectly Control the ZmodADC1410 Control IP by reading and writing the register of AXI ZmodADC IP via AXI4 bus. The two IPS are connected through a set of ADC Control ports, officially provided by Digilent. The ZYNQ7 Processing System is the hard IP address of the Cotex-A9 ARM processor. After the system was built, the global clock on PL-side was set to 100MHz in the ZYNQ IP core, that is, synchronous clock domain, in order to avoid the metastable problem caused by cross-clock domain. In addition, the serial port UART0, Ethernet port ENET0, GPIO, and the interrupt pin IRQ_F2P from PL to PS need to be enabled in the ZYNQ IP core for subsequent use. The AXI Interconnect IP realizes the topology of AXI bus, and connects M_AXI_GP0 of ZYNQ IP core to S00_AXI of AXI ZmodADC IP and Math IP, so as to realize the data communication between PL-side and PS-side.

The Data processing part (Math IP) consists of the power calculation module, power superposition module, and Data_to_axi IP to complete the calculation and superposition of the IPS signal power, and transmit the data to the PS-side for subsequent processing. Since dB is commonly used as a unit in engineering, logarithmic operation should be performed on the raw data. Since the power value to be sent is the average power value within 10ms, the amount of data is small, and a large number of LUTs will be consumed if the logarithm operation is

implemented using the PL-side. In order to save logical resources on PL-side, logarithm operation is carried out on PS-side. The schematic diagram of Math IP is shown in Figure 3. The detailed description of each part is as follows.

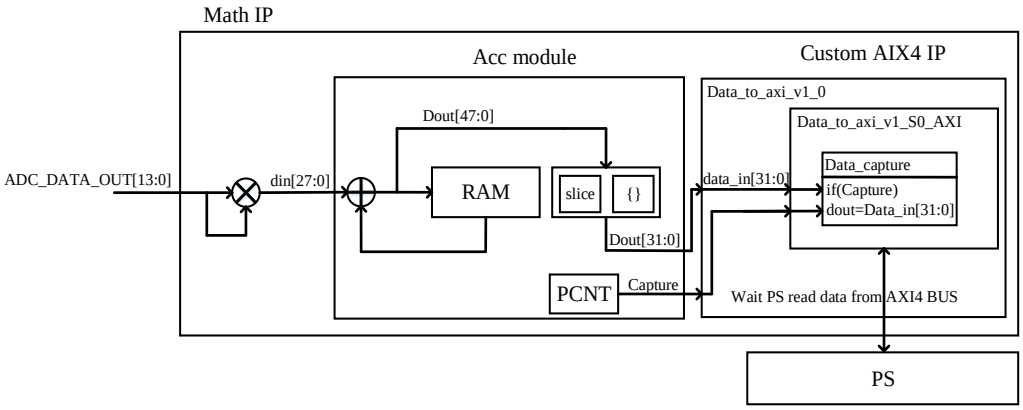

Figure 3. The schematic diagram of Math IP

3.1.1. Power calculation module

In order to calculate the IPS signal power, the amplitude of the sampling point needs to be squared to obtain the instantaneous power value of the point. The multiplication operation uses the Multiplier IP core. The data width of the ZmodADC Control IP output to the module is 14 bits. Therefore, the Multiplier IP input data width should be set to 14 bits for signed multiplication.

3.1.2. Power superposition average module

The function of this module is to calculate the average value of power superposition within 10ms. As shown in Figure 3, the superposition operation is realized by a RAM and adder. Set a PCNT counter, when the PCNT count reaches 1000000, Capture signal is raised, output result of the superposition named Dout[47:0], by intercepting data 28 bits higher to get the average signal power within 10ms. In order to adapt to AXI4 bus bit width, the power data is added to 32 bits and output to a custom AXI4 IP named Data_to_axi. In addition, the Capture signal also triggers an IRQ_F2P interrupt, which triggers a data read transaction on PS-side.

3.1.3. Data_to_axi module

In order to realize the data transmission between PL-side and PS-side, a custom AXI4 IP is created through the Tools option in Vivado, and add user logic. When the IP creation is completed, the IP is packaged for integration into Block Design. The IP hierarchy is shown in Figure 3. The Data_to_axi module internally instantiates a module named Data_capture. Whenever the Capture signal of the power superposition average module is raised, the 32-bit input data Data_in is loaded into the second read register of AXI4 IP at address 0x43C0008. The PS-side can read the value in the register by xil_In32() function reading the address.

3.2. PS-side program design

The PS-side clock frequency is 667MHz. In addition to logarithm taking and data packing operations, in order to achieve flexible parameter control, that is, to control the sampling channel, channel gain and coupling coefficient parameters of AD9648 through serial port, and to realize the functions of calling other IP cores and controlling gigabit Ethernet for data communication, it is necessary to build the PS-side operation program in the Cotex-A9 ARM processor. The main program flow of PS-side is shown in Figure 4.

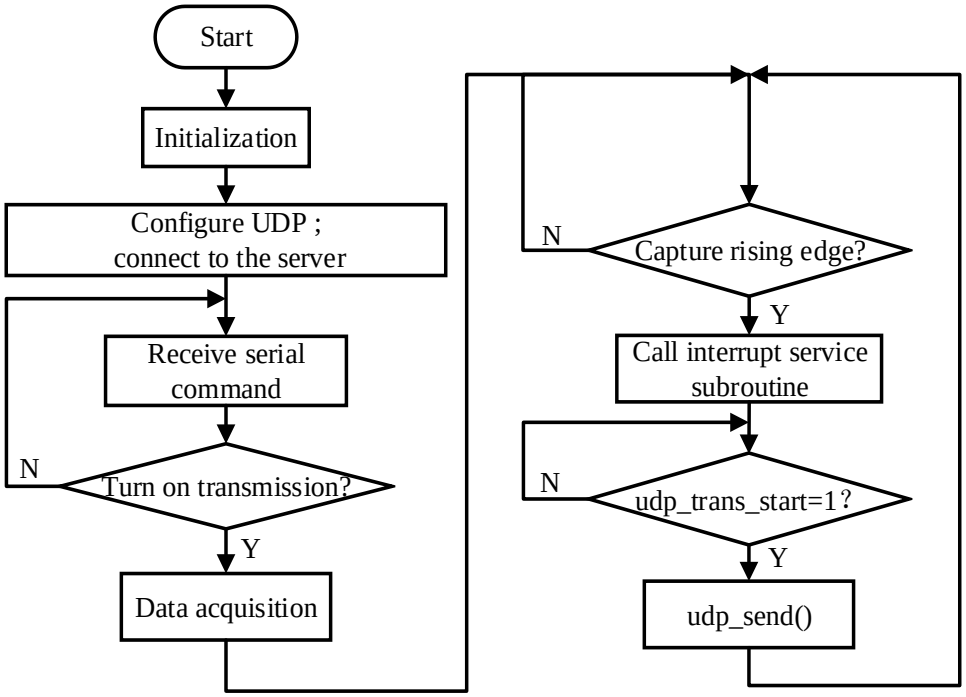

Figure 4. The main program flow chart of PS-side

Initialization includes the initialization of serial port, SPI, GPIO, ZmodADC1410 and LwIP (Light weight IP). The serial port uses uart0 of PS, and the baud rate of the serial port is 115200bps. ZmodADC1410 is initially set to channel 1, low gain mode, and the coupling coefficient is 0. Use the Lwip211 library integrated in SDK to program UDP communication.

After the initialization step is completed, configure the UDP related functions and connect to the server. When the serial port receives the transmission start command, enable AD9648. When Capture, the power data capture signal at the PL-side, is on the rising edge, the PL-to-PS interrupt is triggered. In the interrupt service subroutine, PS uses the xil_In32() function provided in xil_io.h file of SDK to read the power value stored in the system memory at the PL-side. Since the width of this data is 32 bits, after logarithmic operation, the width must be less than 16 bits. Construct data packets with the data type as uint32. Store the power data 16 bits lower and the data count 16 bits higher. After packing data packets, store them in udp_send_buffer to wait for sending, and the interrupt returns. In order to reduce the burden of data display and storage in the host computer, the sending buffer is set to send data once every 100 data is stored, When the sending buffer is full, udp_trans_start=1, the main program calls udp_send() function to transfer data to the LabVIEW host computer. In order to enable the host computer to distinguish one frame of data, set udp_send_buffer[0]=0xAABBCCDD, udp_send_buffer[101]=0xDDCCBBAA,

respectively, as the frame head and frame end. Since the data type of the buffer is uint32, a frame of data has a total of 408 bytes.

4. HOST COMPUTER APPLICATION DESIGN

In this paper, the visual programming software LabVIEW2018 of NI Company is used for the host computer application development. The main functions include:

(1) Serial port communication and UDP communication between the host computer and APSoC,
(2) Display and storage of IPS power data.

The host computer application adopts the string state machine program architecture, which is mainly composed of conditional structure and while loop. The program performs the corresponding state according to the string content by conditional structure. The UDP part and serial part of the application program of host computer are controlled by two state machines. The program flow chart of the LabVIEW host computer application is shown in Figure 5.

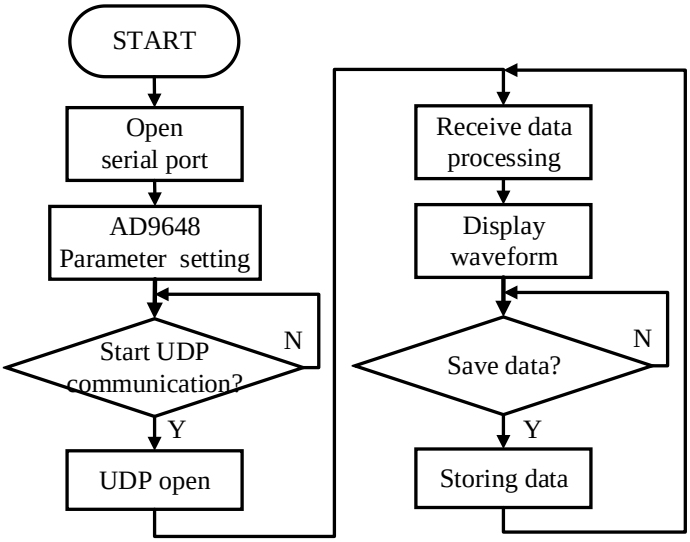

Figure 5. The program flow chart of the LabVIEW host computer application

First, Set and initialize the serial port, When the serial port runs normally, SERIAL_STATE indicator turns green. When the RX buffer of the serial port receives the response "Initialization successful" that APSoC is initialized, it can set the sampling channel, sampling length, channel gain, coupling coefficient and other parameters of AD9648 through the sending buffer according to the message prompted by the serial port. After the parameters of AD9648 are set, click SEND to send the parameters to APSoC. The PS-side of APSoC indirectly controls Zmod Control IP through AXI4 bus, so as to complete the flexible configuration of AD9648 parameters. After sending the start UDP transmission command, set the UDP target address and port, click to OPEN UDP CONNECT, UDP_STATE indicator turns green, you can see the IPS power signal sent from APSoC. Click SAVE DATA to obtain IPS power data saved in .jpg and .txt format in the specified path, which is convenient for subsequent analysis and use.

5. SYSTEM TEST AND RESULT ANALYSIS

5.1. Serial port and UDP function test

To verify the serial port and UDP functions, test according to the following steps:

Step 1: Set the IP address of the Eclypse-Z7 hardware platform to 192.168.1.150, port 8080, the IP address of the LabVIEW host computer to 192.168.1.151, port 8081, and connect the board and the host computer to the same local area network. Step 2: Open the LabVIEW host computer, select right COM number, set baud rate to 115200bps, open it. Step 3: Power on the board and keep the default AD9648 parameter. Step 4: RIGOL DSG815 signal generator is used to generate a signal with a power of -23dBm and a frequency of 327MHz, which is connected to the system. Step 5: Open the UDP connection and use the Wireshark to capture packets and compare the packets with the UDP receiving buffer of the host computer. The experimental results are shown in Figure 6 and Figure 7.

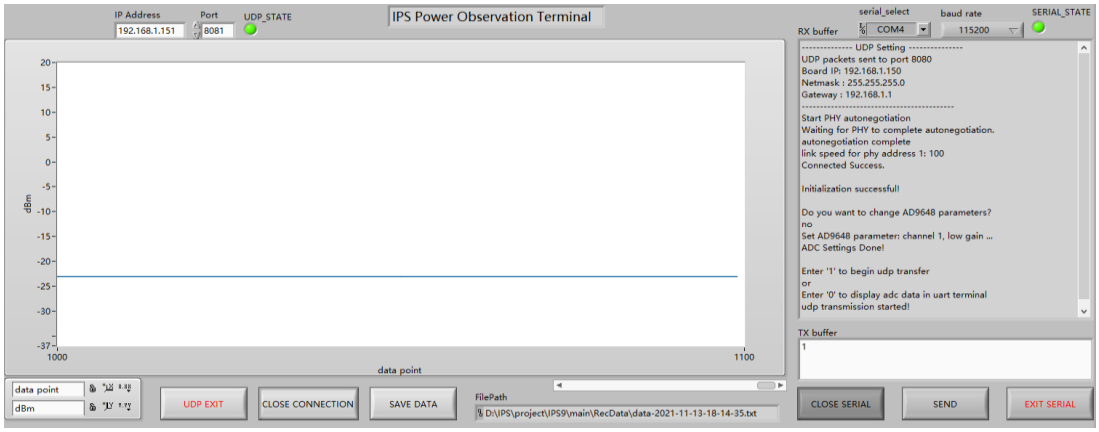

Figure 6. The LabVIEW host computer interface

As can be seen from Figure 6, at the moment when the board is powered on, the RX buffer of the serial port prints out “Initialization successful”, and sends the command, serial port also responds, which verifies that the serial port function is correct.

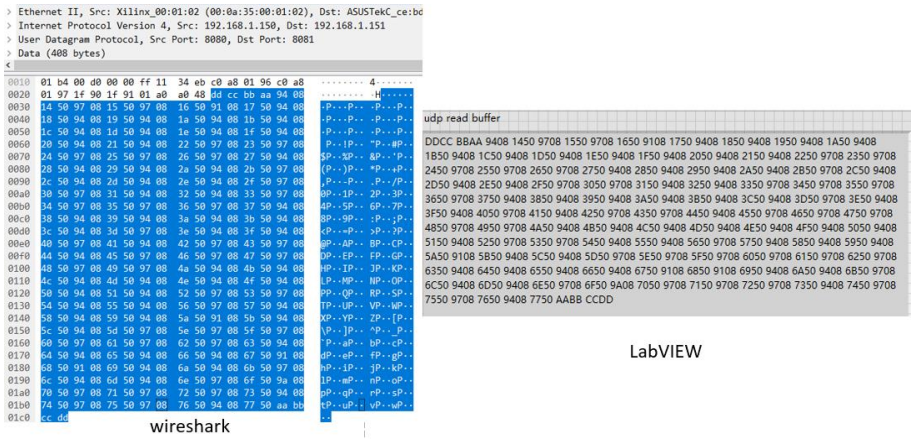

Figure 7. Comparison between Wireshark UDP packet capture and UDP read buffer of the LabVIEW host computer

As can be seen from Figure 7, the data in the Wireshark UDP packet capture and the LabVIEW host computer's UDP read buffer are exactly the same, indicating that the host computer successfully received the UDP packet from Eclypse-Z7, and the IPS signal power in Figure 6 is indeed -23dBm. It also verifies the correctness of the system function. The above experiments verify that the serial port and UDP functions of the host computer are correct and meet the design requirements.

5.2. Time resolution test

Since the characteristic time scale of IPS signal changes is 0.1s to 10s, in order to meet the requirements of the time resolution of the system in practical applications, it is necessary to test the time resolution of the system. Adjust the RIGOL DSG815 signal generator to a single step sweep mode, 30 points, 100ms dwell time, send a sine signal from -10dBm to -40dBm, and connect to the system for testing. Plot the output data of the system, as shown in Figure 8.

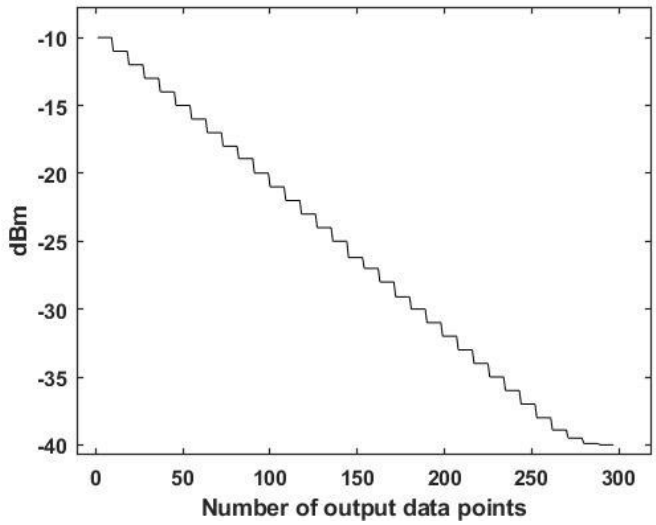

Figure 8. Single step scan mode system output data

As can be seen from Figure 8, when the signal power attenuates from -10dBm to -40dBm, the power value will change in real time with the change of the input signal. Secondly, when the time of a single step scan is 3s, the system output data points are 300 points, so the system time resolution can be calculated as 10ms. After repeated measurements using the above method, the system time resolution is 10ms, so it meets the design requirements.

5.3. Stability test

During the monitoring of IPS data, if the system has problems in the calculation, transmission, and storage of IPS power values, resulting in the omission of data points, the observation values of IPS data in this section will be meaningless and the precious observation time of radio telescopes will be wasted. In IPS observation, the longest observation time is only from sunrise to sunset [16], about 12 hours. In order to test the stability of the system, RIGOL DSG815 signal generator is used to send signals with power of -35dBm and frequency of 327MHz. Under the temperature condition of 20℃, continuous observation for 24 hours is carried out. Save system output data to a .txt file. According to statistics, there are 8640,000 data points in the final text file. The data waveform is drawn by MATLAB, as shown in Figure 9 (a). The first 1000 points

were intercepted and the fast Fourier transform was performed on the data within this time scale to obtain the IPS scintillation power spectrum with an integral time of 10s, as shown in Figure 9 (b).

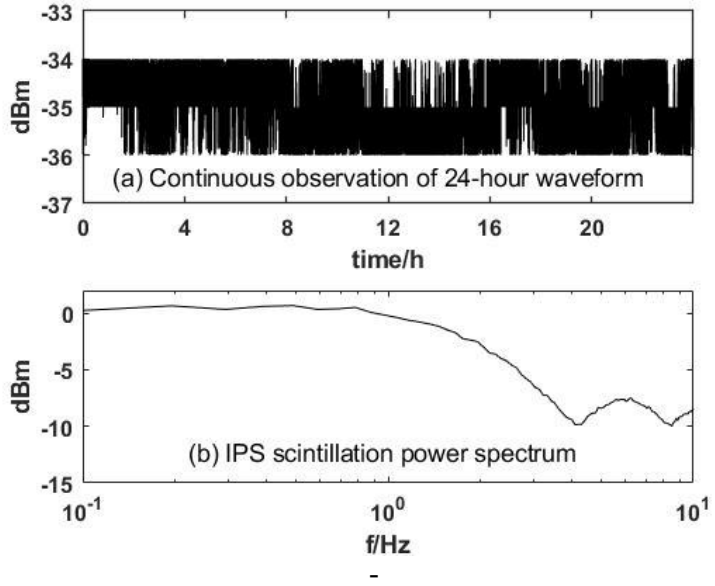

Figure 9. Continuous observation data and IPS scintillation power spectrum

As can be seen from Figure 9 (a), when the signal power is weak, the continuous observation results basically present a straight line. After calculation, the signal power fluctuation is about ±1dBm, indicating that the system has good test accuracy and stability, and meets the design requirements.

5.4. Programmable logic resource usage and power consumption

This system is based on Xilinx's XC7Z020CLG484-1 all programmable system-on-chip. In Vivado, after the PL part of the system is designed according to section 2.1, the final PL-side resource usage is shown in Table 1.

Table 1. PL-side resource usage

Resource	Utilization	Available	Utilization%
LUT	5552	53200	10.44
LUTRAM	513	17400	2.95
FF	8965	106400	8.43
BRAM	24.50	140	17.50
DSP	2	220	0.91
IO	32	200	16.00
BUFG	7	32	21.88

As can be seen from Table 1, BRAM and BUFG are the most used resources on PL-side of the system, accounting for 17.5% and 21.88% of the total resources respectively. DSP is the least used resource, and only 1% of the total resources are used, indicating that the system has a large amount of resource margin and good scalability. And the power analysis tool in Vivado was used to evaluate the power consumption of the PL-side of the system. The power consumption was 1.955W in actual operation, which met the design requirements of low power consumption of the system.

6. CONCLUSIONS

In this paper, we propose an IPS observation system based on Xilinx Zynq7000 APSoC. The system takes XC7Z020CLG484-1 as the core, realizes the real-time processing and transmission of IPS power signal by means of hardware and software cooperation, and realizes a good human-computer interaction interface based on LabVIEW. Experiments show that the system has high integration, high time resolution and good stability. The work in this paper has laid a technical foundation for the 40-meter radio telescope of Yunnan Astronomical Observatory to carry out IPS observation, and has certain application value. Next, we will consider integrating the post-processing of IPS signals into APSoC to improve system performance.

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