FROM FPGA TO ASIC IMPLEMENTATION OF AN OPENRISC BASED SOC FOR VOIP APPLICATION

Faroudja Abid and Nouma Izeboudjen

Microelectronic and Nanotechnology Laboratory, Centre de développement des technologies avancées, Algiers, Algeria

ABSTRACT

ASIC (Application Specific Integrated Circuit) design verification takes as long as the designers take to describe, synthesis and implement the design. The hybrid approach, where the design is first prototyped on an FPGA (Field-Programmable Gate Array) platform for functional validation and then implemented as an ASIC allows earlier defect detection in the design process and thus allows a significant time saving. This paper deals with a CMOS standard-cell ASIC implementation of a SoC (System on Chip) based on the OpenRISC processor for Voice over IP (VoIP) application; where a hybrid approach is adopted. The architecture of the design is mainly based on the reuse of IPs cores described at the RTL level. This RTL code is technology-independent; hence the design can be ported easily from FPGA to ASIC. Results show that the SoC occupied the area of 2.64mm². Regarding the power consumption, RTL power estimation is given.

KEYWORDS

ASIC; FPGA; Opencores; OpenRISC; SoC; VoIP

1. INTRODUCTION

The decision between FPGA and ASIC as an implementation media is primary derived by the targeted application and the required performances. Several issues are considered for this choose namely, power consumption, area usage, device size, design cost and time to market. FPGA platforms offer reduced NRE (Non Requiring Engineering) cost and short time to market; they are widely used in several applications where a complete system can be implemented on a single device. However the FPGA presents a major drawback, which is the increase in power consumption compared to ASIC or full custom design. Nevertheless a hybrid approach that combines the two mediums, where an FPGA is used for prototyping and then the design is ported on ASIC, can be a solution for designers looking for rapid and easy solution for functional validation. On the other hand, when migrating from FPGA to ASIC, systems designer have to consider several technical areas during the design phase [1]. Among these criteria, the RTL description of the IP cores included in the design. These RTL descriptions should be technology-independent, thus the design architecture can be mapped to an ASIC or FPGA; and the migration between the two technologies can be done with few RTL code changes. The use of FPGA for prototyping allows earlier defect detection in the design process and significant time saving.

In this paper we present the OpenRISC [2] based SoC for VoIP application; the design architecture is based on technology-independent building blocks described at RTL level. The design is first prototyped on an FPGA platform for functional validation [3, 4] and then implemented as an ASIC. A few works emerged from industrial and academic researches to design SoC based on soft processor for VoIP application. Among these implementations, the IP04 based Blackfin processor by David Rowe, from Rowetel [5]; he gives an open hardware

implementation which is used by Dan Amarandei et al. for Wideband VoIP Middleware [6]. Another implementation based Xilinx PowerPC processor is given by Stelios Koroneos from Digital OPSIS [7]. However the proposed solutions are based on proprietary processors that are technology dependent. In our work we have used portable building blocks from Opencores to build an OpenRISC processor based SoC. The OpenRISC soft processor can be mapped to an ASIC or FPGA with few RTL code changes when migrating between FPGAs and ASIC, whereas the others embedded processors like Blackfin, MicroBlaze and PowerPC are proprietary and are not available in the ASIC technology. By using IP cores from Opencores to design a SoC, designer are able to prototype their system on FPGA platform with ASIC perspective. In [4, 8] we presented FPGA implementation of the VoIP architecture based OpenRISC processor. Herein we expose the ASIC design and implementation of that SoC. The purpose behind ASIC porting is reducing power consumption, which is a critical issue in SoCs targeted for VoIP application.
This paper is organized as follow: In Section II, the related works regarding ASIC implementation of the SoCs based OpenRISC are given. Section III deals with the FPGA and ASIC advantages and drawbacks. In Section IV, the technology-independent approach is presented. The FPGA prototyping of the proposed SoC architecture is presented in Section V. Section VI exposes the ASIC implementation of the designed SoC; the synthesis results in term of area utilization and power consumption are exposed in this section.

2. RELATED WORKS

Several works regarding the OpenRISC based ASIC implementations, where the design was implemented as a standard cell ASIC using diverse technologies are reported in the literature. In [9] James Tandon has developed a system used to measure temperature maps, and power supply noise variation across a chip on remote devices through the custom protocol. The system includes the OpenRISC core, I2C interface, Ethernet 10/100Mbit, UART, RAM and a boot ROM. The system was prototyped using Altera StratixIII FPGA and then implemented as a standard cell ASIC using the Rhom 0.18 μm process technology. The operating frequency is of 100 MHz and a chip size of 25mm². In [10] the authors developed a SoC that run the uClinux distribution, the ASIC was targeted for the frequency of 200MHz and has been designed using the TSMC 0.13μm process technology, the system was prototyped using Xilinx Virtex2 FPGA. Others standard cells based implementations of the OpenRISC processor as a chip are reported in [11-13]. In the work exposed in [12], the OpenRISC was implemented as a chip using the UMC 13μm technology process, with the operating frequency of 100 MHz. In [13], the OpenRISC with 8 KB data cache and 8 KB instruction cache was synthesized using a 130nm process, the author stated that "When optimized for area, the processor had an area of 2.16 mm² and a maximum frequency of 36 MHz. When optimized for speed, the area was 2.20 mm² and the maximum frequency of 178 MHz". Other implementations based on structured ASIC [14, 15] which is an intermediate technology between FPGA and ASIC; where a portion of silicon is reused were also considered [16, 17]. In [16] the ASIC has been designed using the TSMC 0.18 μm process technology with the structured ASIC approach, the operating frequency is of 90 MHz and a chip size of 13mm². Commercial companies like Flextronics International and Jennic Limited manufactured the OpenRISC as part of an ASIC. The technology-independent criteria and a portable RTL code of the OpenRISC make it suitable for, mainly, designs that are prototyped on FPGA platform with an ASIC perspective. It is noticeable that CMOS standard cell implementation is a widespread approach for ASIC designs, the structured ASIC approach remain not widely adopted.

3. FPGA AND ASIC ADVANTAGES AND DRAWBACKS

3.1. FPGA advantages and drawbacks

FPGAs are reprogrammable platforms, widely used in various designs and divers target applications. They are progressively used as final product platforms for low volume production. In FPGA based system design, there is no manufacturing turn around time, thus the design can be tested and evaluated quickly allowing shorter development cycle, short time to market and lower NER costs. In addition there is no mask making compared to ASIC. Regarding the CAD (Computer Aided Design) tools, the FPGA vendors provide tools that help designers to undertake the steps involved in the FPGA design flow. Among them the ISE software from Xilinx and Quartus II from Altera, these tools are available in low end version for free download. The full version are also available for reasonable fee compared to the ASIC tools cost. However when the design is targeted for low power application and high volume production, the size, power consumption and cost increase. This presents a major drawback which limits the FPGA platforms application to low volume production compared to ASIC. Regarding the FPGA design flow, it is usually a GUI (Graphical User Interface) based tool. Herein the development tool used for the design and implementation is the ISE (Integrated Synthesis Environment) Xilinx 13.1 tool, which is used for all steps involved in the design flow; it includes synthesis and Place&Route.

3.2. ASIC advantages and drawbacks

ASIC are IC (Integrated Circuit) designed for specific applications and a customized hardware implementations of the design. They can be classified to three major parts, namely, the full custom based ASIC that is highest performance and small size however it is a more complex and cost consuming. Secondly, the semi custom ASIC based on gate array and standard cell. The third type is structured ASIC [14, 15]. ASIC implementation allows low power consumption, low cost for important volume production, high speed and smaller die size that leads to board size reduction. In opposite to FPGA designs that are digital only, ASIC technology allows analog circuit and mixed signal design implementations. For power optimization there are several techniques such as clock gating, multi-Vth, operand isolation, which can be used in ASIC implementation. These techniques are, generally, not possible on FPGA. The drawbacks of ASIC are mainly the long development cycle, thus important time to market. The NER and CAD tools are significantly high cost. The verification of deep sub-micron effects is not required in FPGA, whereas this verification is required in ASIC.

4. TECHNOLOGY INDEPENDENT APPROACH

4.1. Technology-independent approach concept

The technology-independent approach is based on the reuse of portable building blocks described at RTL level for SoC design. This approach omits the reference to the target technology, this criteria allows portability of the design based on the technology-independent IP cores, from ASIC to FPGA or vice versa. By adopting this approach, SoC designer leverages, in one hand, the reusable propriety of these IPs, thus a new SoC can be created by adding, dripping or modifying a new core, this reuse process facilitates the rapid creation and verification. In the others hand designer are able to prototype their design into FPGA platform with an ASIC perspective. Figure 1 schematizes the technology-independent approach.

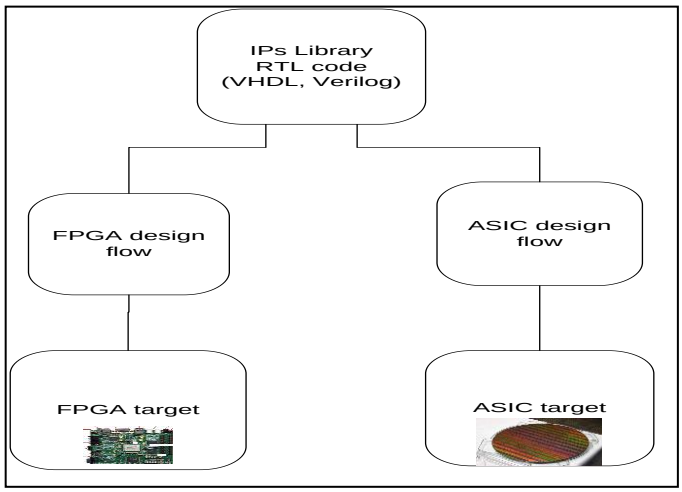

Figure 1. Technology independent approach scheme

4.2. Design architecture

Figure 2 displays the overall architecture of the proposed SoC for VoIP application. From the hardware viewpoint the architecture of the design is based on the IP reuse strategy [4] that facilitates the rapid creation and design verification process and allows lower design cost. The design includes a 32bit RISC processor core and a set of technology-independent elements needed to provide VoIP functionality. Elements are mainly, the MAC/Ethernet (connection is established by this IP), the debug unit for debugging purpose, a memory controller and Universal Asynchronous Receiver Transmitter (UART). An AC97 controller core is also selected and added for audio processing application. The designed SoC was firstly prototyped on Xilinx Virtex5 FPGA for functional validation. The details of the proposed SoC architecture and the system prototyping were presented in previous works [4, 8].

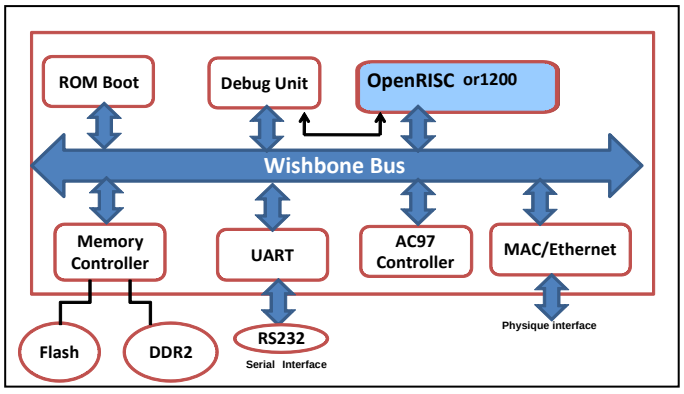

Figure 2. VoIP SoC Hardware architecture

5. FPGA PROTOTYPING

5.1. FPGA design flow and tools

Figure 3 illustrates the FPGA design flow, from functional specifications to FPGA configuration. FPGA design flow is usually GUI based tool. In this work, the development tool used for the

design and implementation is the ISE Xilinx 13.1 tool, which is used for all steps involved in the design flow. It includes synthesis, Place&Route, bitstream generation and FPGA configuration and test.

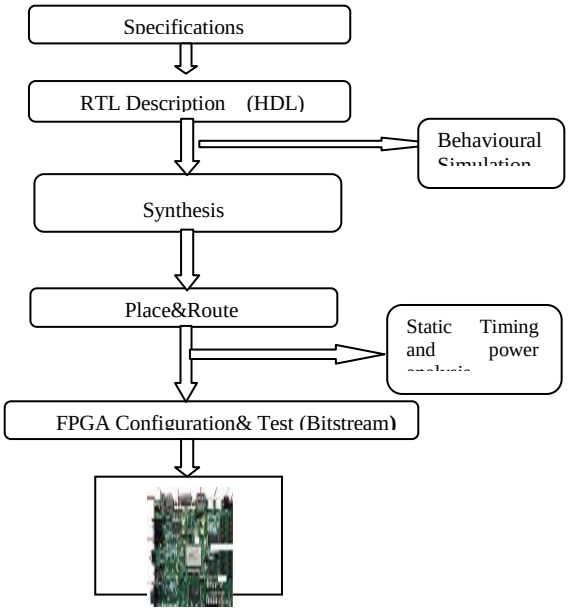

Figure 3. FPGA design flow

5.2 FPGA synthesis results

The design has been implemented on FPGA Virtex5 (LX50) platform and the synthesis is performed using XST (Xilinx Synthesis Tool). The operating frequency is 66 MHz. Results show that the architecture uses 50% of BRAM memories, 27 % of slice registers and 48% of slice LUTs. It is noticeable that the BRAM memories are the most used resources, the use of the other resources remain low. The power consumption is about 4.23W. Table 1 tabulates the FPGA resources allocated to SoC components.

Table 1. FPGA resources allocated to SoC components.

Components	# of LUT	# of Slice Register	# of BRAM	# of Occupied Slice
OR1200	24%	8%	45%	35 %
Ethernet	6%	3%	2%	10 %
UART	1%	0%	0%	2%
AC97	2%	2%	0%	5%
Debug Unit	3%	2%	0%	6%

6. ASIC IMPLEMENTATION

6.1. ASIC design flow and tools

The ASIC design flow defers moderately from the FPGA design flow. The main difference is in the verification setups. Figure 4 presents the ASIC design flow; it involves more verification

compared to the FPGA design flow. A detailed presentation of the steps involved in both FPGA and ASIC design flows is given in [18].

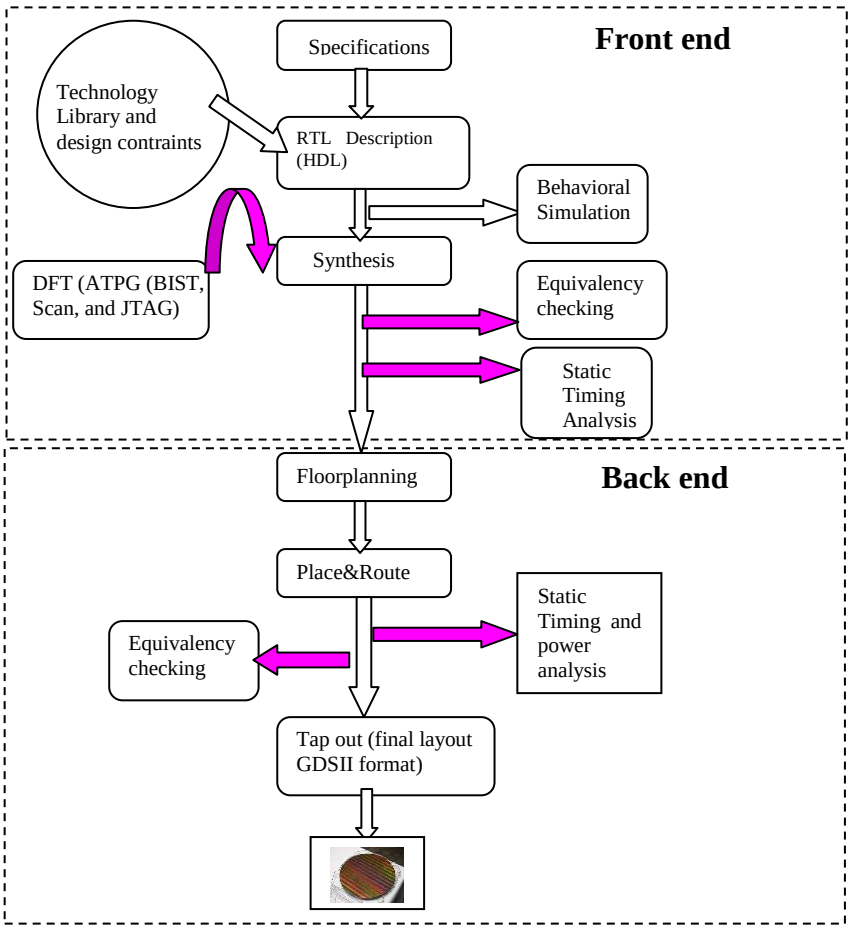

Figure 4. ASIC design flow

6.2. ASIC synthesis results

The synthesis for ASIC implementation was performed using Cadence RTL Compiler v10.10-s209_1 [19], with 0.18µm TSMC process technology. This step is completed using a compile script. Compilation was based on the top-down approach, where all modules are compiled starting from the top level of the design hierarchy. Few RTL changes are required when targeting an ASIC implementation. The changes are mainly done in *defines.v* files and Verilog files that include memories instances. We have set the configuration for an ASIC target and instantiate the targeted ASIC memories. Note that there are several supported ASIC RAMs memories namely, Artisan Single-Port Sync RAM, Artisan dual-Port Sync RAM, Avant Two-Port Sync RAM, Virage Single-Port Sync RAM and Virtual Silicon Single-Port Sync RAM.

In our case we have chosen the Artisan Single-Port Sync RAM and Artisan dual-Port Sync RAM memories. We have first used the random logic approach using flip flop for instances including memories, synthesis results using this approach were reported in our previous work [20]. In this work, a RAM compiler approach which is area-efficient has been used to improve the results. The appropriates memories was generated by the 'IMEC ASIC and design service team' (www2.imec.be) using the memory compiler tool (SRAM-DP-HS SRAM Generator)) from Artisan Components, INC with TSMC 0.18 µm technology process.

6.2.1. Area estimation

The area utilization of the OpenRISC based SoC is about 2.65 mm² and the OpenRISC processor occupied the area of 2.34 mm². As expected the use of dedicated memories enables significant reduction, in area and power consumption. Figure 5 presents the ASIC synthesis results of the designed SoC in term of area utilization.

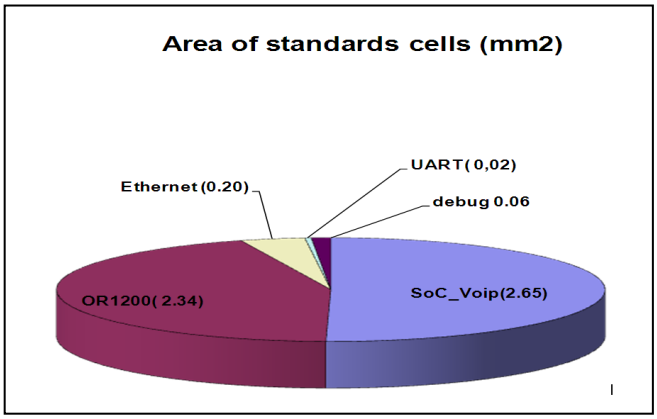

Figure 5. Area of standards cells (mm²)

6.2.2. ASIC power estimation

Herein we give the RTL power estimation, the histogram in Figure 6 shows the ASIC power consumption of some IPs included in the designed SoC. The total power consumption is about 113.75 mW with 113.67 mW for dynamic power consumption and 0.072 mW for the static power. Table 2 summarizes the instances power usage percentages. It is noticeable that the OpenRISC is the most power consuming.

Table 2. ASIC synthesis results regarding instances power usage percentages

Instances	Instance Power Usage
Or1200_top	23 %
Or1200_top_cpu	17.5%
Ethmac	13.65%
UART 16550	2.44%

The histogram in Figure 7 represents the power for ASIC and FPGA. The FPGA power estimation is done using the XPower Analyzer by Xilinx [21]; the total power consumption is about 5160 mW. We recognize that the estimates may not be extremely accurate since measuring the gap between the two media needs a specific measurement approach that gives accurate measurement. Nevertheless the RTL power estimation results give a preliminary inference about the power consumption gap between the two media. It is noteworthy to precise that the ASIC power consumption is considerably less than the FPGA power consumption

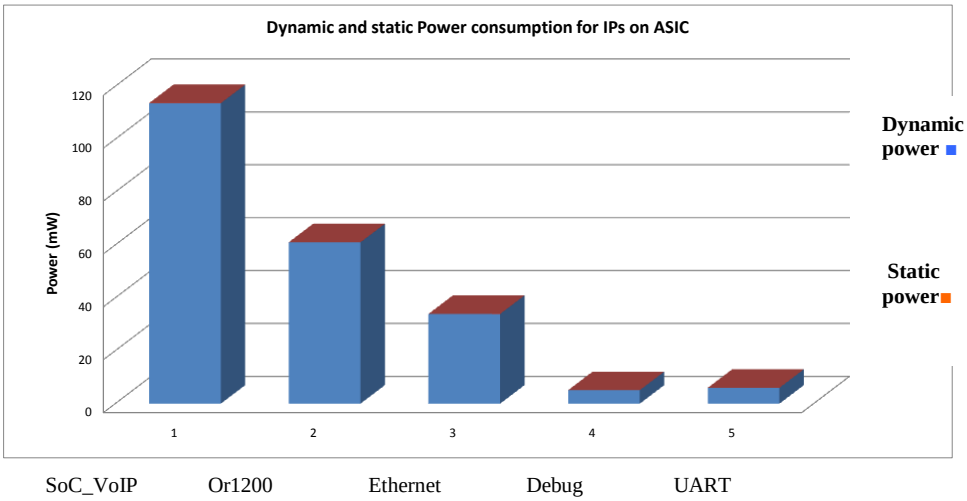

Figure 6. Histogram of power consumption for IPs on ASIC

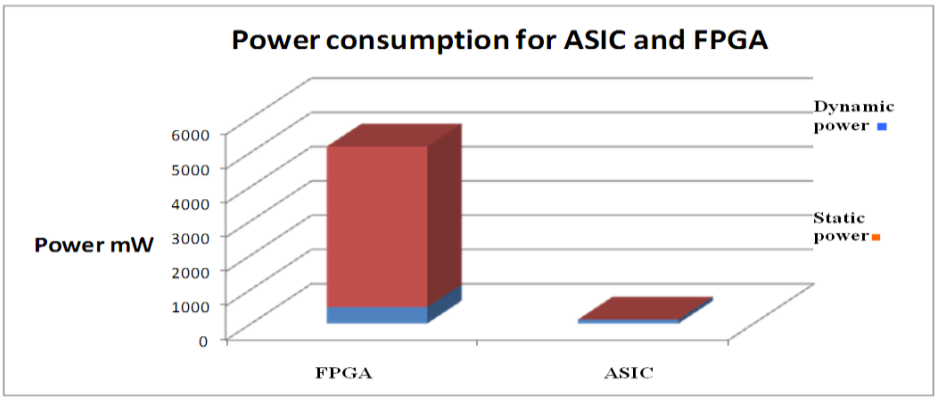

Figure 7. Histogram of power for ASIC and FPGA

7. CONCLUSIONS

We presented in this work an ASIC design of a SoC for VoIP application. The SoC architecture is based on the technology-independent building blocks described at RTL level. A hybrid approach has been applied, where the FPGA platform is used for the functional validation of the design, which is then implemented as an ASIC.

We exposed mainly synthesis results, primary regarding the area issue; that is an important issue for ASIC design cost, and we have given an estimation of the RTL power consumption. In term of area utilization, results show that the SoC occupied the area of 2.67 mm² in which the OpenRISC processor occupied the area of 2.34 mm². Regarding the power consumption, the total power consumption in ASIC is about 113.75 mW whereas in FPGA implementation the power consumption is about 5160 mW. As expected the ASIC power consumption is considerably less than the FPGA power consumption. We consider that, FPGAs are a good solution for functional validation and prototyping of the design that will be implemented in ASIC technology. But they cannot replace ASIC mainly for design requiring low power consumption.

REFERENCES

[1] Colin, Baldwin "Converting FPGA Designs", Open-Silicon.
[2] Mjan Lampret (2001) "Openrisc 1200 IP Core Specification", Rev. 0.7.
[3] Faroudja, Abid; Nouma, Izeboudjen; Mohamed, Bakiri,; Sabrina, Titri; Fatiha, Louiz & Dalila Lazib (17-20 December 2012) "Embedded Implemetnation Of An IP-PBX /Voip Gateway ", ICM , International Conference On Microelectronics, , , Algiers, Algeria
[4] Nouma, Izeboudjen; Dalila, Lazib; Mohammed, Bakiri; Faroudja, Abid; Sabrina, Titri & Fatiha, Louiz (Nov 2013), "A New Design Reuse Approach For Voip Implementation Into Fpsocs And Asics", International Journal On Soft Computing (Ijsc) Vol.4, No.4, , P. 21-31, Doi: 10.5121/Ijsc.4402.
[5] Free Telephony Project, Open Telephony Hardware, IP04 Four Port IPPBX Retrieved February 14, 2010.
[6] Dan ,Amarandei & Mostafa, El-Said (2010), "Implementation Of Wideband Voip Middleware Using Embedded Systems", Electro/Information Technology (EIT) IEEE.
[7] Http://Www.Digital-Opsis.Com
[8] Faroudja, Abid; Fatiha, Louiz; Mohamed, Bakiri; Sabrina, Titri; Nouma, Izeboudjen & Dalila Lazib (26-27 Aug 2013), "Embedded SIP Server Based FPGA-Socs Approach", Ewili'13, 3rd Embedded Operating System Workshop, Toulouse, France.
[9] James, Tandon (2010), "Openrisc Based Control Processor For Measuring Power Supply Noise, Temperature, And I/O Pad Voltages Over A JTAG Like Test Access Network", University Of Tokyo, Japan.
[10] Anoop C, Nair Indian Institute Of Technology, Delhi Hauz Khas.
[11] Paul, Morgan (2008), "Energy Analysis And Optimisation Techniques For Automatically Synthesised Coprocessors", Master Thesis, The Universities Of Edinburgh.
[12] James, Tandon (2009), "Openrisc Based Multicore, Multiprocessor Architecture".
[13] Andreas, Ehliar (2009), "Performance Driven FPGA Design With An ASIC Perspective", Ph.D Dissertation, Linkoping University,
[14] K.-C, Wu & Y.-W, Tsai (2004), "Structured Asic, Evolution Or Revolution?"? ISPD '04, 4th International Symposium On Physical Design. New York, NY, USA: ACM, Pp. 103–106.
[15] Http://En.Wikipedia.Org/Wiki/Structured_ASIC_Platform
[16] Tsung-Han, Heish & Rung-Bin (25-26 Feb 2013), Lin, "Via-Configurable Structured ASIC Implementation Of Openrisc 1200 Based Soc Platform", IEEE 2nd International Symposium On Next-Generation Electronics (ISNE), Kaohsiung , Taiwan.
[17] Paul, Dewell (2004), "Openrisc Implementation In A Viamask Structured ASIC".
[18] Http://Www.Xilinx.Com/Fpga/Asic.Htm
[19] Cadence Design Systems, GUI User Guide For Encounter RTL Compiler, Product Version 10.1,December 2010. Www.Cadence.Com
[20] Faroudja, Abid & Nouma, Izeboudjen (April 2015) , "ASIC Implementation Of An Openrisc Based Soc For Voip Application", 6th International Conference On Information And Communication Systems (ICICS), Pp.64-67, Amman; Jordan. Doi:10.1109/IACS.2015.7103203.
[21] Xpower Estimator User Guide, UG440, January 18, 2012.

Authors

Faroudja ABID received her engineering degree in Electronics Engineering from the University of Tizi ouzou, Algeria; and the M.S. from Ecole Nationale Polytechnique (ENP) of Algiers, Algeria. Currently, researcher at the CDTA center. Her research interests include embedded system, FPGA design, ASIC design, Real-time and System on Chip Design.

Nouma Izeboudjen received her engineering degree in Electronics Engineering from the University of sciences and technology Houari Boumedienne, Algeria. And the P.H.D degree from Ecole Nationale Polytechnique (ENP) of Algiers. Currently, researcher at the CDTA center. Her research interests include embedded system, FPGA and ASIC design, System on Chip Design and neural network.