A 130-NM CMOS 400 MHZ 8-BIT LOW POWER BINARY WEIGHTED CURRENT STEERING DAC

Ashok Kumar Adepu and Kiran Kumar Kolupuri

Department of Electronics and communication Engineering,MVGR College of Engineering, Chintalavalasa, Vizianagaram.

ABSTRACT

A low power low voltage 8-bit Digital to Analog Converter consisting of different current sources in binary weighted array architecture is designed. The weights of current sources are depending on the binary weights of the bits. This current steering DAC is suitable for high speed applications. The proposed DAC in this paper has DNL, INL of ±0.04, ±0.05 respectively and the power consumption of 16.67mw.

This binary array architecture is implemented in CMOS 0.13µm 1P2M technology has good performances in DNL, INL and area compared with other researches.

KEYWORDS

Current Steering, Binary Weighted, Current Source, INL(Integral Non Linearity), DNL (Differential Non Linearity), Power.

1. INTRODUCTION

Real world signals are in analog form but digital signals are processed easily with simple circuits so analog signals are converted into digital form. The digital signals are converted back to analog form to do some real world functions. The circuit that performs this conversion are digital-to-analog converters, and at the output of this DACs load is connected. In this paper binary weighted CMOS current steering DAC is designed with current sources and resistor at the output stage. Each current source has weight with respect to the position of the current source.

Basically there are three types of current steering architectures unary array, binary array, and segmented array architecture. Unary current DACs use a single-current element for each quantization step. Unary current DACs are analogous to resistor divider DACs with a resistor element for each LSB. The drawback of unary arrays is that the complexity of the digital decoder is exponentially related to the resolution.

Binary current DACs group current elements into binary multiples that are turned on or off directly with the input bits. This eliminates the decoder required in unary current DACs. Segmented arrays consist of different sub-arrays, or segments, each with a potentially different array coding. The MSB-segment is a unary array with 2^M-1 element and represents the upper M bits. The LSB-segment realizes the lower L bits in a binary array.

DOI: 10.5121/ijci.2016.5434

The current source used here has no capacitance so the circuit need not to be charge or discharge in ON state. For high speed and high resolution designs current steering Digital to Analog Converters are more suitable. As frequencies and conversion rates increases, frequency domain parameters like SNR, SFDR parameters become more useful than static parameters like INL and DNL.

2.CIRCUIT AND LAYOUT

2.1.Current Source

The current source used here is driven by the binary input. To act as a current source the gate voltage must be constant. The current source performance is improved by improving two parameters i) small signal output resistance by increasing resistance a more constant current over a large range of Vout values. ii) Reduce the V_{min} voltage by allowing a large range of V_{out} over which current source work properly. To reduce V_{min} by increasing value of W/L and adjusting the gate to source voltage to get the same output current.

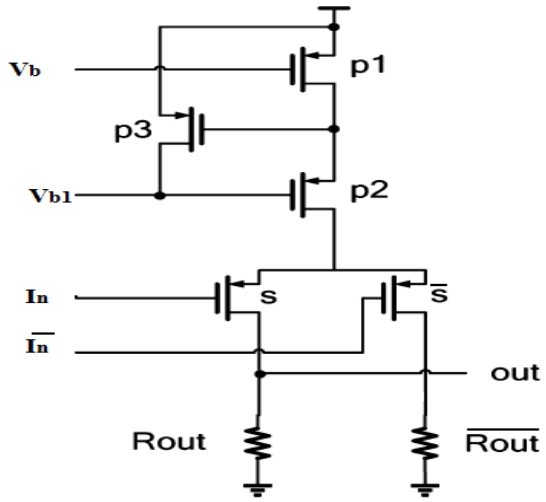

Figure1:Schematic diagram of current source

In the Figure 1: P_1 controls the value of current by varying width of P_1. The goal of MOSFETs *S* and $\overline{S}$ they act like switches. The gate terminal of *S* is connected to binary input. MOS *S* turns on the switch and $\overline{S}$ turns off the switch for a given input. The current sources that are turned on generate current flows through the output resistor R_{out} to generate an analog output from the DAC. MOSFET P_3 is used to increase the output impedance. The high output impedance can improve the performance of INL and SFDR. The 8-bit DAC requires 8 current sources and all the currents from each current sources are added at the output stage. The layout of the current source is shown in Figure 2.

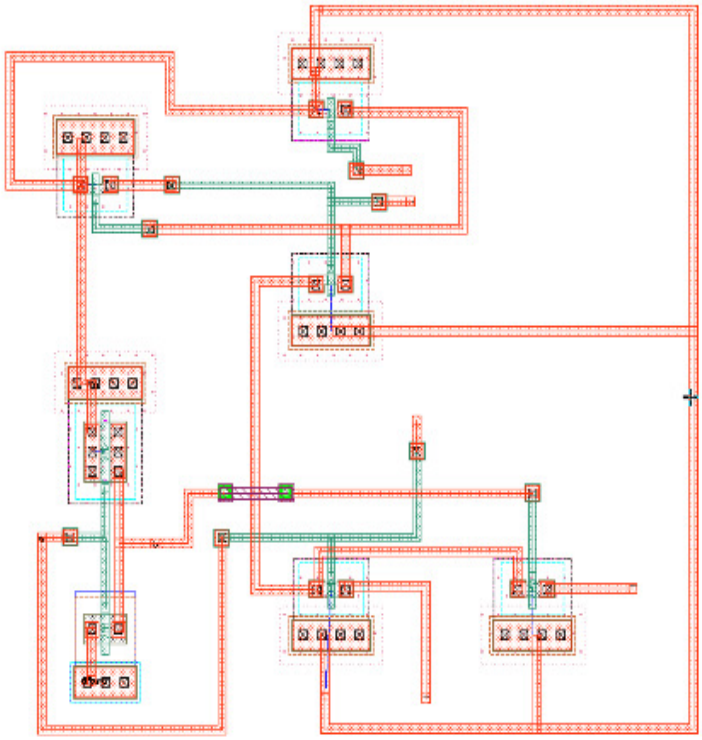

Figure 2: Layout of the current source.

2.2.Binary Weighted Dac

Now a day's the interface between the digital systems and analog systems are Digital to Analog Converters. The current steering DAC architectures are intrinsically fast, cost effective, and have high power efficiency [5][6]. The current-steering DAC replaces the resistor element in the resistor DAC architectures with a MOSFET current element and uses some form of summation of the current elements to produce the result. Binary weighted DACs group current elements into binary multiples that are turned on or off directly with the input bits. Figure 3: shows the general block diagram of binary weighted DAC. This eliminates the decoder required in unary current DACs. Unary and binary current DACs are often used together. Mostly, unary DACs are used for the MSB current elements because of their inherent monotonicity. Binary DACs are used for the LSB elements because of their much smaller size when created with weighted transistors.

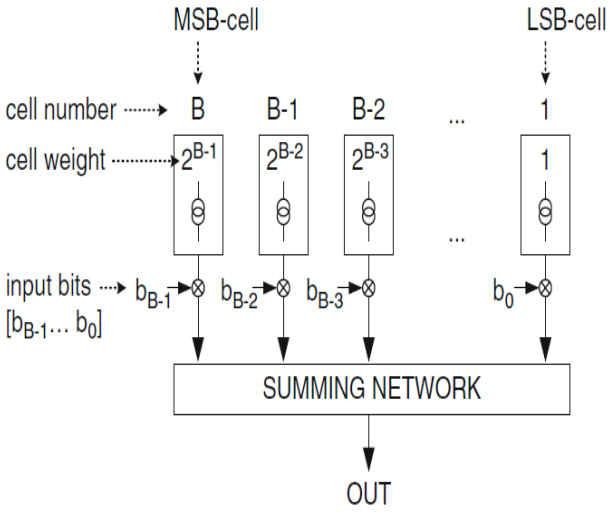

Figure 3:Binary weighted DAC architecture

Figure 4: Shows the schematic diagram of current source circuit designed by using PMOS transistors. A 50Ω resistor R_{out} is connected at the output. The relation between the output resistance and the achievable INL specification is given by:

$$INL= I*R^2_{out}*N^2/(4*R_{imp})$$

Where R_{out} is the load resistor, I is the LSB current,N is the total number of unit current sources [7].

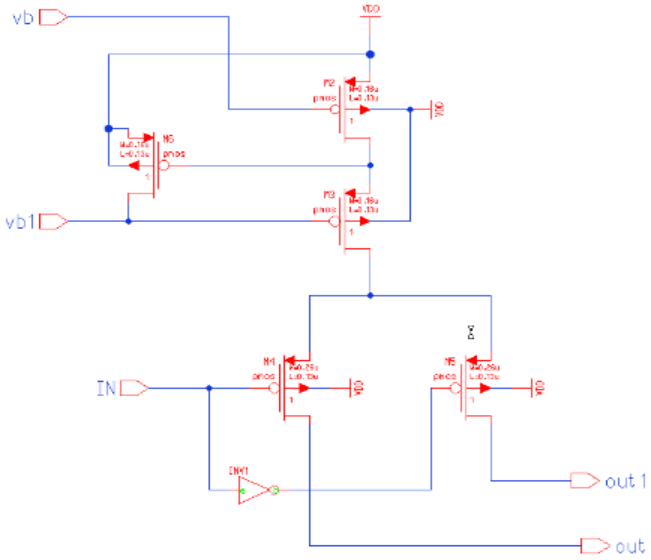

Figure 4:Schematic of Current Source

Figure 5: Shows the schematic of 8-bit DAC. This DAC using 8 current sources each current source has its own weights according to the position where it is used.

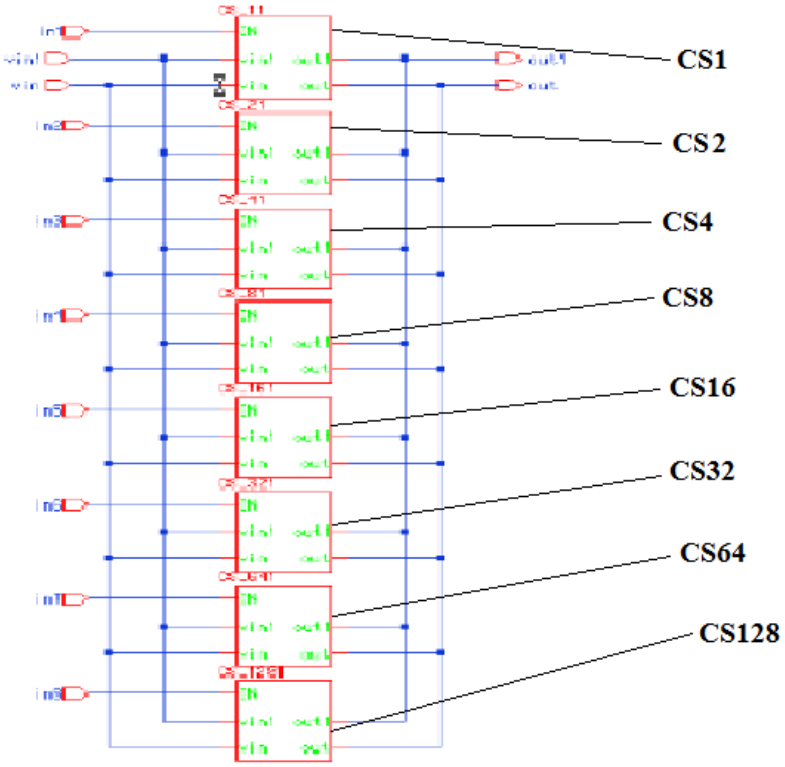

Figure 5:Schematic of 8-bit DAC

3. EXPERIMENTAL RESULTS

Figure 6: Shows the 8-bit DAC, which consists of current source modules of different weights. The digital input bits In_1 and In_2 drives the first two current sources of having weights 1 and 2 gives a current of I_1 and I_2 respectively. The current sources driven by inputs In_3,In_4,In_5,In_6,In_7,In_8 are having weights 4,8, 16, 32, 64 and 128 times of the current sources driven by In_1 respectively. The output analog values corresponding to digital inputs 00000000, 00100000, 01000000, 10000000, 11111111 are shown in Figure 7. The proposed 8-bit DAC was implemented using Mentor Graphics CMOS 0.13nm 1P2M technology with supply voltage 3.3V at sample rate 400MHz.

Differential nonlinearity is the difference of the output level between two adjacent codes. Integral nonlinearity is the measure of the actual output voltage level minus the ideal level. The values of DNL and INL after simulation are ± 0.04 and ± 0.05. The loading effect may degrade the performance.

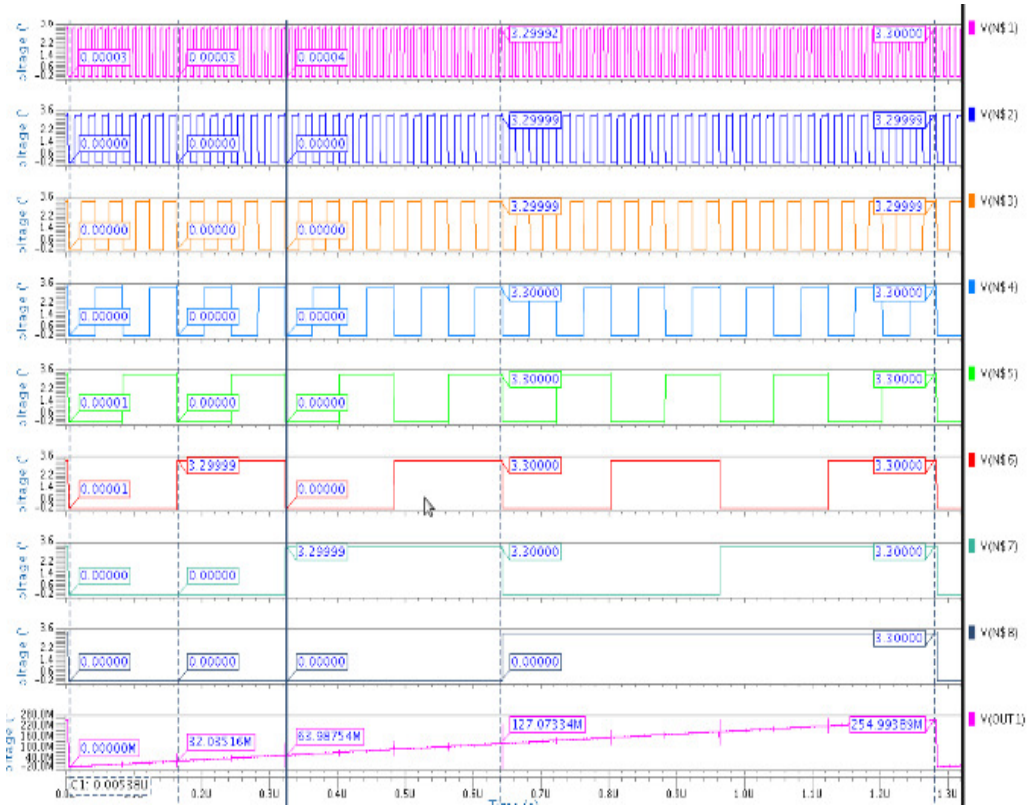

Figure 6: Simulation results of 8-bit DAC

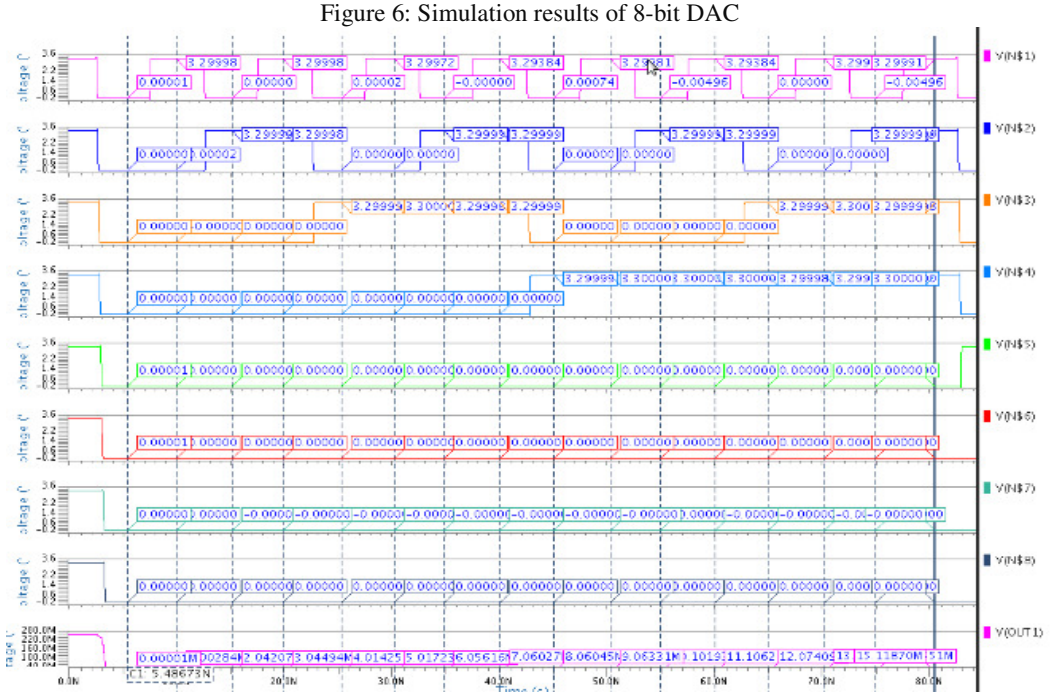

Figure 7:Results of first 15-binary values

The result of the 8-bit binary weighted DAC are shown in the Figure 6. This DAC eliminates the decoder circuit and the output of M-bit DAC is 0 to 2^M-1 i.e 0 to 255. The DAC is producing an output of 0mv, 4.014mv, 8.060mv and 15.03mv respectively for digital inputs of 0(00000000), 4(00000100), 8(00001000) and 15(00001111). The power dissipation of the DAC is 16.66mw.

Ref. [1] is a 10-bit current steering segmented DAC. Compared to this work the DNL of the circuit is less and here we are not using any decoder so the circuit complexity, the area occupied is less and transistor count is also very less.

Table 1:Summary of Experimental Results.

Parameters	[1]	[2]	[3]	[4]	This Work
Resolution	10	8	10	10	8
Sample rate(MHz)	200	100	210	80	400
DNL	±0.06	+0.31/–0.09	0.7	0.55	< 0.04
INL	±0.04	+0.26/–0.17	1.1	0.4	±0.05
Supply Voltage (v)	3.3	3.3	3.3	2.5	3.3/3
Power (mw)	7.9	27.5	83	27.65	16.67/7.211
Technology (nm)	350	130	350	250	130

4. CONCLUSION

In this paper, a 8-bit current steering binary weighted DAC was implemented. The technology used here is CMOS 0.13µm 1P2M process. The circuit is operated at two supply voltages 3.3v and 3v at the sample rate of 400 MHz. It achieved a DNL and INL of ±0.04 LSB and ±0.05 LSB, respectively.

The power consumption was about 16.67 mw at the sample rate of 400MHz. While the power supply is 3v respective power consumption is 7.211mw. This work presented a good performance when compared with researches in area, DNL, INL and power consumption.

ACKNOWLEDGEMENTS

We the authors would like to take this opportunity to extend our thanks to Department of ECE, MVGR College of Engineering, Vizianagaram for providing required tools to do research in VLSI Domain.

REFERENCES

[1] Yi S-C. A 10-bit CMOS current-steering digital to analog converter. AEU – Int J Electron Commun 2012;66:433–7.
[2] Yi S-C. An 8-bit current-steering digital to analog converter. AEU – Int J Electron Commun 2012;66:433–7.
[3] Cho H-H, Park C-Y, Yune G-S, Yoon K-S. A 10-bit 210 MHz CMOS D/A converter for WLAN. In: IEEE Asia-Pacific conference on advanced system integrated circuits. August 2004. p. 106–9.
[4] Halder S, Banerjee S, Ghosh A, Prasad R, Chatterjee A, Dey SK. A 10-bit 80-MSPS 2.5-V 27.65-mW 0.185-mm2 segmented current steering CMOS DAC'. In: 18th international conference on VLSI design. January 2005. p. 319–22.
[5] Hnp:llwww.cc.nctu.edu.twi-jtwui.
[6] B. Razavi, Principles of Data Conversion System Design. New York IEEE Press, 1995.
[7] Huei-Chi Wang, Hong-Sing Kao, and Tai-Cheng Lee. An %bit 2-V 2-mW 0.25-mm2 CMOS DAC in 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits(AP-ASIC2004).

Authors

A.ASHOK KUMAR pursuing Ph.D in JNTU Kakinada. He is working as Assistant Professor in department of Electronics and Communication Engineering, MVGR college of engineering, Vizianagaram, A.P, India. He has 9 years of teaching experience in reputed engineering colleges and 3 years of industry experience. His research interests include VLSI data converters and Embedded Systems. He is member in various professional societies such as ISTE, IAENG, IACSIT and IEI.

KIRAN KUMAR KOLUPURI received B.E degree in Electronics and Communication Engineering from SVP Engineering College in 2013. Pursing M.Tech in MVGR College of Engineering. Doing project on Digital to Analog Converters during Post Graduation Course.