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July 29~30, 2016, Vizianagaram, India

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Preface

The International Conference on Electronics and Communication Engineering (ICECE- 2016) was held in Vijayanagaram, A.P, India, during July 29~30, 2016. The conference attracted many local and international delegates, presenting a balanced mixture of intellect from the East and from the West.

The goal of this conference is to bring together researchers and practitioners from academia and industry to focus on understanding communications, signal processing and VLSI , Embedded Systems, Cloud Computing, IoT and to establish new collaborations in these areas. Authors are invited to contribute to the conference by submitting articles that illustrate research results, projects, survey work and industrial experiences describing significant advances in all areas of computer science and information technology.

The ICECE-2016 Committees rigorously invited submissions for many months from researchers, scientists, engineers, students and practitioners related to the relevant themes and tracks of the workshop. This effort guaranteed submissions from an unparalleled number of internationally recognized top-level researchers. All the submissions underwent a strenuous peer review process which comprised expert reviewers. These reviewers were selected from a talented pool of Technical Committee members and external reviewers on the basis of their expertise. The papers were then reviewed based on their contributions, technical content, originality and clarity. The entire process, which includes the submission, review and acceptance processes, was done electronically. All these efforts undertaken by the Organizing and Technical Committees led to an exciting, rich and a high quality technical conference program, which featured high-impact presentations for all attendees to enjoy, appreciate and expand their expertise in the latest developments in Electronics and communications research.

In closing, ICECE-2016 brought together researchers, scientists, engineers, students and practitioners to exchange and share their experiences, new ideas and research results in all aspects of the main workshop themes and tracks, and to discuss the practical challenges encountered and the solutions adopted. The book is organized as a collection of papers from the ICECE-2016.

We would like to thank the General and Program Chairs, organization staff, the members of the Technical Program Committees and external reviewers for their excellent and tireless work. We sincerely wish that all attendees benefited scientifically from the conference and wish them every success in their research. It is the humble wish of the conference organizers that the professional dialogue among the researchers, scientists, engineers, students and educators continues beyond the event and that the friendships and collaborations forged will linger and prosper for many years to come.

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DESIGN OF TRIPLE-BAND CPW FED CIRCULAR FRACTAL ANTENNA

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ABSTRACT

A novel miniaturized circular fractal antenna is designed by inscribing circular slot on rectangular ground plane and successively forming circular rings connected by semi-circles for circular-fractal patch. Novel modified Coplanar Waveguide (CPW) is used as feed for fractal circular patch. The analysis of parametric variations is performed by consecutive fractal iterations, varying the radius of inscribed circle of ground plane, slots and different ground plane configurations. To further enhance gain and radiation pattern a dual inverted L slots is included in ground plane. From the results it is evident that, the proposed fractal antenna possesses triple bands at 1.8GHz, 3.5GHz and 5.5GHz. These bands are used in Digital Communication Systems (DCS) (1.8GHz), IEEE 802.16d fixed WiMAX (3.5GHz) and IEEE 802.11a WLAN (5.5GHz) applications.

KEYWORDS

Fractal Geometry, Circular fractal Antenna, WLAN/WiMAX, Coplanar feed, Slotted ground plane

1. INTRODUCTION

The wireless standards of WLAN/WiMAX low frequency applications, require miniaturized and compact antennas. Low and medium fixed channel capacity point-to-point links uses the Digital Communication System (DCS) or GSM1800 frequency band. In order to gratify the IEEE WLAN standards in the 2.4 GHz and 5-6 GHz bands, a single antenna with multiple bands is needed. The proposed IEEE 802.11a 5.5GHz standard handles higher throughput and data rate at 1Gbps compared to 2.4GHz band where there is a huge traffic of data transmission. The IEEE 802.16d fixed 3.5/5.8 GHz WiMAX standard available for diverse broadband high speed data transmission [1]. The application of fractal geometry on antennas is one of the methods, which provides multi frequency operating band capability.

Fractals are quantitatively curved shapes, which are self-similar, repeating themselves at various scales [2]. Utilizing the fractal geometry in a patch antenna increases the length, or maximize the perimeter (inner or the outer structure), of patch that can collect or broadcast electromagnetic radiation within a total given surface area or volume [3]. The self-similarity and space-filling are the main properties, as the fractal geometries are mathematically linked to its frequency characteristics of the antenna [4]. The use of coplanar ground plane makes the new inscribed circular triangular fractal design conformal and more suitable for the ultra wideband and miniaturized applications [5]. Generally fractal designs are meant for their multi and wideband operation and also these designs are optimized for UWB characteristics [6].

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Different techniques have been introduced to get desired and unwanted sub bands in UWB domain. Most prominent examples are inserting a T-stub in the patch element or dual strips of parasitic in nature beside the feed or by inserting quarter wave and half wave split ring resonators or embedding H-slot in the patch. Another way is to embed the arc-shaped parasitic patch besides the radiating element or inserting various slots in the feed [7]. A novel way of applying fractal geometry approach to produce multi bands in an miniaturized fractal antenna due to space filling and self similar properties, which in turn enhances the valuable electrically effective length to minimize the area of the patch element [8-10].

In this paper, the design of a novel tri-band coplanar waveguide fed circular fractal antenna is proposed for modern era of wireless communication applications..

2. ANTENNA GEOMETRY

The proposed fractal antenna geometry with designated dimensions is shown in Figure 1. The proposed fractal antenna with substrate of FR4-epoxy (ε_r) =4.4 having dimensions 25 × 26 mm^2 (L × W) with height (h) = 1.6mm. The rectangular ground plane is inscribed with a circle of radius R_1=10.7mm and radiating patch is constructed with circular rings R2=8mm, R3=6mm and R4=4mm where each rings are 1mm wider and 1mm apart. All the rings are connected through a radius of 1.1mm semi circles. The ground plane is modified with W_5=5mm and a pair of inverted L slots of 2×2 mm^2 (L_2×W_2) with a W_6=0.5mm is inserted. The coplanar ground plane is having a strip of W_3=1.9mm. The gap between patch feed and ground plane is W_4=1mm.

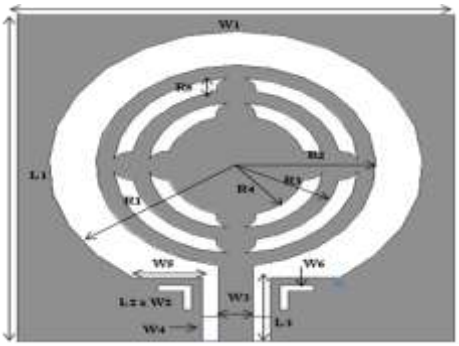


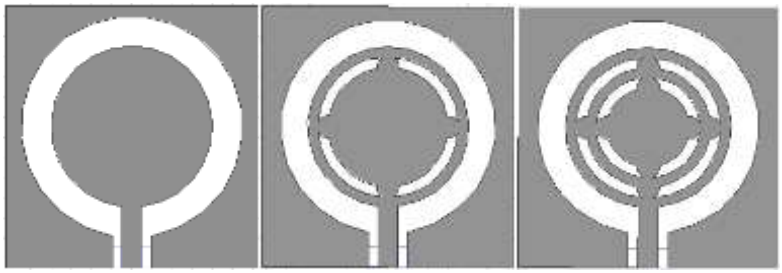
Figure 1: The proposed circular fractal antenna

3. PARAMETRIC ANALYSIS

The fractal antenna is designed and simulated using ANSYS HFSS 14.0 software package. The performance of the proposed circular fractal antenna is estimated using parametric studies of different fractal iterations, radius R1 of ground plane, various ground plane structures and different feed gap values of W_4 and W_5 are presented below.

3.1. EFFECT OF FRACTAL ITERATIONS

The self similar fractal iterations are performed as shown in Figure 2 (a)-(c) and their results are observed with respect to S11, VSWR, Gain and Radiation Pattern.



(a) Iteration 1 (b) Iteration 2 (c) Iteration 3

Figure 2: Successive Fractal Iterations

The corresponding results of fractal iterations of antenna are plotted in Figure 3-4 and tabulated in Table 1. Among all, the third iteration is having better return loss, gain of 3.75dB VSWR lesser than 1.5 and an offered bandwidth of 800MHz at 3.5GHz and 750MHz at 5.5GHz.

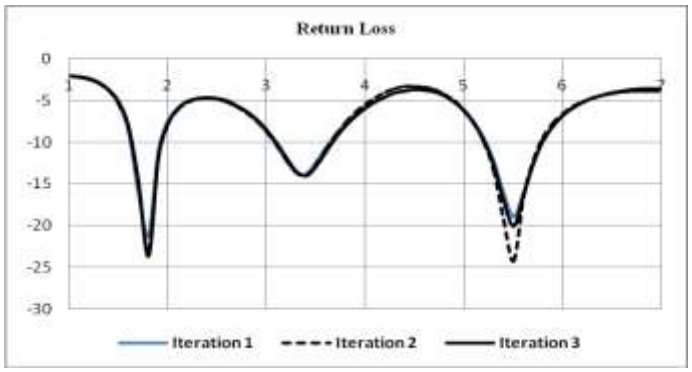


Figure 3: S11 versus frequency for all fractal iterations

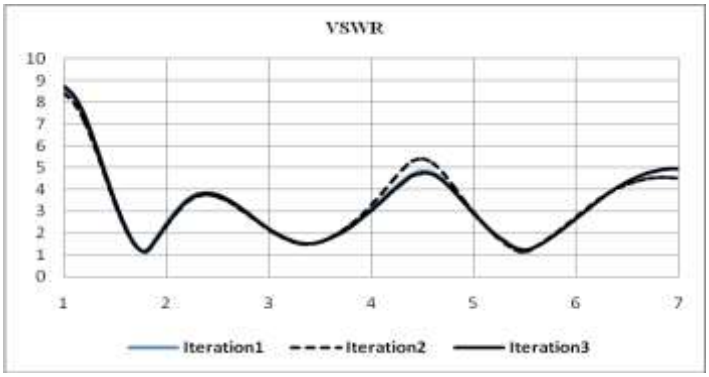


Figure 4: VSWR for all the fractal iterations

Table 1: Results of circular fractal iterations

Sl.No	**Resonant Frequencies (GHz)**	**Return Loss (dB)**	**VSWR**	**Bandwidth (MHz)**	**Gain (dB)**
Iteration 1	1.8	-23.2	1.05		3.65
	3.4	-14.5	1.5	550	

Sl.No	Resonant Frequencies (GHz)	Return Loss (dB)	VSWR	Bandwidth (MHz)	Gain (dB)
	5.5	-19.2	1.1	600	
Iteration 2	1.78	-23.5	1.1		3.72
	3.4	-14	1.5	550	
	5.5	-24.2	1.1	600	
Iteration 3	1.8	-32.5	1		3.75
	3.5	-17	1.25	800	
	5.5	-29.2	1.05	750	

3.2. EFFECT OF RADIUS R_1 OF GROUND PLANE

The inscribed circle of radius R_1 of ground plane is varied by keeping other patch elements constant and their results are shown in Figure 5. The proposed dimension for inscribed circle of ground plane R_1=10.7mm.

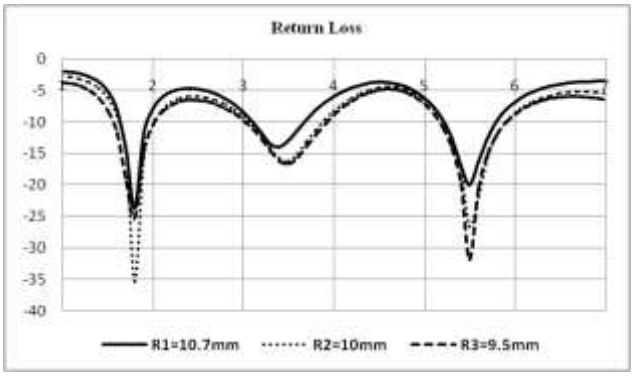
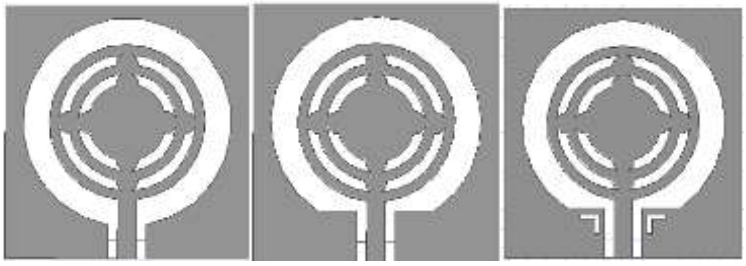


Figure 5: S11 versus frequency for different values of R_1

3.3. EFFECT OF DIFFERENT GROUND PLANE VARIATIONS

Three different configurations of ground planes are presented in Figure 6. Among all Ground plane 3 with L slots is proposed and the corresponding return losses of -25dB at 1.8GHz, -15.6dB at 3.5GHz and -47dB at 5.5GHz are shown in Figure 7.



(a) Ground plane 1 (b) Ground plane 2 (c) Ground plane 3

Figure 6: Three different configurations of ground planes

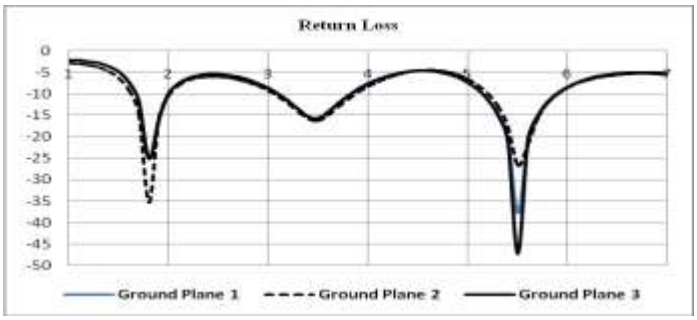


Figure 7: Return loss observations for different ground planes

3.4. EFFECT OF W_3, W_4, W_5

The effect of feed line width W_3, gap between ground and feed of the patch (W_4), and W_5 is observed for different values by keeping W_1, W_2 and W_6 constant. From Figure 8 it is evident that, for the proposed W_4=1mm and W_5=4mm the antenna resonates at 1.8GHz (GSM1800), 3.5GHz (IEEE 802.16d fixed WiMAX) and 5.5GHz (IEEE 802.11a WLAN). For W_4=0.85mm when W_3=2.2mm the possesses 1.9GHz, 3.5GHz and 5.6GHz.

For W_4=0.5mm and W_5=5mm, the antenna resonates at 2GHz (Advanced Wireless Services i.e. Mobile Satellite services), 3.7GHz and 5.8GHz (IEEE 802.16d WiMAX). For W_4= 0.5mm without L slot, the antenna resonates at 1.9GHz (DECT-Digital Enhanced Cordless Telecommunications), 3.7GHz (IEEE 802.11y extended version of 802.11a), 5.725GHz (ISM band). The above triple band proposals are quite good and they can cover multiple wireless applications. From Figure 9 it is observed that, all the proposals are having VSWR<=1.5 as per industry standard.

Figure 8: S11 versus Frequency observations for different gaps (W_4)

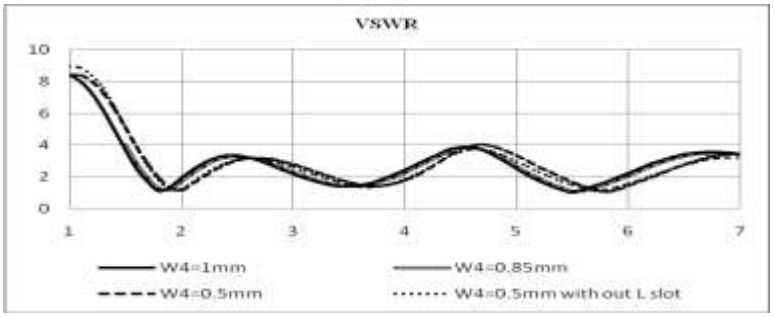
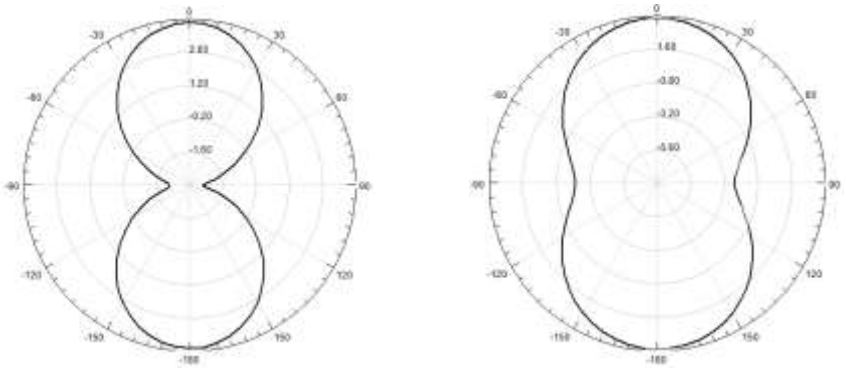


Figure 9: VSWR observations for different gaps (W_4)

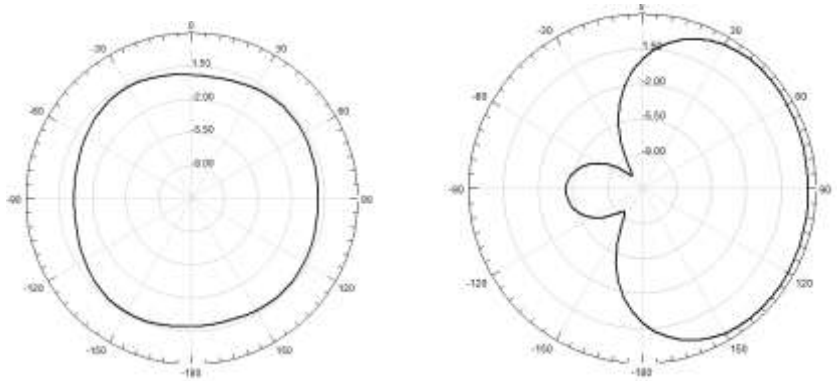
3.5. RADIATION CHARACTERISTICS

The far field radiation patterns of the proposed circular fractal at the resonant frequencies (3.5GHz and 5.5GHz) are shown in Figure 10-11. The E and H-Plane patterns of the antenna at resonant frequencies are shown below.



(a) (b)

Figure 10: Radiation patterns at 3.5GHz (a) E-Plane (b) H-Plane



(a) (b)

Figure 11: Radiation patterns at 5.5 GHz (a) E-Plane (b) H-Plane

Figure 10 shows that the E-plane pattern exhibits dual band and H-plane provides almost wide band characteristics at 3.5GHz. Figure 11 shows that E-plane pattern possesses omni-directional and H-plane provides wideband characteristics. The antenna has a gain of 3.7dBi at 3.5GHz and 4.5dBi at 5.5 GHz solution frequencies.

4. CONCLUSIONS

In this paper, a novel miniature triple-band fractal antenna is designed by successive self similar circular rings are connected with semi circles and it is fed by CPW feed. The parametric studies of fractal antenna with respect to number of iterations, different inscribed circle radius R_1 in ground plane, various ground plane structures and different gap widths between ground and feed are performed and analyzed in this paper. The proposed circular fractal antenna has triple bands at

Digital Cel1ular System (GSM1800), WiMAX (IEEE 802.16d at 3.5GHz) and WLAN (IEEE 802.11a at 5.5GHz). From the results it is evident that the proposed antenna offers a bandwidth of 800MHz, a peak gain of 3.5-4.5dBi and the antenna has good radiation characteristics.

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PERFORMANCE ANALSIS OF CLIPPING TECHNIQUE FOR PAPR REDUCTION OF MB-OFDM UWB SIGNALS

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ABSTRACT

Multiband Orthogonal Frequency Division Multiplexing (MB-OFDM) is used as efficacious procedure for ultra-wideband (UWB) wireless communication applications, which divides the spectrum into various sub-bands, whose bandwidth is approximately 500MHz. Major arduousness in multiband-OFDM is ,it have very large peak to average power ratio value which causes the signal to enter into dynamic region that consequence in the loss of orthogonal properties and results in the interference of the carrier signals which crops the amplifier saturation and finally limits the capacity of the system. Many PAPR amortize algorithms have reported in the survey and pre-coding is PAPR reduction which is inserted after modulation in the OFDM system. The Existing work presents the reduction of that value by different clipping techniques namely Classical-Clipping (CC), Heavy side-Clipping (HC), Deep-Clipping (DC) and Smooth-Clipping (SC) and their comparison analysis is done. Every clipping method is best at its own level .The proficiency of these strategies are evaluated in locutions of average power disparity, complete system decadence and PAPR reduction. Finally results show the MB OFDM yields better performance to reduce PAPR in effective way.

KEYWORDS

OFDM, PAPR, HPA, Clipping techniques, MB OFDM

1. INTRODUCTION

In present scenario, high data rate wireless links got a great importance, due the development of digital imaging and multimedia applications. Ultra Wide Band is emergent technology which facilitate that requirement of providing high data rate of 110 Mbps at a distance of 10 m and 480 Mbps at a distance of 2m[9].

This technology has raised a great influence in the wireless networking links because of its productive account in providing high data throughput, low power out sending, accurate ranging/localization and multipath immunity. MB-OFDM is more beneficial than the 'impulse radio' and other multiplexing based transmission. In this multiband multicarrier system the transmission symbol follows the high frequency hopping at pre-defined time –frequency interference (TFI)[9] pattern over the multiple bands. Timing and frequency synchronization is a defenceless issue in any Orthogonal FDM based systems. System performance perversion is caused due to the inter symbol interference and inter carrier interference which occurs due to time synchronization error. In MB-OFDM [5] system, frequency synchronicity is possible as source oscillator frequency offset generates different frequency carriers at distinct bands which provide high data transmission. It supports low intricacy, fast converging.

MB-OFDM forms basis for all 4G wireless communication systems due to its huge capability in terms of number of subcarriers, high data rate in excess of 100 Mbps and ubiquitous coverage with high mobility.

The introduction chapter consists of following parts:

In an MB-OFDM, more autonomous modulated sub-carriers are existing. Due to their presence, there is high Peak to average power ratio value of the system where peak value is 'M' times the average value due to addition of the same phase signals

The significant cons of a high Peak-Average Power Ratio are-

1. Complicacy increment in Analog –Digital convertors
2. Decline in efficiency of RF amplifier.

In this paper, MD-OFDM signals are generated and the High PAPR value is reduced using the clipping techniques, namely classical clipping, heavy side clipping, smooth clipping, deep clipping. The PAPR values are compared between the techniques. The average power, total degradation and BERVs SNR CCDF graphs are plotted

The remnant part of this particular paper is constituted following: section 2 introduced the Multiband-OFDM system model. Sub-section 3 deals with the clipping technique implementation for the PAPR abasement of MB-OFDM signals. In next section the simulation outputs are highlighted followed by the conclusion in the section 5.

2. MULTIBAND ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (MB-OFDM) SYSTEM MODEL

In this subsection, the basic MULTIBAND OFDM system is overviewed. . The federal communication commission (FCC) has declared the band width from 3.1GHz to 10.6GHz (7.5GHz) for ultra wide systems having spectral density of -41.3dBm/MHz[5].UWB system based on OFDM is combination of modulation technique with a multi- banding approach processed for efficient utilisation of spectrum having each band of 500Mhz approximately [6]. There is switching of sub bands after operating in one for some time. In each sub-band, OFDM modulation is used to transmit data symbols. In order to exploit the spectral diversity, the transmitted symbols are time interleaved across the sub-bands.

Multicarrier Communication involves splitting of the spectrum to give a number of signals over that frequency range i.e spectrum 7.5GHz into 14 bands each of 528 MHz[9] [2].Each signal is modulated separately and transmitted over the channel and de-multiplexed at receiver side i.e demodulated and recombined to get the initial signal. This techniques implements OFDM scheme which is one of the multicarrier communication technique. Many advantages are posed by this procedure

- Transmitting power is same due to functioning over complete band-width
- Power consumption and cost are low due to processing of information in small bands
- Spectral pliability improvement

2.1. REPRESENTATION OF MULTIBAND-ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (MB-OFDM) SIGNAL:

The transmitted RF signal is associated to the base band signal as preceded

$$s_{RF}(t) = Real\{\sum_{i=0}^{M-1} \binom{n}{i} s_i(t - kT_{SYS}) e^{J2\pi f_i mod 6}\} \quad (1)$$

Where Real (.) delineate complex variable real value.s_i(t) is the base band signal representing the i[th] OFDM symbol occupying a symbol interval of length T_{SYS} and M in the number of OFDM symbol transmitted .the carrier frequency or band that the i[th] OFDM symbol is transmitted over is denoted as f_i range over 3 frequencies assigned to the band group that the system is operating in those frequencies are organised into sequence of length 6 ,called time-frequency code(TFC).Location of the i[th] symbol in the packet decides it's exact location All the OFDM symbol s_i(t) is obtained with a certain set of Coefficients C_n which are applied IFFT operation. the coefficients are defined as either data, pilot or training symbols.

$$s_i(\mathrm{t}) = \begin{cases} \sum_{-N_{ST/2}}^{N_{ST/2}} C_n e^{J2\pi n \Delta \mathrm{f(t)}} , & \mathbf{t} \in [\mathbf{0}, T_{FFT}] \\ \mathbf{0} , & \mathbf{t} \in [T_{FFT}, T_{FFT} + T_{Zp}] \end{cases} \quad (2)$$

where Δf represents carrier frequency and N_{ST} represents the subcarrier frequency spacing and number of total subcarrier users respectively[8].The final waveform have time period of $T_{FFT} = 1\Delta$f zero padding T_{zp} is done to provide guard interval between different sub-bands as well as to avoid the multipath effect.

3. PEAK TO AVERAGE RATIO REDUCTION OF MULTIBAND ORTHOGONAL FREQUENCY DIVISION MULTIPLEXING (MB-OFDM) SIGNALS USING CLIPPING TECHNIQUES

In this section, the description of PAPR [4] and PAPR reduction done by clipping technique is given. Clipping techniques mainly focused on classical clipping, deep clipping, heavy side clipping and smooth clipping.

3.1 PEAK TO AVERAGE POWER RATIO (PAPR)

High date rate communication is very adverse task in wireless communication. With the ever growing demand of wireless communication in this generation various modulation techniques are introduced. Multi band multi carrier frequency division multiplexing is one of prominent technology amongst. There are different techniques to diminish PAPR of OFDM. It can be divided into two types. They are signal scrambling techniques and signal distortion techniques.
The complex data block for the OFDM signal to be transmitted is given by

$$\mathrm{y(t)} = \frac{(1)}{\sqrt{\mathrm{M}}} \sum_{\mathrm{k=1}}^{\mathrm{M\text{-}1}} \mathrm{Y_k}\, e^{j2\pi \mathrm{fkt}} \quad (3)$$

Where M is number of sub-carriers Y_k is the k[th] component of symbol Y, f_k frequency of the k[th] subcarrier.

$$PAPR = \frac{peak\ instantanous\ \ power}{avearge\ power} = \frac{max|y(t)|^2}{E[|y(t)|^2]} \quad (4)$$

Where E [·] states the expected value [4].

3.2 CLIPPING TECHNIQUES

Among, the all the methods of PAPR reduction, clipping technique [4] is simplest .In this method, high peak values of the multicarrier signal are clipped before it passes through the power amplifier. This is done by clipper which restrict the signal envelop to the fore determined threshold level known as clipping level[10].this technique may cause distortion which emanate in-band and out-band disparity, which is solved using filter. The implementation of the clipping is demoed through the following diagram

Figure 1 explains the multicarrier MB-OFDM transmitter which consists of mainly clipping equipments and filter. Depending on the type of the clipping technique used for PAPR reduction, the behaviour of clipper varies, which is given by the function n.f(.)The filter consists of FFT and IFFT pair where FFT transmogrify $\hat{Y}_n$ to $\hat{Y}_k$ i.e from frequency to time domain. The in-band components of Y ˜ is passed without any change where as the out-of-band components are set to zero, which is given as

$$X_k = \begin{cases} Y_{k,} & \widetilde{k \in In} \\ 0, & k \in Out \end{cases} \quad (5)$$

Where as In is in-band , Out is out-of-band components of Y.Y_n is the MDOFDM symbol, $\hat{Y}_n$ is the clipping symbol , $X_{n\hat{}}$ is the clipped output and f_{car} is carrier frequency.

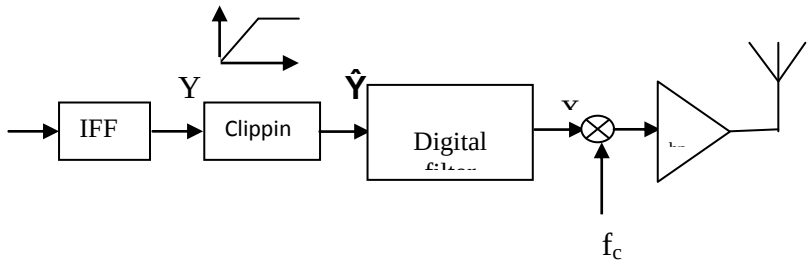

Figure 1: multicarrier (MB-OFDM) transmitter

VARIOUS CLIPPING TECHNIQUES IMPLEMENTED FOR PAPR REDUCTION

In this paper only four clipping techniques are highlighted: Classical clipping, Heavy side clipping, Deep Clipping and Smooth Clipping[4] whose the functions of clipping are depicted in figure 2. The discrete-time OFDM signal Y_n is rewritten into polar coordinates gives $Y_n = p_n e^{j\theta n}$, where p_n implied signal amplitude Y_n and Θ_n is phase .The clipped signal Y ˜n is expressed as

$$\hat{Y}_n = f(p_n)e^{j\omega n} \quad (6)$$

3.2.1 CLASSICAL CLIPPING (CC) TECHNIQUE

The most popular PAPR reduction technique proposed in the literature known as far is CLASSICAL CLIPPING (CC)[4]effects PSD and MB-OFDM performance This function is given as follows and depicted in fig2(a)

$$f(p) = \begin{cases} S & , p > S \\ p & , p \leq S \end{cases} \quad (7)$$

Where S is the threshold amplitude considered.

3.2.2 HEAVY SIDE CLIPPING (HC) TECHNIQUE

It is also called hard clipping. The communication system execution is improved by using Heavy side clipping as baseband non linear transformation technique[4] .this is give by the following function, depicted in fig2(b)

$$f(p) = S \quad \text{?} \; p \geq 0 \quad (8)$$

3.2.3 DEEP CLIPPING (DC) TECHNIQUE

Deep clipping (DC)[4] is proposed to solve the problem of peaks re-growth caused due to out-of band filtering. Here the function is altered to avoid high amplitude peaks. Depth factor is parameter that is nait to control the clipping depth. This technique is given as below and paraded infig2(c)

$$f(p) = \begin{cases} p & , \quad p \leq S \\ S - ß(p - S) & , \quad ß < r \leq \frac{1+ß}{ß} A \\ 0 & , \quad p > \frac{1+ß}{ß} A \end{cases} \quad (9)$$

Where ß is depth factor.

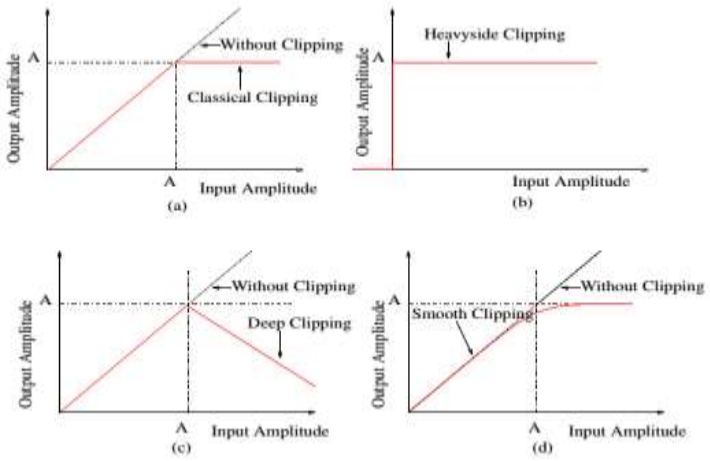

Figure 2.Different Clipping techniques

3.2.4 SMOOTH CLIPPING (SC) TECHNIQUE

MB-OFDM peak-average power is diminished using this method. The function is given as follows and the characteristic graph is shown in 2(d)

$$f(p) = \begin{cases} p - \frac{1}{r}p^3 & , \quad p \leq \frac{3}{2}S \\ S & , p > \frac{3}{2}S \end{cases} \quad , \text{where } r = \frac{27}{4}S^2 \quad (10)$$

4. EXECUTION RESULT

The system performances are calculated considering the factors like clipping ratio(CR)[4] and input back off(InBO).

$$ClippingRatio = 20\ log10\frac{S}{\sqrt{K}}[dB] \quad (11)$$

$$InBO = -10\log10\frac{(Exp|C_{in}.C_{in}.*|)}{K_{satar}}\text{dB} \quad (12)$$

Here K is knee factor which decides the smoothness, K_{satar} is signal saturated power.

4.1 OBSERVATION PARAMETERS

The peak-average power ratio is computed by taking the instantaneous power normalised with the expectation of square of average power .the peak power is calculated based on complementary cumulative distribution function [1]

$$CompCumDisFun(\text{ɵ}) = \text{Prob}\{Peak \geq \Theta\} \quad (13)$$

Which means probability of samples that surpass the instantaneous power (Ɵ)

The three parameters which are considered for the system execution in this paper are

- ΔPpapr which marks the peak to average power reduction performance[4]that is described as

$$\Delta\text{Ppapr} = P_{[Clipped]} - P_{[Not\ Clipped]}\ \text{dß} \quad (14)$$

Where $P_{[Clipped]}$ gives the value of CCDF when clipping is exercised

- Total system degradation[4] states the transmission of the system which is defines as

$$Toatl\ sys\ Deg = \Delta\text{ENR} + \text{InBO} \quad (15)$$

Where ΔENR is degraded energy per bit and InBO is input back off value

- Third factor ,Average peak power difference shown by ΔP

$$\Delta\text{P} = Avg_{[\text{clippedvalue}]} - Avg_{[\text{noclippedvalue}]} \quad (16)$$

Where $\text{Avg}_{[\text{clipped value}]}$ is the mean power of clipped signal and $Avg_{[\text{no clipped value}]}$ is the value obtained when no clipping is done.

Modulation scheme	QPSK
Subcarrier number	M=128
Oversampling factor[4]	L=4
Channel [4]	AWGN

TABLE 1: Modelling measurements

Figure 4:original MB-OFDM sequence, peak sequence and outputs of different clipping techniques .MB-OFDM sequence which demonstrates that more number or users using the band (i.e 1500's in number)while the other subplots depicts the amplitude clipping by the different clipping techniques[4].

Figure 5: Total system degradation Vs input back off (IBO) This figure depicts the system degradation performance when the different clipping techniques are applied at the Bit Error rate of 10^{-2}. classical clipping and deep clipping have well-nigh the same result in this case, where as the smooth clipping technique gave more power degradation compared with the remaining two the minimum system degradation value for classical and deep clipping is around 6.5dB but for smooth clipping it is around 7.5dB.As per this parameter considered .final line ,this deep clipping is good with minimum loss of 6.43dB (classical clipping=6.54dB)

Figure 6:different clipping ratios[4] and their effect on the Peak to average power ratio reduction performance for deep clipping technique This figure provides the performance of the PAPR reduction by deep clipping technique at different clipping ratios (for convince only three values are considered).the value of PAPR remains almost constant for the clipping ratio values < 3dB,where as for the clipping ratio values >3dB the PAPR value varies .For the clipping depth factor (CDF)[4] value greater than 0.5,the graph shows nigh same value of PAPR (whatever may be the clipping ratio value).

Figure 7: clipping ratio effect on the PAPR reduction gain. This figure exemplify the PAPR Reduction gain performance[4] for different clipping ratio values for different clipping techniques .PAPR reduction gain value for classical clipping is next to smooth clipping. There is a linear decrease in the gain value from clipping ratio=4dB.deep clipping shows good performance compared with classical and smooth clipping techniques .the gain value decreases from CR=8dB for deep clipping. After 10dB of clipping ratio value the reduction gain becomes zero and there will be no more reduction.

Figure 8: clipping techniques-classical clipping, deep clipping, smooth clipping and heavy side clipping analysis through average power deed. This figure shows the different clipping techniques performance based on average power [1]. Transmission quality is affected by transmission signal average power .so the technique which has avg power=0dB is considered to be the best. There is decrease in the average power with clipping ratio factor increase in case of deep, classical and smooth techniques from clipping ratio factor=4dB.Heavy side clipping have no effect by clipping ratio on PAPR reduction gain so the avg power=0dB.so it is considered as best at CR[4] factor =4dB to 6 dB.

Figure 9: peak to average power ratio reduction by clipping techniques. This figure demonstrate the different clipping techniques performance on PAPR reduction .the value of PAPR without applying any clipping technique is obtained as 29.84dB.while classical clipping gave nearly half of the value (14.29dB).smooth and deep clipping techniques gave similar outputs around 8dB. In particular smooth clip technique gave the best result of 7.83dB.

Figure 10: Bit error rate verses energy per bit [4] of different clipping methods .This shows that the Smooth clipping is more advantageous compared to the deep clipping and the classical clipping technique.BER Vs Eb/NO graph here shows that the clipping techniques showed good output than without clipping

5. OUTPUTS

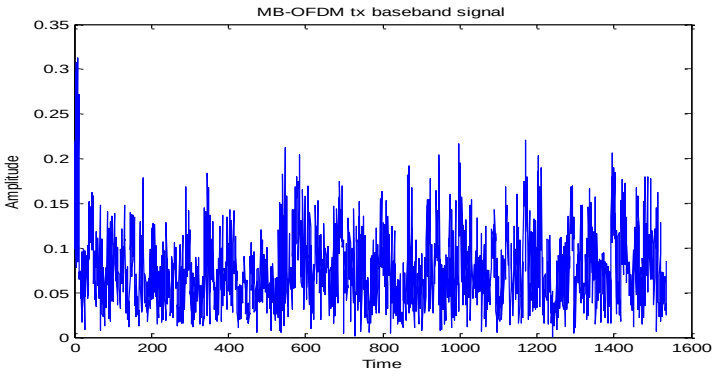

Figure 3:MB-OFDM Transmitted Baseband Signal

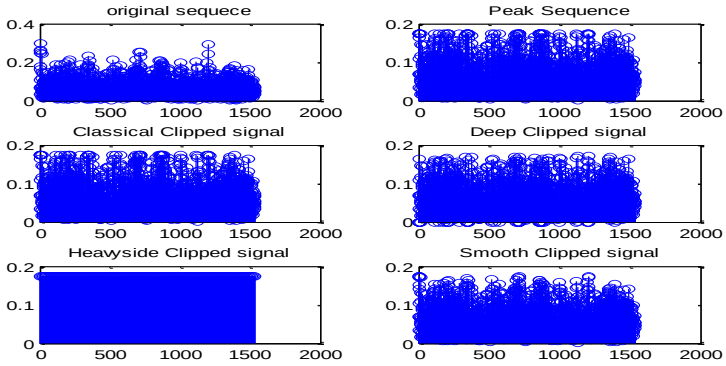

Figure 4: Original MB-OFDM Sequence, Peak Sequence And Outputs Of Different Clipping Techniques

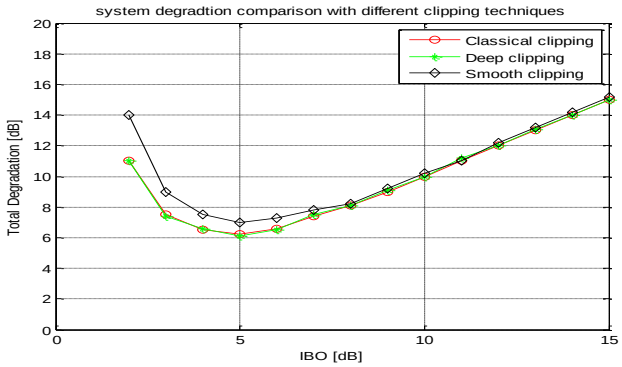

Figure 5: Total System Degradation Vs Input Back Off(IBO)

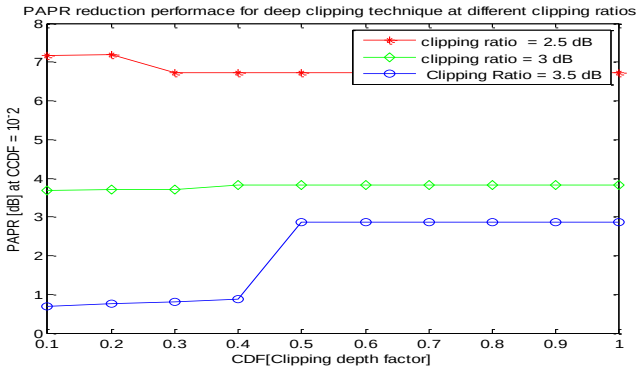

Figure 6: Different Clipping Ratios [4] And Their Effect On The PAPR Reduction Performance For Deep Clipping Technique.

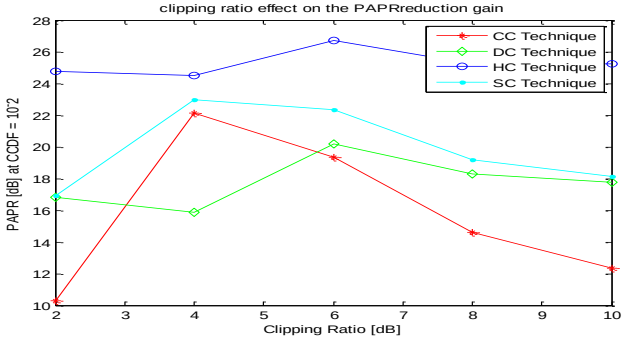

Figure 7: Clipping Ratio Effect On The PAPR Reduction Gain.

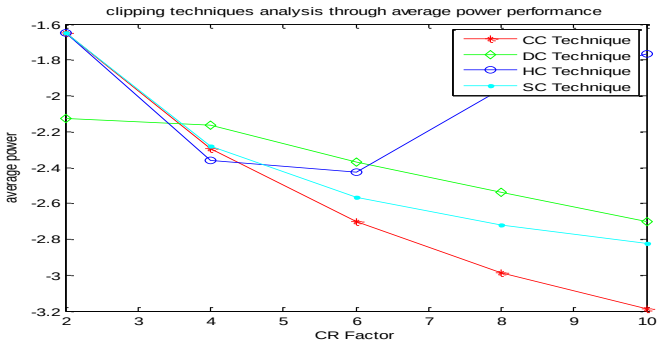

Figure 8: Clipping Techniques Analysis Through Average Power Deed.

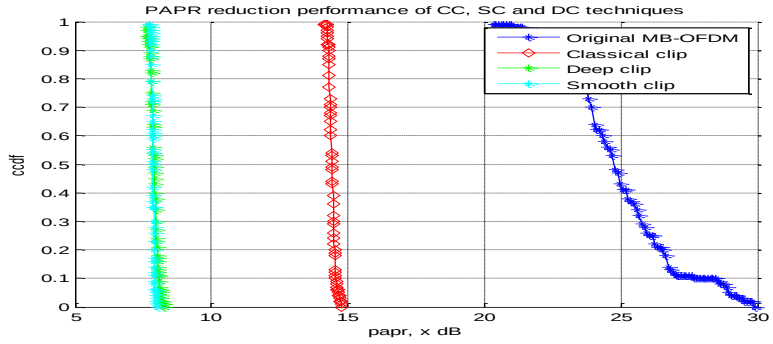

Figure 9: Peak To Average Power Ratio Reduction By Clipping Technique

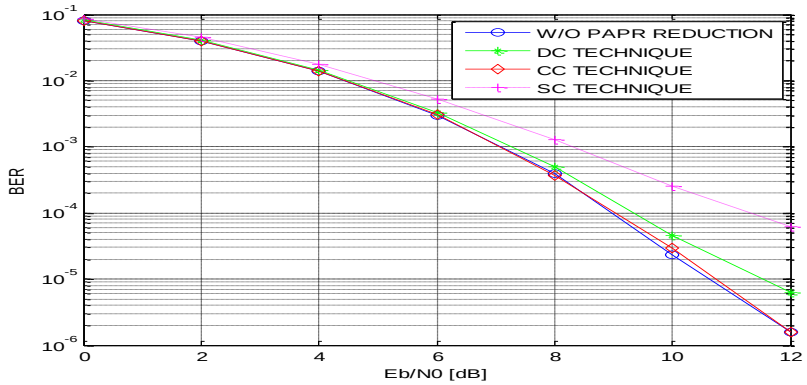

Figure 10: Bit Error Rate Verses Energy Per Bit [4] Of Different Clipping Methods

6. CONCLUSION

Although tremendous progress has been made in the past decade to reduce the PAPR in OFDM system but still it is consider as an area of concern in the wireless communication scenario. MB-OFDM[5] for UWB technology[6] flaunts a noumenon technacy for prominent set of short range (distance) and high performance application. But this scheme causes high Peak-to-Average Power Ratio (PAPR) resulting in the saturation of High Power Amplifier.

In this work a genuine weighted scheme is forth put to minimise the PAPR [1]in an efficient way without any distortion and successfully remove the respective weights at the receiver end. The reduction of PAPR in multicarrier system mainly relies on condition that time consumes at the Transmitter end should be same as at the receiver end.

In this paper a comparative analysis between different clipping methods[4] Classical-Clipping (CC), Heavy side-Clipping (HC), Deep-Clipping (DC) and Smooth-Clipping (SC)in terms of total system degradation, Peak to average power ratio(PAPR) reduction and average power performance is accomplished. Heavy side clipping have the worst results amongst the four because of its high Bit error rate (BER) degradation. After intense research and experiments finally DC clipping technique is best resultant among four clipping techniques because it gives best result in considered parameters- total degradation, average system power and PAPR limiting .When the depth factor of deep clipping is equivalent to zero Deep and classical clipping(CC)techniques are identical . It is envisioned to define the wireless links engross the communication rate to the intense.

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ERROR CORRECTION FOR PARALLEL FIR FILTERS USING HAMMING CODES

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ABSTRACT

In this paper ,we propose a error correction for parallel FIR filters using Hamming code in which single parallel FIR filter is taken as a bit in ECC technique. In many complex circuits, reliability plays a crucial role and it requires fault tolerant filter implementations. Now a days, technology grows up, the complex system use many filters which operates simultaneously. Consider an example in which same parallel filter is applied to different inputs. To achieve fault tolerance, an ECC technique uses the presence of parallel filters are considered. The ECC technique provides protection where more number of parallel filters are used by using the case study, the effectiveness in error correction and circuit design cost is evaluated.

KEYWORDS

Soft Errors, FIR filters, Error Correction Codes.

1. INTRODUCTION

Digital filters plays a vital role in DSP systems. Now-a-days, complex circuits are rapidly increasing in many applications in which their reliability is critical.To meet the intrinsic reliability challenges like manufacturing variations and soft errors,fault tolerance is introduced. If redundancy is added at the logic level the faults occurred in the circuit can be reduced and its system functionality will not be affected by those errors. The common technique i.e. ,Triple Modular Redundancy (TMR) is used to add redundancy.TMR triples the input block and to correct errors it adds voting logic.The disadvantage of TMR is the area and power of the circuit is increased and it doesnot acceptable to some applications.

The block diagram for TMR is shown in figure 1,

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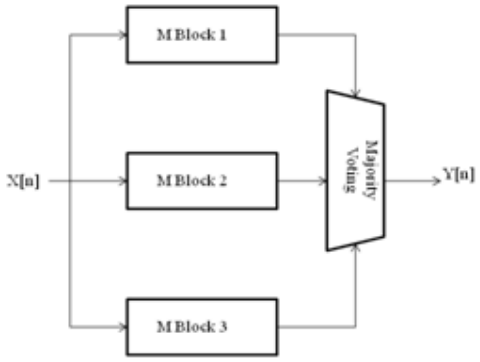

Fig 1:Triple Modular Redundancy

RPR is used to reduce the circuit design cost.The FIR filters protection is done by using residue number system and arithmetic codes are proposed.The Error Correction Codes(ECC's) with hamming protection is presented.when the parallel FIR filters are larger in number,then it enables efficient implementations.By using advanced ECC's can correct failures in multiple modules and powerful protection is also provided.

2.PARALLEL FILTERS WITH SAME RESPONSE

The parallel FIR filter implementations are used for high performance applications.FIR filters are mostly used because they have good stability and they are easily designed to match a given response.
The general FIR filter equation is summerized as,

$$y[n] = \sum_{i=0}^{N-1} x[n-i].h[i] \qquad \text{……..(1)}$$

Consider input data and parallel filters with same response .The diagram for parallel filters are shown in figure 2.

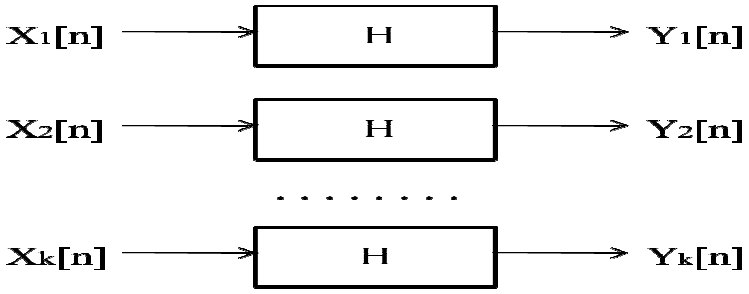

Fig 2:Parallel Filter With Same Response

Hamming codes are used to protect FIR filter to achieve an optimal design and to reduce resource consumption.Hamming codes are also called as block codes and the Hamming Rule is determined as,

$$2^{P} \geq x+p+1 \qquad \text{.....(2)}$$

Where, X : Number of data bits,

P : Number of parity bits.

3.PROPOSED METHOD

By using ECC scheme,the parallel FIR filter with hamming code is designed.Consider an ECC with 4 data bits and 3 parity check bits to produce 7 bits.For example,take a simple Hamming code of K=4 and n=7.By using data bits d1,d2,d3,d4 the parity check bits p1,p2,p3,p4 are computed as a function of,

p1=d1 xor d2 xor d3

p2=d1 xor d2 xor d4

p3=d1 xor d3 xor d4

.....(3)

If there are any errors in one of the bits,the total bits are stored and recovered later.The parity bits are calculated again and by using stored values the results are compared.The Hamming code with generating G matrix and parity check H matrix are,

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \qquad H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

From above example,

The error in d1 causes errors on p1,p2,p3 check bits and the error in d2 causes errors on p1 and p2 and an error in d3 causes on p1 and p3 and finally error in d4 causes on p2 and p3.
The error bit position is shown in table 1 as,

S_1 S_2 S_3	Error Bit Position	Action
0 0 0	No Error	None
1 1 1	d1	Correct d1
1 1 0	d2	Correct d2
1 0 1	d3	Correct d3
0 1 1	d4	Correct d4
1 0 0	p1	Correct p1
0 1 0	p2	Correct p2
0 0 1	p3	Correct p3

Fig 3:Error Location In Hamming Code

The architecture for 4 parallel FIR filters & hamming code is given in figure 4,

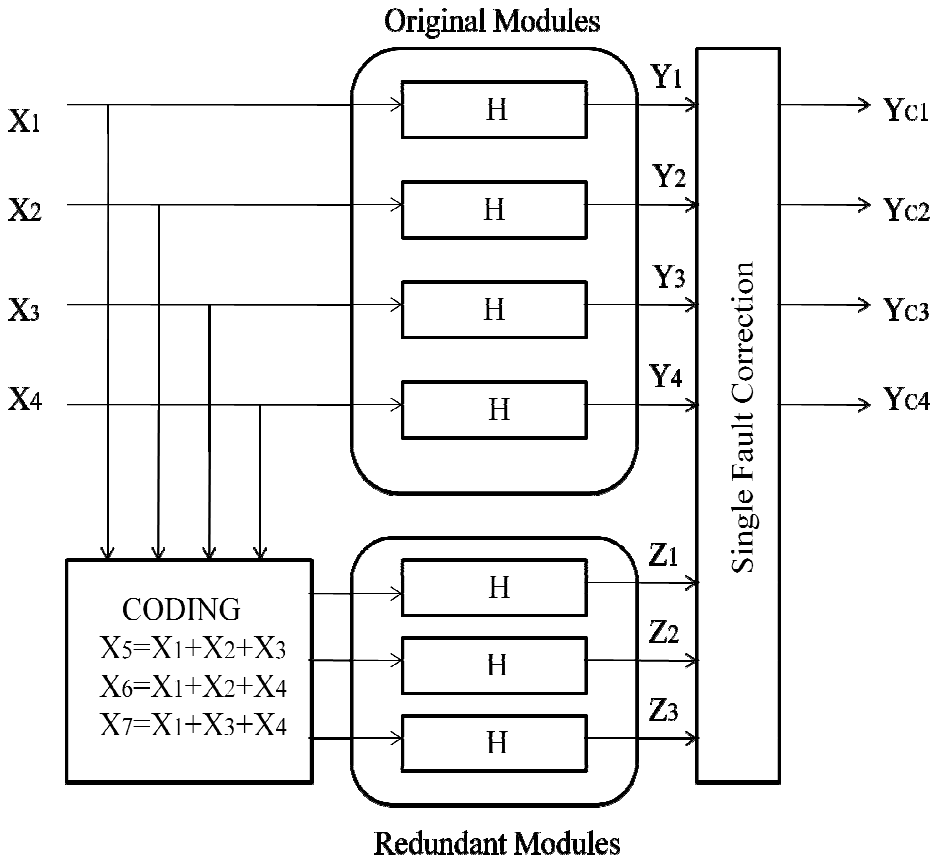

Fig 4:ECC Based Scheme For 4 Filters & Hamming Code

The calculations are, Encoding is calculated as, $y = x \bullet G$ ……..(4)
Where syndrome is calculated as,

$$S = y \bullet H^{T} \quad \text{……..(5)}$$

where • denotes XOR and multiplication operation .To identify the bits in error the syndrome is used for correction.when the error bit is found,it can be corrected by inverting the bit.
The check filters Zj is calculted as,

$$Z_1[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_3[n-l]) \cdot h[l]$$
$$Z_2[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_2[n-l]+X_4[n-l]) \cdot h[l]$$
$$Z_3[n] = \sum_{l=0}^{\infty} (X_1[n-l]+X_3[n-l]+X_4[n-l]) \cdot h[l]$$

…….(6)

Checking is done by,

$$Z1[n] = Y1[n]+Y2[n]+Y3[n]$$

$$Z2[n] = Y1[n]+Y2[n]+Y4[n]$$

$$Z3[n] = Y1[n]+Y3[n]+Y4[n]$$

…….(7)

Consider an example ,if an error Y1 is detected the error is corrected by,

$$Yc1[n] = Z1[n] – Z2[n] – Z3[n] \quad \text{……(8)}$$

Consider eleven parallel FIR filters with hamming code of total 15 bits including four redundant bits .The reductions for eleven parallel filters are large only when number of filters are larger.By using the traditional ECC's if number of filter increases,the overheads decreases.There is a trade off between area and delay i.e., if area is increased the delay is reduced in 11 parallel filters.Finally the circuit complexity is less when compared with 4 parallel filters and the circuit cost is also low.The above results are confirmed by using a case study.

By using a case study consider 16 coefficients with input bits and filter coefficients . Two evaluations are implemented for a block of parallel filters with data bits k=4 & k=11 and total bits n=7 & n=15 bits. These techniques are synthesized and simulated by using a Xilinx tool.

The fault injection experiments and effectiveness in terms of error correction is done by using eleven parallel filters.For input filters and the coefficients the errors are injected randomly and in all these cases the single errors can be injected & it can be detected and corrected.So, by using

case study the effectiveness is confirmed to correct the single errors and system cost is determined.

4. SYNTHESIS & SIMULATION RESULTS

The RTL Synthesis and Simulation results for proposed system are given below.

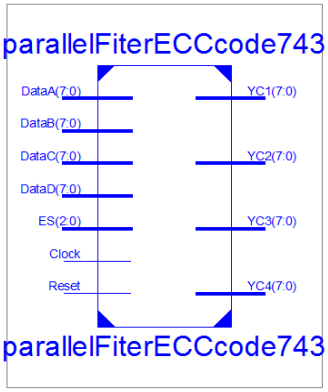

Fig 5:RTL Schematic For 4 Parallel Filters

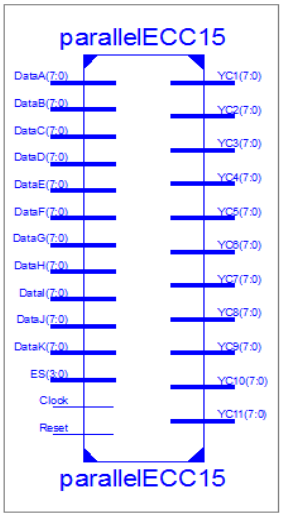

Fig 6:RTL Schematic For 11 Parallel Filters

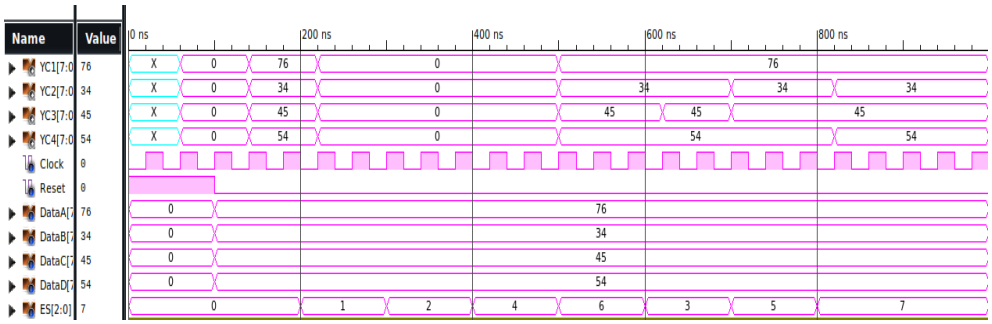

Fig 7:Simulation Result For 4 Parallel Filters

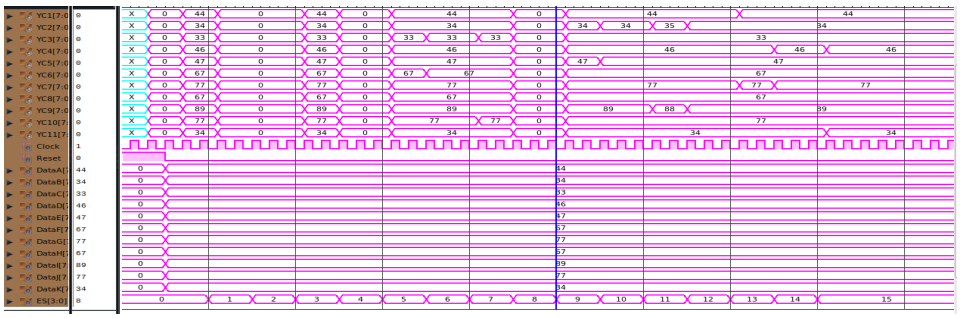

Fig 8 : Simulation Result For 11 Parallel Filters

4.1.Timing Report

For 4 Parallel Filters:

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.027ns (Maximum Frequency: 493.340MHz)
   Minimum input arrival time before clock: 3.399ns
   Maximum output required time after clock: 12.031ns
   Maximum combinational path delay: No path found
```

For 11 Parallel Filters**:**

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 2.058ns (Maximum Frequency: 485.909MHz)
   Minimum input arrival time before clock: 4.804ns
   Maximum output required time after clock: 4.368ns
   Maximum combinational path delay: No path found
```

5. CONCLUSION

By using the proposed scheme the protection of parallel FIR filter can be done in DSP systems. The error detection and correction is done by applying ECC's to parallel filter outputs.The effectiveness i.e., circuit overheads and single fault correction is discussed by using case study.The performance is improved in terms of delay is reduced.

The future scope is the scheme is also done for IIR filters instead of FIR filters. Another extension is instead of using hamming codes another error correction codes can be used.

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FRAMEWORK FOR SECURING EDUCATIONAL E-GOVERNMENT SERVICE

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ABSTRACT

Enhancement in technology is leading to a change in the way governments, individuals, institutions and business entities provide quality services to the citizen. Today's education system plays crucial role for developing cognizance in society so e-government service is obliged to integrate with educational system. In this work we proposed a novel framework for integrating educational service within e-government services. One of the main tasks of this paper is to explore or propose a Secure Examination Management System (SEMS). The system has been designed using cryptographic primitives, which enables students to take the exam from anywhere. The student is allowed to take the exam after he gives his necessary authentication details. In SEMS, it is important to exclude false students while ensuring the privacy for the honest students. It allows evaluators to share student examination papers for evaluation with proper authentication. This is done using digital signatures, authentication and confidentiality provided by public key cryptographic system.

KEYWORDS

Framework, Educational System, Secure Examination, E-government services, Encryption, Examination Server, Authentication.

1. INTRODUCTION

In today's society, e-government and digital government are those terms that are used to describe the application of information and communication technologies (ICTs) to improve public services, educational services and to increase citizen participation in democratic government [1]. In most of the countries, e-government has been the dominant term used for policy-making. This term gives emphasis on user-centric services that can be integrated to support easy and efficient use of services by citizens, businesses and education services as shown in Fig.1.

Fig.1. E-government Service Components

1.1. E-Government Services

Electronic Government or e-government is at the forefront of current public sector reform policies across the world, where the use of computer-based information and communication technologies (e.g. telecom networks, computers and mobile phones) to deliver public services in the public sector is seen as a major leverage of public sector innovation. E-Government is usually seen as using ICT in order to provide easy and very efficient access to government information and services to the citizens, businesses and government agencies and also improve the quality of services, by increased speed and efficiency, provide citizens with the opportunities to participate in different kinds of democratic processes [2]. The digital interactions between a citizen and their government (C2G), between governments and government agencies (G2G), between government and citizens (G2C), between government and employees (G2E), and between government and businesses/commerce (G2B). Essentially, e-government delivery models can be broken down into the following categories [3], which shown in Fig.2.

- G2G (government to governments)
- G2C (government to citizens)
- G2E (government to employees)
- G2B (government to businesses)

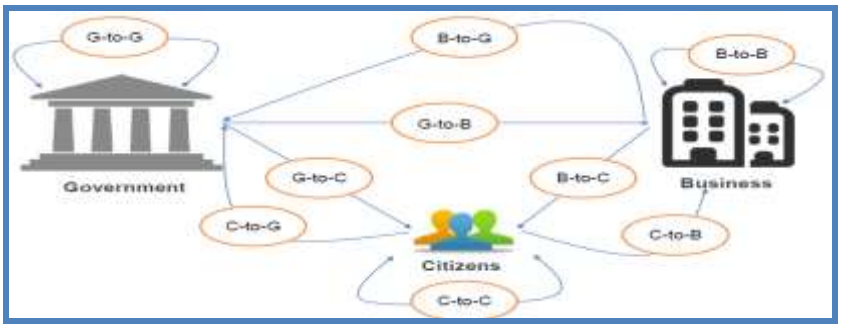

Fig.2. Digital interactions between e-government service components

1.2. Benefits of E-Government Services

So many authors explained about the use of the e-government services in their tasks. Accordingly the benefits of these services are described in [4] as follows.

- **Huge or large benefits are offered by the e-government for citizens through:** It is providing the every government information and services through a single window. It

allows more flexibility and convenience for most of the government offices and agencies, through online access of services. Here, it meets the target of minimizing the turn-around time for citizens in the provision of every government services.

- **Businesses also benefited by it:** e-government is serving as a gateway for the mutual development and beneficial interactions between the government and businesses. It is eliminating the administrative procedures when dealing with the government, thus resulting in considerable time and costs savings for the businesses; and providing a secure and trustworthy environment for conducting online transactions with the government.
- **An E-Government service helps the government by:** It is improving the means of providing information sharing and communication among all those government offices that belongs. As the result of this, there is a major enhancement in the organization of most public sector resources. Here, it avails more tools in order to solve the raising number of problems that facilitates efficiency of related issues.

1.3. Need of E-Government Services in Education System

Education is the key service in the society where we are living. There is no question about the importance of this sector for the society. Unfortunately, no emphasis is given to incorporate it to the e-government services. In this sector, there is a high competition among the students for to be employed but most of the tasks are within the government offices. By incorporating this sector, we can improve issues like vacancy and their exam requirements.

Using ICT as a means, education is becoming moving from a knowledge-transfer model to a collaborative, active, self-directed, and engaging model that helps students increase their knowledge and develop the skills needed to succeed in the "Learning Society [5]. So the need of e-government services in education system plays a vital role in the present society.

Technology is just one of many methods that have its own contribution in education today [5]. This is to say we are living in the age where the assets of information and the acquiring of new things bring its own impact on educational institutions to rethink the means of teaching and learning in a global market. Accordingly, this system also needs to follow an appropriate guidelines and one of the major element from this service is delivering its assessment sub service in a secured way.

But from our discussions, reading and revision so far no one: be it an individual, public and private sectors give an appropriate emphasis on educational systems especially on making the exams at different stages of educational hierarchy to be a secured one. So, the purpose of this study is to build an initial framework to secure the sub service of the educational system.

2. LITERATURE REVIEW

Steve Harrison [6] tried to develop a framework by utilising the Open Web Application Security Project's (OWASP) Application Security Verification Standard (ASVS). The author in his work focused on developing his own security framework that can be used within Agile sprints to develop secure applications and to give assurance to the business owner that any technical risks have been mitigated.

Geoffrey Rwezaura [7] focused on proposing a framework for enhancing services in government to efficiently offer secure way of e-government services. He came up with a new approach by

incorporating security services into eGMMs. In addition, he enhanced the awareness, need and importance of security services to be an integral part of eGMMs to different groups such as research organizations, academia, practitioners, policy and decision makers, stakeholders, and the community.

Min-Shiang HWANG [8] proposed a classification of e-government applications and some problems in e-government by considering from the four perspectives such as technical, political, cultural, and legal aspects.

However; in all the above tasks the authors in their research strategies did not take into consideration about the education system in e- government services, which we believe that this is one of the important sectors to be considered. Besides, there is no task so far on the secured based framework on this area.

3. THE PROPOSED FRAMEWORK

Framework is always needed to do tasks as per their standards; hence we came up with the framework that facilitates to conduct secured exams as shown in Fig.3. The proposed framework addresses the integration of educational service within the existing e-government services. The framework was developed with the intension of responding to the inefficient and weak privacy checking systems of conducting exams in government educational system. The Secure Exam Management System (SEMS) will be assumed to serve as a benchmark for conducting secured examination in educational e-government services. This helps to improve the standard of conducting examination for the entire educational system in the present and puts great milestone for the upcoming society too.

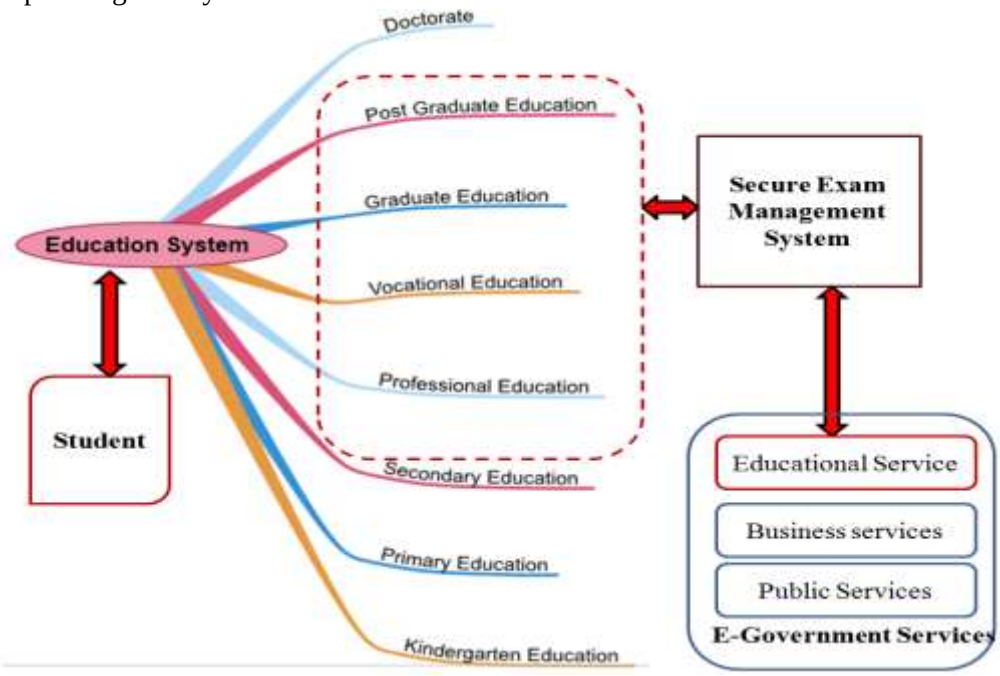

Fig.3. Framework for SEMS

The framework also addresses a lot of security related issues. Some of these concepts include proper way of using information: privacy, modification and availability. The use of these are

making a genuine method of assets being stored, processed, and transmitted within and between e-government domains(government , education service, students, employees) as shown in Fig.4.

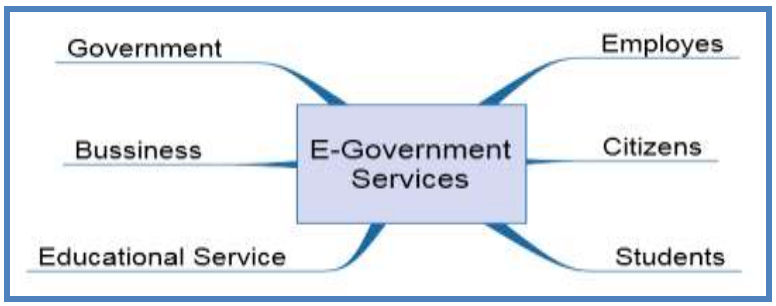

Fig.4. E-government service domains

3.1. The Secure Exam Management System (SEMS)

Examination system is one of the efficient methods for testing the ability of students in any education system. Examination is considered to be very crucial process in determining the progress and mostly about the understanding of subjects or courses of any academic activities. But currently examination is taken without properly identifying the target individuals, conducting the examinations and evaluating them. Using Secure Exam Management System (SEMS) these very weak methods of assessments and arrangements will be eliminated.

SEMS has been designed using cryptographic primitives, which enables students to attend examination from anywhere. The student is allowed to write exam only after his registration process has been completed and verified by the system for secure authentication purpose. In this system students are allowed to write objective and descriptive type examinations [9]. It allows evaluators to share student examination papers for evaluation with proper authentication. Instructors can design the model papers and conduct examinations with efficient security. SEMS is considered to be one of very important methods for faster, safer and efficient implementation of examination procedures for the progress of academic activities. Registering the users and identifying them as valid are the most important phases where security must be provided to the at most level. Examination paper will be generated at the time of examination so that reliability is maintained.

This paper is an effort towards attaining a good if not the best solution to the registration and identification of students in SEMS and provides confidentiality to question papers, answers, evaluation & results. The answer papers are encrypted by using student's private key & decrypted by using student's public key. The SEMS also supports the requirements, such as completeness, soundness, privacy, un-reusability, eligibility, fairness, authentication, confidentiality, receipt-freeness, non-duplication, public participation, and private error correction.

With the above requirements in mind, our goal was to develop a secure, user-friendly SEMS, which can be accessed anywhere from any place. Besides, there are three steps absolutely required for any of the examination system. These are registration, examination and evaluation.

1. For registration, the student must send user authentication details to SEMS, which goes to the appropriate administrator to his identity, prove for secure authentication, and stores that in server along with some essential authentication details.
2. For examination, the student can simply download the exam applet from his client system, and he need to provide his authentication details, and it is to be verified by the system.

3. For evaluation, evaluators can share all the exam papers among themselves for perfection. The results announced without delay.

We also able to maintain a centralized database containing the details of all the students who have registered and they can be accessed from any client system, so that they can write examination from anywhere.

3.2. System Design

There are three main stages:

1. Registration
2. Examination
3. Evaluation

Notation Used

→ WAP : Wireless Application Protocol
→ AS : Admin server
→ EVS : Evaluating server
→ ES : Examination server
→ Vi : Student i
→ vi : Examination selected by Student from mobile phone
→ KU : Public key
→ KR : Private key

1. Registration Stage

Fig.5. shows the registration process of SEMS where students at the Examination server (ES) accesses the AS to download the registration form and submit the authentication details. These details are encrypted with public key of WAP and then sent to AS. AS decrypts them with its private key. If the student signature does not match with the one at AS then, AS gives an error message. Otherwise the student is allowed to enter the examination stage.

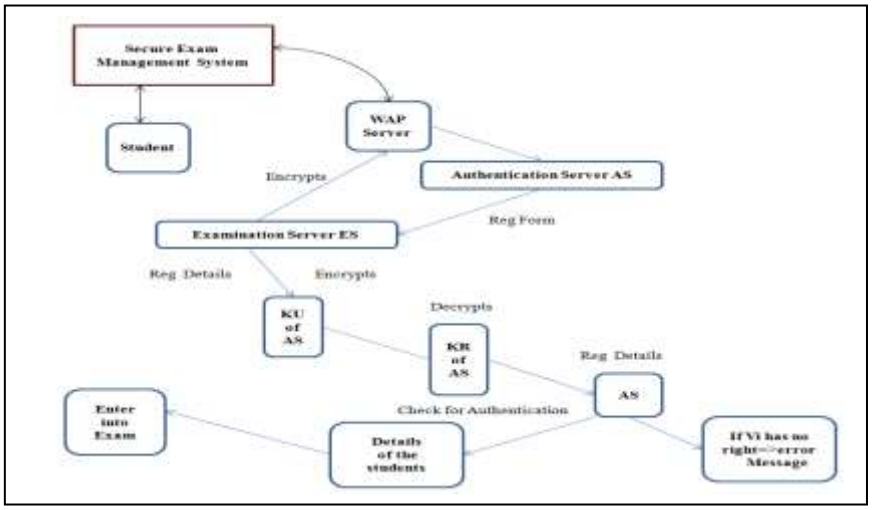

Fig.5. Registration Stage

2. Examination Stage

In the examination stage as depicted in Fig.6, AS checks whether the student has previously was taken the examination or not. If the student has already taken the examination, AS rejects him or her. Otherwise the student is allowed to download the examination form. Then, the student selects an examination vi and this is encrypted with the public key of ES as xi. Encrypted examination xi is then blinded as ei. Examination ei is then signed by student as si and sent to AS. AS verifies the signature si of examination ei, if it is valid gives its signature to the examination ei as di. This is sent back to the student. Student retrieves the examination di and unbinds it to get yi. (xi, yi) is then sent to the ES.

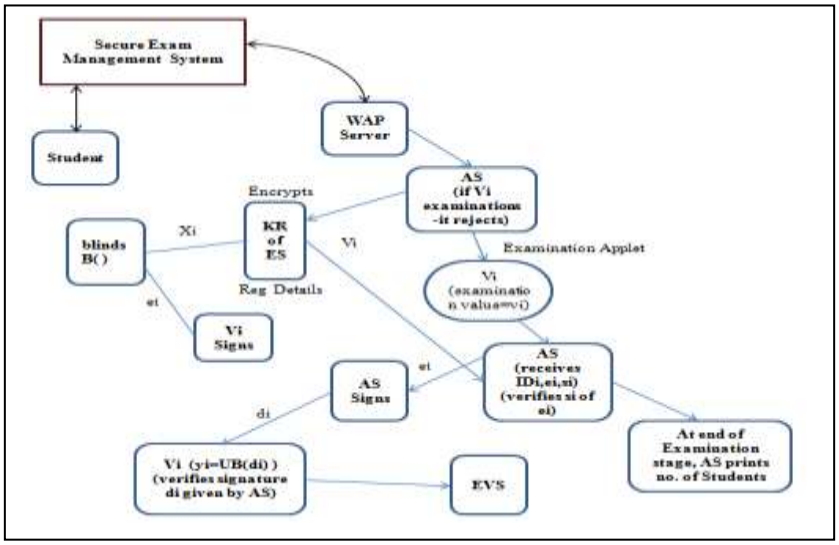

Fig.6. Examination Stage

3. Evaluation Stage

Fig.7 shows the evaluation process of SEMS, here EVS checks whether yi is valid signature of xi. If verification fails the examination is discarded. Otherwise EVS decrypts the examination xi with its private key and stores the examination results in the database. EVS publishes the examination results after the evaluation period is over. Students can view their results immediately after the evaluation process has been completed.

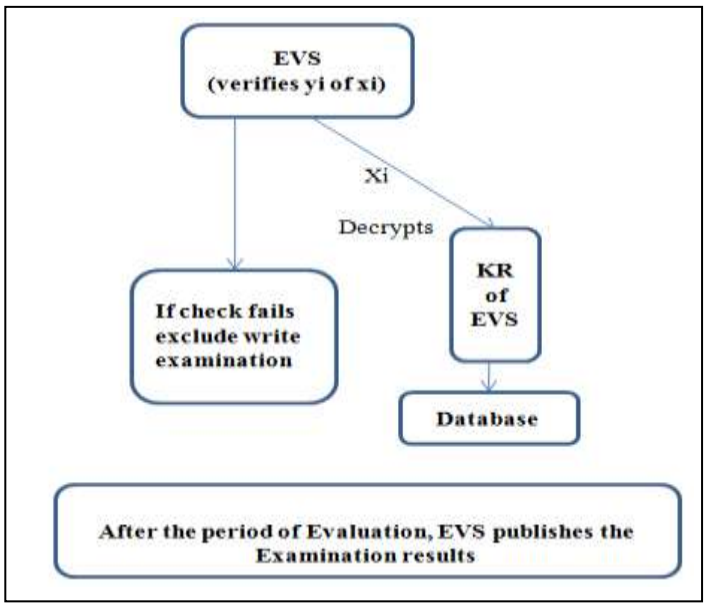

Fig.7. Evaluation Stage

4. CONCLUSIONS

This paper is aimed for developing a novel framework for integrating educational service with e-government services. In doing so, we identified the problems seen in currently educational systems to conduct exams. A framework was proposed that facilitates delivering examination for all categories. Moreover, we designed a Secure Examination Management System (SEMS) that helps the eligible student to take examination from anywhere, make all the assessments processes very efficient, transparent for every one and also facilitates the students to know their results very fast. In essence, it will create a greater and smooth environment in the education system.

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A DESIGN OF DOUBLE SWASTIKA SLOT MICRO-STRIP ANTENNA FOR ULTRA WIDE BAND AND WiMAX APPLICATIONS

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ABSTRACT

This paper presents a design of double Swastika Slot Micro-strip Antenna which can be used in UWB and WiMAX Applications. The proposed antenna operates at resonant frequencies 3GHz and 3.11 GHz. At 3GHz obtained value of VSWR is 1 and return loss is -42dB and at 3.11 GHz VSWR is 1.7 and return loss is -12dB. RT Duroid having dielectric constant 2.2 is used as substrate. Here the double Swastika slot Antenna is fed with the coaxial feeding technique.

KEYWORDS

VSWR, Return loss, Double Swastika slot antenna.

1. INTRODUCTION

Circularly Polarized Micro-strip antennas are widely employed in UWB, WiMAX, RADAR, mobile Communication, aircraft, spacecraft, satellite communication and RFID applications where small size i.e. portability, low cost, high performance, ease of installation, low power consumption and the capability to transmit information at high data rates are major constraints. Liability to transmit and receive maximum power is influenced by polarization of the antenna. UWB is a promising technology for many real time applications as this technology consumes very low power and WiMAX technology provides portable mobile broadband connectivity across nations through a variety of devices. A Compact design of double slotted swastika antenna for circular polarization is proposed and introduced. Circular polarization is brought about by Embedding micro Swastika slot with in main Swastika slot. Since RT Duroid offers better radiation it is selected as a substrate. It offers many advantages such as lowest dielectric loss, low moisture absorption, uniform electrical properties over entire frequency range, high thermal Resistance and conductivity, excellent characteristics for High frequency and excellent high speed and functionality for portable electronic devices in rapidly expanding mobile network. Major limitations of Micro-strip antenna are its narrow Bandwidth and Gain .The design of

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portable antenna configuration further deteriorates the two parameters, which is the most serious disadvantage preventing it from being used in microwave applications.

Therefore portability, along with Gain and BW enhancement is becoming major design considerations for real time applications of Micro-strip antenna for wireless communication. Here we are proposing an innovative technique to enhance gain and BW of Micro-strip patch antenna. Slots are cut into double swastika shape to improve the BW and also satisfies convenient impedance matching over entire broad frequency of operation. Characteristics such as dual and circular polarization, dual frequency operation, broad bandwidth, feed line flexibility and so on are easily obtained in this patch shape. Patch is excited by coaxial feed in this particular design. Simulation and Experimental results of antenna are prescribed and discussed here.

2. ANTENNA DESIGN & CONFIGURATION

Slots are cut in the design such that they appear in the shape of Double Swastika slot antenna. The Inner Swastika slots are extended from main Swastika slots and the legs of Inner swastika slots are smaller than the legs of the main Swastika slots. The shape of double Swastika slots could provide desired Band width because of variations in the current distribution and the radiation pattern at the edges. Patch width is properly adjusted to get improved results.

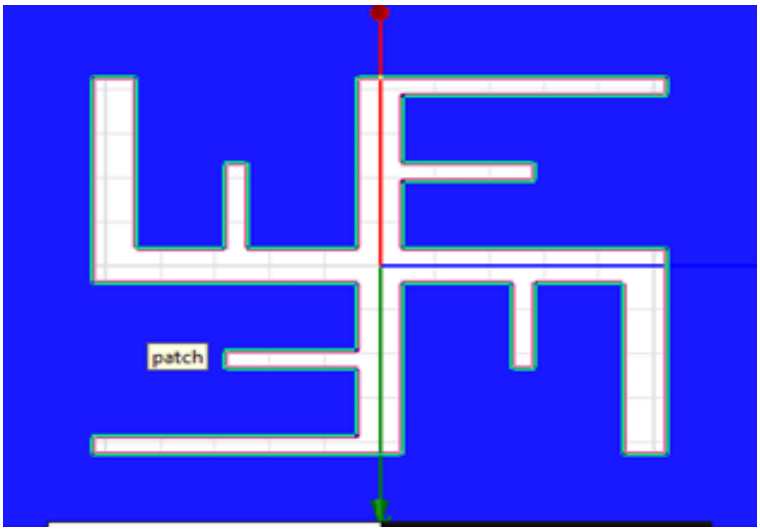

Fig.1 Double swastika slot

Design Equations:

$$\Delta L = 0.412h\frac{(\varepsilon_{reff}+0.3)(\frac{W}{h}+0.264)}{(\varepsilon_{reff}-0.258)(\frac{W}{h}+0.8)}$$

$$W = \frac{c}{2f_o\sqrt{\frac{(\varepsilon_r+1)}{2}}}$$

$$L_{eff} = \frac{c}{2f_o\sqrt{\varepsilon_{reff}}}$$

$$\varepsilon_{reff} = \frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left[1+12\frac{h}{W}\right]^{-\frac{1}{2}}$$

Where,

ΔL = increased length due to fringing effect

W = Patch width of the antenna

L_{eff} = Effective length of the patch

ε_{eff} = Effective dielectric constant of the substrate

C = Speed of light

h = height of the substrate

f_0 = Resonant frequency

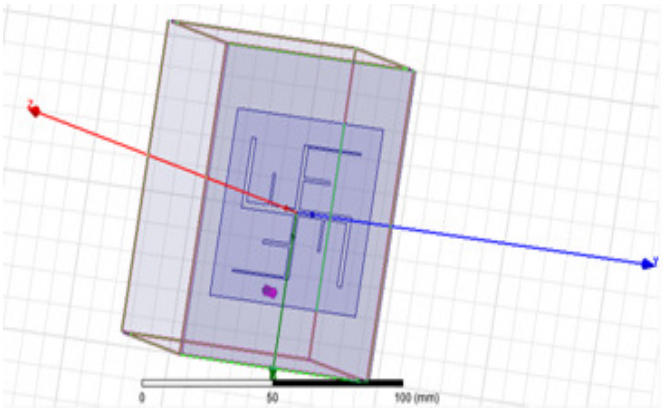

Fig.2 The construction view of double swastika slot antenna with feed

Micro-strip antenna in general can be fed from underneath via a probe as shown in the above figure. The outer conductor of the cable is connected to the ground plane, the center conductor is extended up to reach the patch antenna and the antenna efficiency in terms of return loss mainly depend up on the impedance matching between patch and transmission feed line. We get more efficient results when both transmission feed and patch have perfect impedance matching.

The position of the feed can be altered to control the input impedance. The coaxial feed introduces an inductance in to the feed point that may need to be taken into account if the height h gets large i.e. an appreciable fraction of wavelength. In addition the probe will also radiate, which can lead to radiation in undesirable conditions. The main aim to use coaxial or probe feeding is that, it enhances the gain, provides narrow bandwidth and perfect impedance matching.

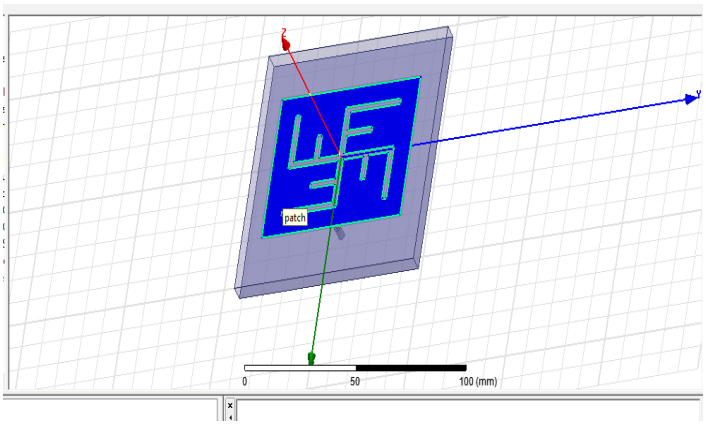

Fig.3 Top view of Double Swastika Slot Patch Antenna

Feed point is varied to different positions to get good radiation and impedance matching. While cutting the slot optimum dimensions should be considered. So the dimensions of slot are important for good efficiency of antenna.

3. THE DESIGNING PARAMETERS

Length of the patch(Lp)	60mm
Width of the patch(Wp)	70mm
Height of the substrate(Hs)	1.6mm
Length of the substrate(Ls)	100mm
Width of the substrate (Ws)	90mm
Outer cylinder Radius (Rout)	1.6mm
Inner cylinder Radius (Rin)	0.7mm
Height of the air box (Ha)	40mm

Correct position of substrate, ground and patch can be obtained by properly using the following equations. Ten rectangular boxes (gaps) are required to get the shape of double swastika slot patch antenna. Slot sizes can be varied using the following equations.

1. Substrate - Ls/2,Ws/2,0mm
2. Ground - Lp/2,Wp/2,-h
3. Patch – Lp/2,Wp/2,,0mm
4. Gap1 –lp/2-(c+e) ,-d/2 ,0mm
5. Gap2--d/2 ,-k/2 ,0mm
6. Gap3 -lp/2-e ,k/2 ,0mm
7. Gap4 -(lp/2-e)-a ,-k/2 ,0mm
8. Gap5 --lp/2+e ,-k/2 ,0mm
9. Gap6 -lp/2+e ,k/2 ,0mm
10. Gap7 -((c/2)+(d/2))/2 ,m/2+d/2 ,0mm
11. Gap8 -((c/2)+(d/2))/2 ,(m-k/2) ,0mm
12. Gap9-((c/2)+(d/2))/2,-((k/2)+(d/2))/2 ,0mm
13. Gap10 -((c/2)+(d/2))/2 ,k/4+d/4 ,0mm

14. Air box-((c/2)+(d/2))/2 ,k/4+d/4 ,0mm

Where

C=lp-(2*lp/7)

k=wp-(2*(wp/8))

e=(lp-c)/2

m=(k/2)-d/2

4. RESULTS & DISCUSSION

In the design, dual band frequency characteristics are obtained and the analysis using HFSS simulation tool resulted in acceptable values for Return Loss, VSWR and Gain.

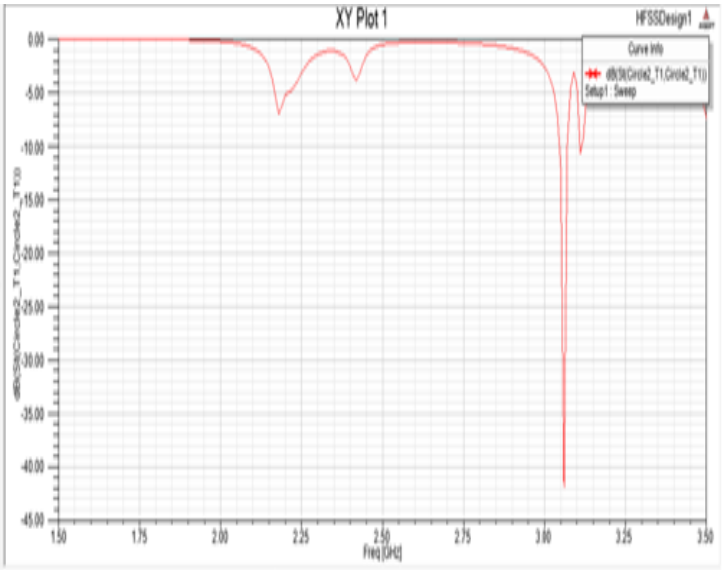

Fig.4 Return loss at two proposed frequencies (3&3.11GHz)

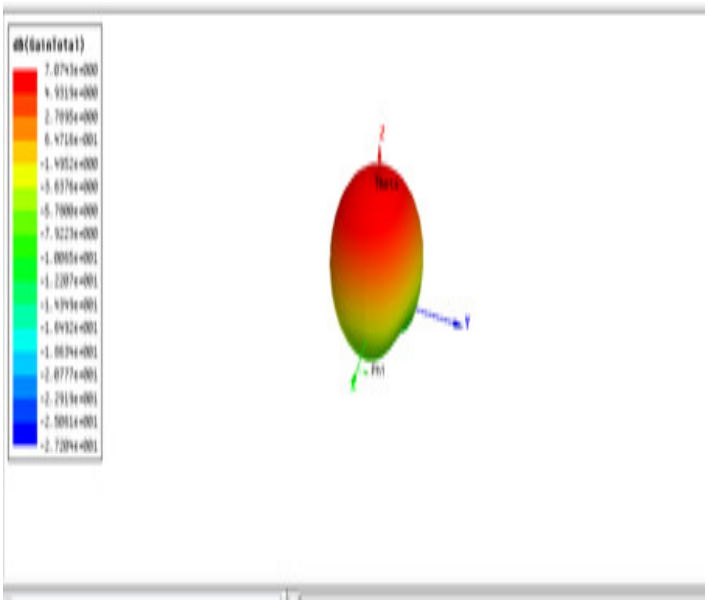

Fig.5 Gain plot of the Double swastika slot microstrip patch antenna

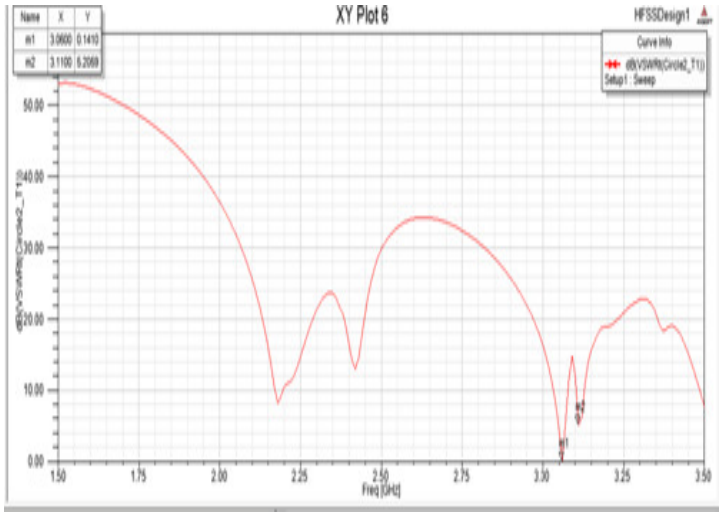

Fig.6 VSWR at two proposed frequencies (3&3.11GHz)

Above results shows that Return loss and VSWR as

At 3GHz, Return loss = -40dB

VSWR = 1

At 3.11 GHz, Return loss = -12dB

VSWR = 1.7

Hence VSWR (<2) and Return loss (<-10dB) obtained in the acceptable range.

5. CONCLUSION

A double Swastika slot patch antenna with coaxial feed line was designed and simulated here. The values of Return loss and VSWR were accomplished in the acceptable range. VSWR 1 and 1.7, Return loss -42dB and -12dB were achieved at resonant frequencies 3GHz and 3.11GHz respectively. Gain of about 7dB achieved. Slot dimensions were varied to get desired results. The proposed Antenna in this paper can be used in UWB and WiMAX Applications. Here HFSS Simulation tool has been used.

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ARDUINO BASED ABNORMAL HEART RATE DETECTION AND WIRELESS COMMUNICATION

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ABSTRACT

The heart rate is to be monitored continuously for the heart patients. This paper proposed a system that awakes to monitor the heart rate condition of the patient. This work includes two parts. 1) We developed an application to monitor the patient's heart beat and if the heart beat is abnormal, a message should be transmitted to the doctor using 3G shield. Thus, doctors could monitor the patient's heart rate condition continuously and suggests few earlier precautions to the patient. The heart rate is detected by using photoplethysmograph (PPG) technique. 2) The Arduino wireless communication is developed in such a way that it performs voice calls, sends SMS by interfacing with 3G shield using AT commands. One of the input given is a user specified number to be dial and the expected output is voice call should be successfully performed. Here the program is written in such a way that there are many options available like dynamic call, emergency call (police, ambulance, and fire), sending message, receiving call, Disconnect a call, Redial, Forward message.

KEYWORDS

PPG, 3G shield, Arduino, SMS, AT commands.

1. INTRODUCTION

Now-a-days the development and usage of the mobile systems and wireless networks became prominent. There is an enhancement in telemedicine applications and patient monitoring. To improve cost reduction, resource management, time and patient care, the mobile systems and wireless networks[10-12] will be an aid in hospital and other medical environments. The real-time information is useful for making critical decisions about the care of the patients, the demands on strength and consistency of wireless communication systems[8] can be used by medical environment. Wireless networks can be used in hospitals in order to provide network infrastructure for clerical work but not for health monitoring systems. The Instruments that are used for monitoring health conditions are not networked and are not controlled or monitored remotely [1,11]. This paper on hand a system that is developed which is able to monitor and alert's the doctors and/or patient's relatives regarding the patient's heartbeat conditions. Using processing software, a heart beat sensor circuit is designed which adopted photoplethysmograph (PPG) technique. The Signals that are detected are analyzed and processed before sent through SMS to family members and medical experts. It is advantageous in terms of cost, save time, no complicated settings, and even very useful for patient who lives alone. The developed system also perform a voice call, sending SMS using Arduino board and a 3G shield using AT commands.

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Input given to the project is user specified number to be dial and the expected output voice call should be successfully dialed. While forwarding the SMS the user specified number is dialed and the message to be sent is given and the required output is to send the message to that particular number successfully.

There is a need for wireless transmission of heart rate information to handheld devices that are used by medical practitioners. PPG techniques have been adopted in the design by the authors in [5].For developing the monitoring of cardiovascular state of the patients, the researchers [5] presented their idea of a device . It is useful for monitoring the cardiovascular state of the patients. All recorded physiological signals (ECG, PPG photopletysmograph) are stored for medical post-processing. If in case of critical values of the measured parameters occurs, they also proposed that the doctors or relatives can be informed by an automatically sent SMS. Yet, no additional results on this research are disclosed.

A practical system is developed for monitoring heartbeat which does not use the self–count pulsation of blood or ECG signal [6]. Using a 7-segment display, output of the sensor is viewed on the counter display through the numbers of beat count. For every two seconds, the reading is updated on the counter display.The main intention of system development in [7] is to build a heart rate monitor using the wireless transmission to the receiver which displays the heart rate [9] in beats per minute. The system uses the Bluetooth technology to communicate data with a terminal computer. The system's drawback is the distance between sensor and the computer should not more than 20 meters which is impractical to be implemented.

2. PROPOSED SYSTEM

The proposed system is to send the heart rate information to the doctor through SMS, if there are any abnormalities in heart rate of the patient, they will get patient's information from their mobile, and then simply, they provide treatment within short time. This paper is based on development of Arduino wireless communication system and heart rate monitoring by sending SMS to monitor the cardiac patients.

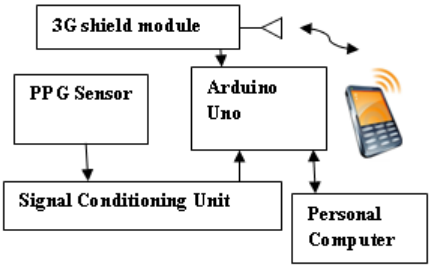

Fig. 1. Block diagram of Proposed System

The Block diagram of proposed system is shown in Fig 1. The block diagram contains PPG sensor circuit, Arduino Uno,3G shield module and personal computer .When finger is placed into the sensor, the PPG signal is generated which is filtered and amplified. Arduino reads the PPG signal continuously and transmits the data to the PC through the USB-UART interface. On PC, we develop an algorithm that reads the incoming PPG signal from the Arduino and process them to find out the heart rate[2]. The Processing software is used to plot PPG signal. An alert message

will be sent to mobile phone by 3G shield ,if there is any abnormal heart rate is detected. Then doctor will get the patient heart rate information by monitoring in his mobile.

2.1. Photoplethysmograph

PPG is a low-cost and simple optical technique that can be used for detecting blood volume changes in the microvascular bed of the tissue. Recurrently, it is used noninvasively to obtain measurements at the skin surface [3]. By using the pulse oximeter, which illuminates the skin and measure the changes in the light absorption [4] ,a PPG is obtained. Typically, to determine blood flow the PPG tool uses an emitter receiver pair. It consists of a photodiode and matched infrared emitter, which transmits the changes in infrared reflectance resulting from varying blood flow.
A photo detector and an IR LED are placed on two opposite sides and are made to face each other. When a fingertip is placed into the sensor, the IR light coming from the LED is illuminated on it[13] . The photo detector diode obtains the transmitted light through tissue on other side. Based on the tissue blood volume, more or less light is transmitted. Accordingly, the transmitted light intensity changes with pulsing of the blood with heart beat. A plot for this variation to time is referred as photoplethysmographic[7] or PPG signal.

2.2 ArduinoUno & 3 G shield

The 3G module which is connected to Arduino allows downlinks rates over 115200 bauds (~11.5KBps). Fig.2. shows the interfacing of Arduino Uno & 3G shield.

Fig. 2. Arduino interfaced with 3G shield.

The first thing that we are going to do with the system is to connect the module to a PC directly (using an Arduino as gateway) and refer the basic AT commands. In this case, serial communication jumpers have to be set on USB gateway position. Then connect the SIM card and the USB cable. Finally plug the USB cable to the computer and open a serial port terminal to communicate via USB port (e.g: hyperterminal (win), cutecom / gtkterm (linux)).Set the baud rate to 115200 bps and open the serial port, then press the ON button for two seconds. Then, if we type AT we'll get OK, it means that the communication with the module is working fine. Now, with the module working you can check some AT commands to control the module.

3. RESULTS AND DISCUSSIONS

Arduino wireless communication is established by using Sketch, generally programme written in arduino software is dumped into the Arduino board via USB serial communication and made to run.The output is displayed on the serial monitor. The programme displays 8 different options to

the user. According to the necessity, the user can enter a choice and the corresponding task is done. The different options are:

1. Emergency call
2. Make a call
3. Send SMS
4. Receive a call
5. Disconnect a call
6. Redial
7. Forward
8. Know your heart beat
9. Exit

The Flowchart of developed system is shown in Fig.3.

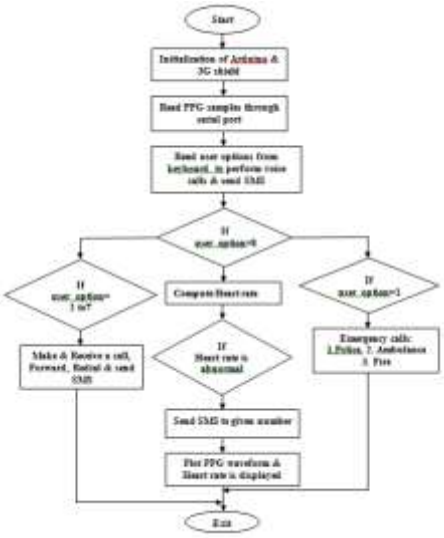

Fig. 3. Flowchart of developed system.

1. Emergency Call:

When choice 1 is entered, it corresponds to emergency call. A call is automatically dialled to a particular number. The number is already in the programmed.

Again in this, we have 3 options:

1. Police
2. Ambulance
3. Fire

By entering suitable choice, the number is successfully dialled.

2. Make a Call:

Here the number to which we are intended to call is to be dialled in the serial monitor. The present work has a facility of dialling calls of more than 10 digits (i.e., we can call to other countries even).

3. Send SMS:

By entering choice 3, we choose the option of sending SMS. Here the number to which the message should be entered and also the message.

4. Receive a Call:

We can receive the incoming calls by entering this choice provided that the speaker beeps.

5. Disconnect a Call:

A call can be disconnected by entering this choice at any time.

6. Redial:

A facility for the purpose of calling to the last dialled number is given. If you enter the choice 6 for your first call, automatically message is displayed.

7. Forwarding the last message:

The last sent message is forwarded by entering this choice. If you enter choice 7 and it is your first message, then message is displayed on the serial monitor.

8. Know your heart beat:

Place the finger in the holder and get the heart beat. Run the processing software to show the PPG Waveform

9. Exit:

This option makes to exit out of the programme.

Fig.4. shows the Arduino programming and serial window for selecting the option by the user.

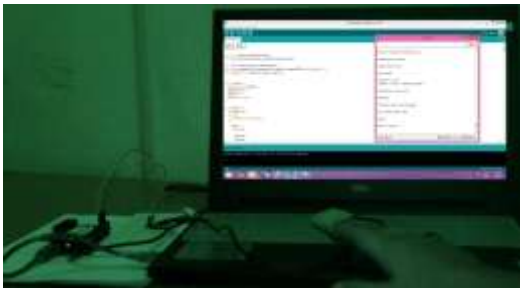

Fig.4. Complete setup of the proposed system

A basic circuit to display the PPG waveform, detect the abnormalities in it and emergency calling if it senses the abnormalities is built using Arduino. In this application heart rate is calculated using PPG sensor and Arduino uno.

Fig. 5. Developed system with PPG waveform.

Fig.5. shows the continuously varying PPG waveform. Based on the number of heart beats per minute message will be sent to doctor. Message is sent by interfacing Arduino Uno with 3G shield. If the heart rate is abnormal, message will be automatically sent to the doctor. Fig.6. shows the heart rate display on the serial window.

Fig.6. Developed system with heart rate.

CONCLUSIONS

This paper presents a development in Arduino wireless communication and heart rate monitoring system based on SMS for biomedical applications. This system is developed by integration of both hardware and software components. The developed system is to perform voice calls, send SMS by interfacing with 3G shield using AT commands. One of the input given is a user specified number to be dial and the expected output is voice call should be successfully performed. We developed an application to monitor the patient heart beat and if the heart beat is abnormal, a message should be transmitted to the doctor using 3G shield.

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DESIGN AND FABRICATION OF S-BAND MIC POWER AMPLIFIER

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ABSTRACT

In this paper, we demonstrate an approach to design FET (pHEMT) based amplifier. The FET is from Berex Inc.The design is carried out using the measured S-parameter data of the FET.ADS is used as design tool for the design. A single-stage power amplifier demonstrated 13dB output gain from 3GHz-4GHz .The saturated output power of 1W and the power added efficiency (PAE) up to 43%.The amplifier is fabricated on a selective device GaAs power pHEMT process in MIC (Microwave Integrated Circuit) Technology. MICs are realized using one or more different forms of transmission lines, all characterized by their ability to be printed on a dielectric substrate.Active and passive components such as transistors/FET, thin or thick film chip capacitors and resistors are attached.

KEYWORDS

pHEMT, MIC, Power Amplifier

1. INTRODUCTION

Power amplifiers (PAs) are the most energy-consuming component in wireless transceivers. PAs represent more than 60% of consumed energy in the overall communication system. The trends show that the next generations of wireless communication system will require broadband, High Power Added Efficiency PA allowing reliability capabilities.

Microwave Integrated Circuit (MIC) technologies have made a great advance in various aspects. No area of the field has seen greater changes than that of microwave amplifiers and oscillators. The active devices used in amplifiers and oscillators have evolved from vacuum tubes (klystrons and magnetrons) to two terminal solid state devices (Gunn, IMPATT, Tunnel and Varactor diodes) and finally to three terminal solid state devices (GaAs FETs, and silicon bipolar transistors). At the same time, the transmission line media has changed from waveguides, to coaxial cable and finally to micro strip lines. GaAs devices address high power and high

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efficiency performances. The main future challenge is to design PA with high power characteristics associated with the highest bandwidth and the smallest size as possible.

S-parameters are important in microwave design because they are easier to measure and work with at high frequencies than other kinds of parameters.They are conceptually simple, analytically convenient, and capable of providing a great insight into a measurement or design problem.A network analyzer is an instrument that measures the network parameters of electrical networks. Today, network analyzers commonly measure S- parameters because reflection and transmission of electrical networks are easy to measure at high frequencies.

2. pHEMT DEVICE

The characteristics of our pHEMT devices make them ideal choices for usage as high efficiency, linear power amplifiers with variable output capabilities. The high gain at low drain currents and the sham pinch off *I* large-drain voltages enable the devices to operate very efficiently over very large portion of their I-V characteristics. Our amplifiers maintain their linearity,bandwidth and high efficiency when their drainvoltages are reduced to as low a value as 2V. This is accomplished without retuning the amplifiers at eachdrain voltage - the amplifiers are fixed tuned. Amplifiers with comparable performance have not beenpreviously demonstrated with any solid state devices.

The pHEMT device used is BCP120T**.** BCP120T is a GaAs Power pHEMT with a nominal 0.25 micron gate length and 1200 micron gate width making the product ideally suited for amplifier applications where high-gain and medium power from DC to 26 GHz. The product may be used in either wideband or narrow-band applications. The BCP120T is produced using state of the art metallization with SI3N4 passivation and is screened to assure reliability.

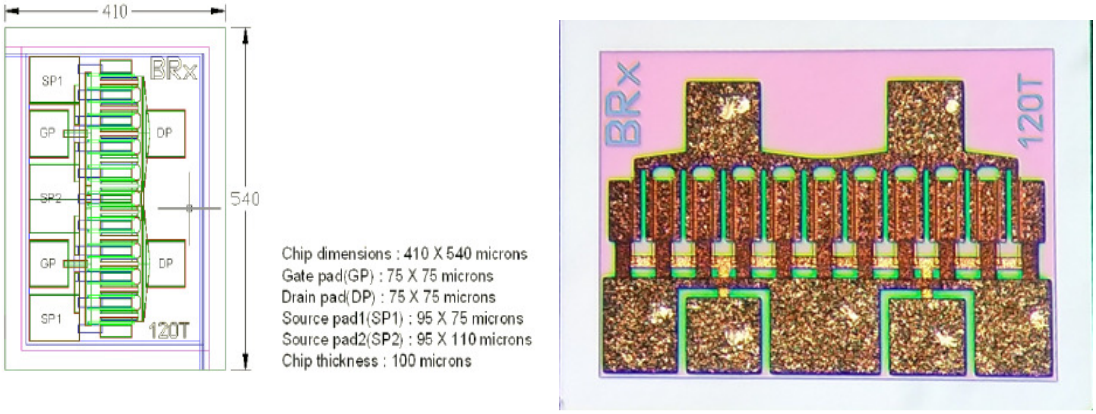


Fig1. pHEMT

At 25 C, The continuous values can be as Drain-Source Voltage Vds 8 V ,Gate-Source Voltage Vgs -3 V ,Drain Current Ids =Idss ,Forward Gate Current Igsf 10 mA ,Input Power Pin @ 3dB compression. The electrical characteristics for calculating the output power the specifications

given as Output Power P1dB is 31.0dBm @ P1dB (Vds = 8V, Ids = 50% Idss) , Gain is 11.0dBm @ P1dB (Vds = 8V, Ids = 50% Idss) PAE is 40% @ P1dB (Vds = 8V, Ids = 50% Idss).

3. AMPLIFIER DESIGN

The design of any practical amplifier is a multistep process. The design procedure leading to the simulation of an ideal circuit is Define a specification, Choose a topology, Choose an active device, Stabilize the device, Choose a bias circuit, Address power or noise matching conditions, Perform computer simulations and optimizations to realize the specifications. Tool used: ADS Tool is used to design the power amplifier circuit design. Advanced Design System (ADS) is an electronic design automation software system. It provides an integrated design environment to designers of RF electronic products such as mobile phones, pagers, wireless networks, satellite communications, radar systems, and high-speed data links. This chapter describes the windows, menus and basic operations or working in the ADS Design Environment performs the operations: Creating projects to organize and save your designs. Creating system diagrams, circuit schematics and EM structures. Placing circuit elements into schematics. Placing system blocks into system diagrams. Incorporating and tuning sub circuits into system diagrams and schematics. Running simulations for schematics and system diagrams, displaying output graphs, creating layouts. S-parameters for two port networks, at microwave frequencies, the parameters used for measurement have inputs and outputs expressed in power. These microwave parameters are called S-parameters. S-parameters are transmission and reflection coefficients between the incident and reflected waves. The transmission coefficients are commonly called gains or attenuation, and the reflection coefficients are directly related to VSWRs and impedances. Each parameter is typically characterized by magnitude, decibel and phase. The expression in decibel is 20 log S_{ij} because S-parameters are voltage ratios of the waves.

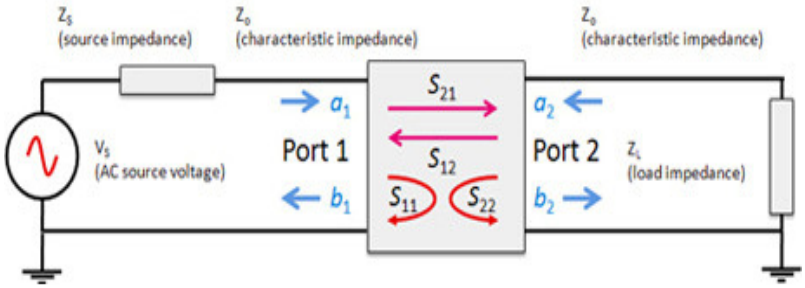
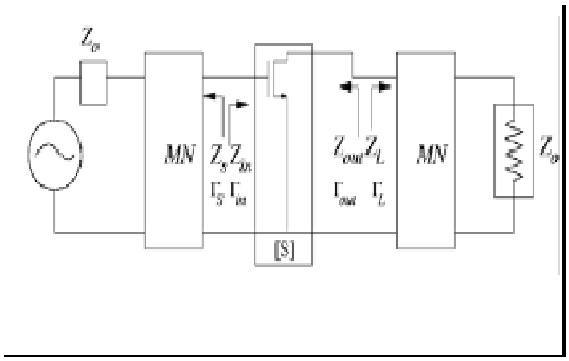


Fig 2.Block diagram of S-Parameters



$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Fig 3.Matching Network

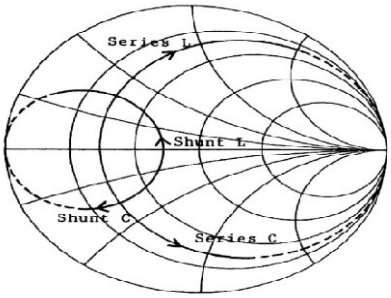


Fig 4.Smith chart

Impedance Matching Using Smith Chart: Matching a transmission line simply means terminating the line in its characteristic impedance so that the standing wave ratio of unity transmits a given power without any reflection. Also, transmission efficiency is optimum where there is no reflected power. Matching can be tried first on the load side to flatten the line, then adjustment may be made on the source side to provide maximum power transfer.

4. CIRCUIT DESIGN

Input and output matching networks are released by necessary theoretical calculations.Transmission lines are used to design the circuit.Signals at high frequencies are usually sinusoidal or can be analyzed as though they are composed of sinusoidal waves that are propagating through a component from input to output. Moreover, any signal waveform can be represented in terms of sinusoidal components using Fourier analysis. Considering all signals to be sinusoidal makes the solution of partial differential equations (3.1) and (3.2) in time domain much easier. Hence, it is appropriate to analyze transmission line equations in steady-state sinusoidal form. Both the voltage and current will be in phasor form and will vary in time and distance. Let V and I be the voltage and current phasors, respectively, at any arbitrary point on the transmission line.

The derivatives of the voltage and current phasors from the above equations can be expressed as:

$$-\frac{dV}{dz} = RI + L\frac{dI}{dt} \quad (1)$$

$$-\frac{dI}{dz} = GV + C\frac{dV}{dt} \quad (2)$$

A generalized solution of the coupled differential equations (1) and (2) can be given by,

$$V(z,t) = (V^{+}e^{-\gamma z} + V^{-}e^{+\gamma z})e^{j\omega t} \quad (3)$$

$$I(z,t) = (I^{+}e^{-\gamma z} + \Gamma e^{+\gamma z})e^{j\omega t} \quad (4)$$

where $\gamma = \alpha + j\beta$ is the propagation constant

V^{+}, I^{+} = complex voltage and current amplitudes in the positive z direction
V^{-}, Γ = complex voltage and current amplitudes in the negative z direction
α = attenuation constant per unit length of the line
β = phase constant per unit length of the line

Substituting equations (3) and (4) into (1) and (2) gives

$$\frac{dV}{dz} = -(R + j\omega L)I = -Z.I \quad (5)$$

$$\frac{dI}{dz} = -(G + j\omega C)V = -Y.V \quad (6)$$

where Z = impedance phasor per unit length of the transmission line

Y = susceptance phasor per unit length of the transmission line

Transmission line parameters are considered for the design as Propagation constant (γ), Phase velocity (v_p), Characteristic impedance (Z_0), Reflection coefficient (Γ), Voltage standing wave ratio(VSWR),

$$\gamma = \alpha + j\beta = [(R + j\omega L)(G + j\omega C)]^{1/2} \quad (7)$$

$$v_p = \omega/\beta \quad (8)$$

$$Z0 = (Z/Y)^{1/2} = [(R+j\omega L)/(G+j\omega C)]^{1/2} \quad (9)$$

$$\Gamma = E_r / E_i = (V^{-}e^{\gamma l}/V^{+}e^{-\gamma l})$$

$$VSWR = |V_{max} / V_{min}| = (1+\Gamma) / (1-\Gamma) \quad (10)$$

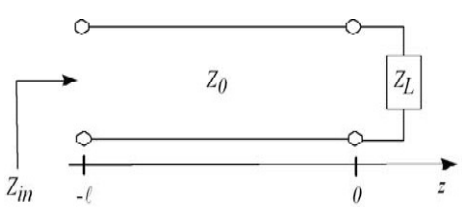


Fig 5. Transmission line terminated load impedance

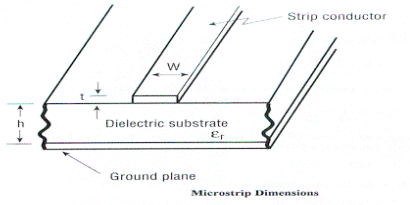


Fig 6. Microstrip

Micro strip parameters considered are $v_p = c/(\varepsilon_{eff})^{1/2}$

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(8\frac{h}{W} + \frac{W}{4h}\right)$$

$$\text{where } \varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{W}\right)^{-1/2} + 0.04\left(1 - \frac{W}{h}\right)^2\right] \text{ for } \frac{W}{h} \le 1$$

or

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W}{h} + 1.393 + 0.667\ln\left(\frac{W}{h} + 1.444\right)\right]}$$

$$\text{where } \varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-1/2} \text{ for } \frac{W}{h} \ge 1$$

Stability considerations are one of the important aspects for the design of the circuit. So ,In terms of k factor, the stability criteria are, unconditional stability, k > 1.0.conditional stability, k < 1.0

$$k = \frac{(1 - |S11|^2 - |S22|^2 + |D|^2)}{2|S12||S21|}$$

where S_{11},S_{22}, S_{12},S_{21} are the complex S-parameters and $D=S_{11}S_{22} - S_{12}S_{21}$.

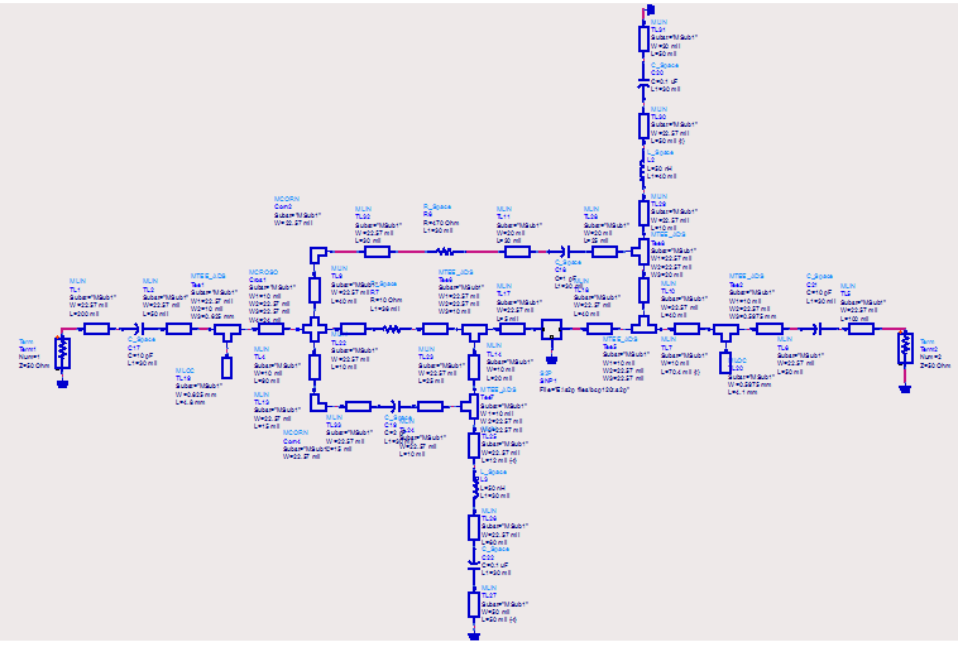


Fig 7. Schematic of power amplifier

Fig 7 is the schematic diagram of power amplifier attained from the ADS tool software after designing the circuit by considering the input and output matching network.Fig 8 is the layout resulted from the fig 7.

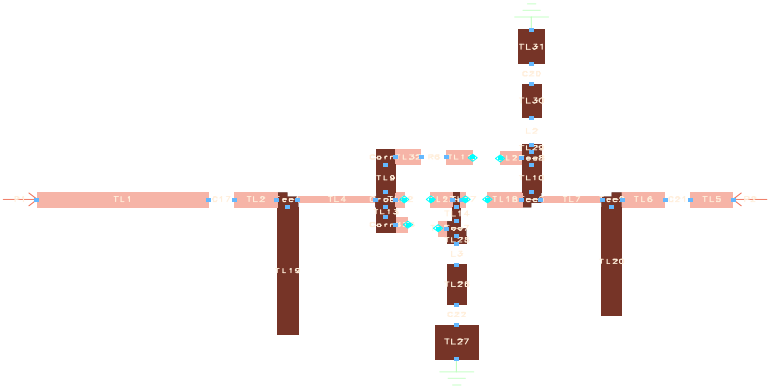


Fig 8. Layout of power amplifier

5. FABRICATION:

On the RT duroid material the blue print of the circuit distributed components is done and given for the circuit assembly. Assembly deals with placing the component on the fabricated circuit.

The components can be attached by using epoxy /eutectic bonding, soldering. Any Interconnection between the transistor chip and the components can be provided by wire bonds. The IC fabrication flow using the transistor chip and lumped elements such as a chip capacitor and coil inductor.

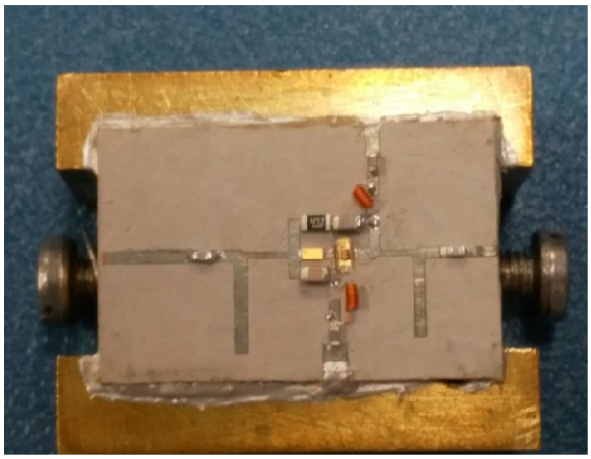


Fig 9. MIC fabricated power amplifier

6. AMPLIFIER PERFORMANCE

After testing the fabricated device in the network analyzer,the final transmission and reflection coefficients results are given below.The return losses are above -18dB.The output power resulted is 30dBm.

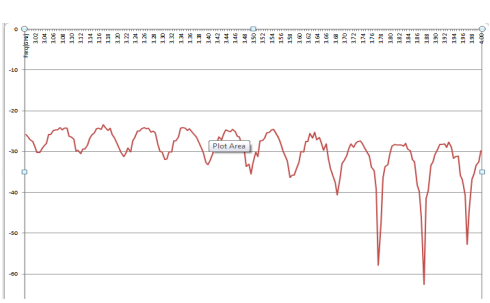


Fig 10. s22

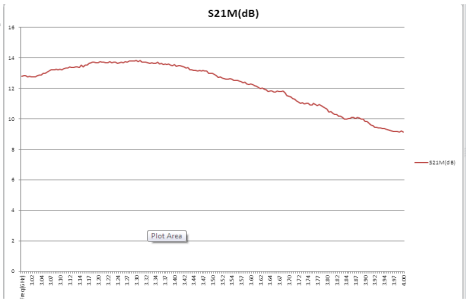


Fig 11. s21

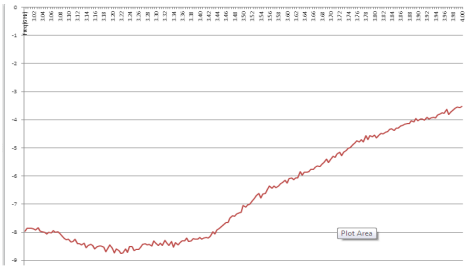


Fig 12. s11

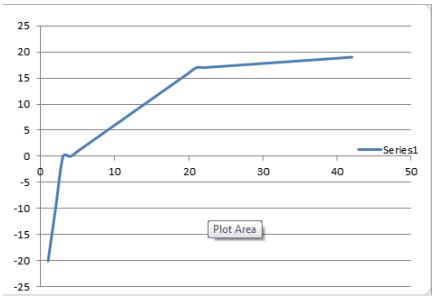


Fig 13. Output power

The final simulation results attained for the circuit shown in fig 7 are given in Fig 14.

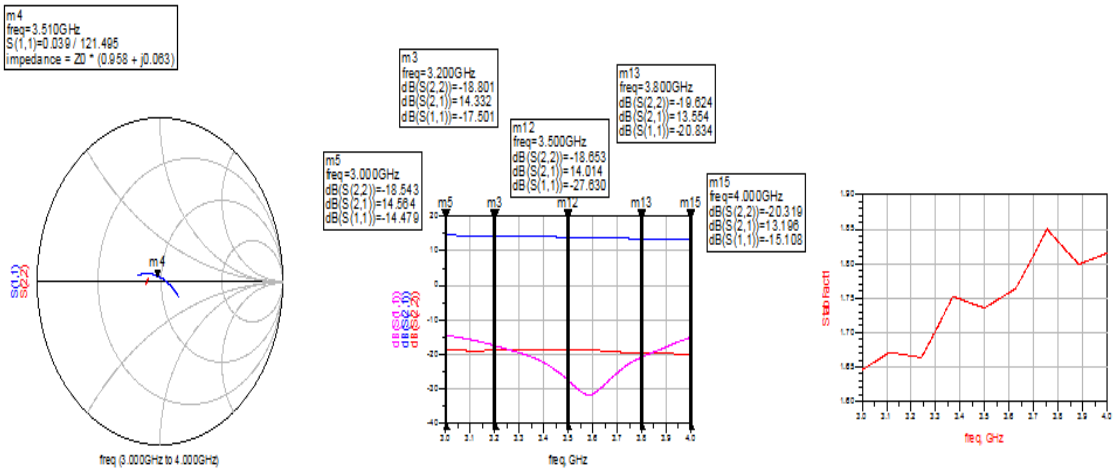


Fig14. Simulation results

7.CONCLUSION:

This paper presents the design of a Microwave Power amplifier with below mentioned specifications.Frequency range = 3GHz-4GHz,Band width = 1GHz, Gain = Minimum 13dB, Flatness = $\pm$0.7dB,Input Return losses better than -10dB,Output Return losses better than -30Db,Power output = 30dBm,P1dB=30dBm,PAE= 43%.

The layout is generated from the designed circuit schematic using ADS, which is then printed on the RT duriod substrate using a Miller machine. All the components are assembled to realize the final circuit. Therefore the designing and fabrication of the MIC power amplifier is complete.

ACKNOWLEDGEMENTS

The author would like to acknowledge SANGAM BALKE ,HOD of ATQC of GAETEC, Hyderabad for his constant mentoring during the complete course of the work.

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PROTOTYPING OF WIRELESS SENSOR NETWORK FOR PRECISION AGRICULTURE

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ABSTRACT

Now-a-days the climatic conditions are not same and predictable. More over the wireless sensor network [1] carved path in many applications. There are many manual methods to cultivate a healthy crop which involves a lot of manpower. Hence there is a need to design a system for precision agriculture. Precision agriculture means giving the correct input to the crops at the right time. This paper explains how the real input is given to the crops according to the environment change [2]. This system design uses Arduino Uno .The values which are measured by the sensors are transmitted to a centralized device which is Zigbee (coordinator). After the values received by the Zigbee, according to those values precise decision will be taken by the experts.

KEYWORDS

Arduino, Zigbee, Wireless Sensor Network, Xbee, Precision agriculture.

1. INTRODUCTION

Now-a-days cultivating crops are becoming a very hectic task for the farmers because of the unpredictable climate and expense cost of the seeds. Due to the unpredictable and sudden change of the climate the damage ratio will be high and even the loss rate will be high. The solution for this problem is to adopt the techniques of precision agriculture. Precision Agriculture [9] is a process of giving a correct set of inputs to the crops or lands according to the environment changes. Precision Agriculture follows a defined set of rules. They are collecting the data , processing the data , sending the data to the centralized machine and according to the data received, the decisions will be taken by the expert.

The protection of the crops is very essential. So there is a need for monitoring of the data and that data should be real. In order to provide instant solution to the crops the data should be collected in a smart way. To achieve smartness we have to adopt wireless communication techniques.

In telecommunication and computer science, wireless sensor networks are the active area of research. It plays a major role in many areas of research. Applications are health care monitoring, Area monitoring, quality management, Air pollution monitoring, Nature disaster prevention, data logging etc. In the present work the design consists of a processor board, a group of sensor and a transceiver.

The main object of this paper is to provide quality crop cultivation procedure in a predefined standard i.e. using ZigBee technology [8]. In a network nearly 65500 devices can be connected and synchronized for the monitoring. A network contains many nodes and each node will be deployed in a specified and predefined places. In this several nodes, one node acts as the coordinator that is connected to the centralized machine. Each node consists of a processor i.e. Arduino, sensors to measure the following parameters soil moisture, humidity, temperature, light intensity and a ZigBee which acts as the end device. In order the data has to be routed to many places and reach the destination, in between many router ZigBee are connected in order to complete the network without any packet transmission errors.

1.1 Motivation

The present scenario where the farmers are facing problem is with the input for the crop. If the input like water level, light intensity level to which the plant has to be exposed etc. these are some parameters which should be examined at starting level itself. If parameters are maintained properly the yield will be more. So to provide correct input to the crop and to increase the yield here we are designing a system which is real.

1.3 Domain

Here if we use wired communication, the system becomes complex and sometimes to send data delays may occur and if any damages occurs to the wire the communication struts. To avoid these errors in our system we are adopting wireless communication which is reliable and flexible.

2. OVERVIEW OF ZIGBEE TECHNOLOGY

ZigBee is an IEEE based standard for wireless communication. The difference between the ZigBee and 802.15.4, 802.15.4 has only Mac and physical layer but layer above that is present in the ZigBee which makes the communication very effective. As it has additional layers when compared to 802.15.4 it supports the mesh network topology which is very effective to construct a network. In order to complete a network it needs a coordinator, router and an end device. Each device has its own address and PAN ID (permanent area network identification). The PAN ID of the devices in a network should be same.

Coordinator collects the data from all the nodes and saves in a database. It assigns the PAN ID. Router collects the data from the nodes, it helps the network to grow and it also routes the data in the network. This joins the PAN ID before it transmits the data. End device it collects the data from the processor board. Coordinator can communicate with any Zigbee device in a network. The end device can't communicate directly with another end device [3].

The Xbee modules can be configured in both AT and API modes. Here in order to form a network, API mode is used for both point-to-point and mesh network communication .

API FRAME: The communication between the two Xbee are done in a structured way, where it has to follow the same format throughout the network.

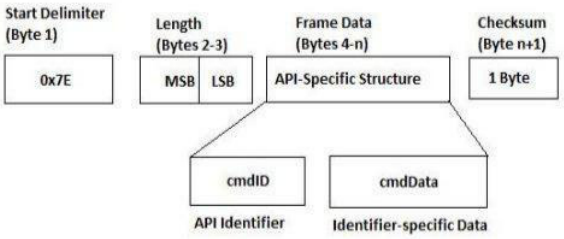

Fig 1. Frame format.

3. DESIGN IMPLEMENTATION

To design a wireless sensor network (WSN), the components required are a processor board, sensors and transceiver, which are explained below.

Sensor unit: The parameters which are going to measure here in this work are Soil moisture, temperature, humidity and light intensity [4]. The soil moisture is measured because some crops require lot of water flow and some plants doesn't require water flow. To maintain the water present in the soil the moisture sensor is used. The light intensity is measured because some plants don't require lot of sunlight and some require more. So by evaluating all the requirements for the crop cultivation it is clear that if we have these sensors it's enough for monitoring. If the plant requires pH monitoring then we can also go for pH sensor also. *Microcontroller Unit*: Here in this work an Arduino Uno is used. It consists of Atmel AVR microcontroller. As Arduino has standard connections i.e. that can be connected to the CPU directly the ease of programming is high. It has 14 digital I/O pins, 6 Analog inputs, a 16 MHz quartz crystal, a USB connection, a power jack, an ICSP header and a reset button. Its operating voltage is 5V. The data from the sensors are captured and processed by the Arduino and it is kept in the data frame of the X Bee (API) [5].

Transceiver: To generate communication between two nodes here X Bee PRO is used [8]. This is the PRO Series 2 ZigBee protocol 63mW with wire antenna. It supports point-to-point, mesh networks and multi networks. It has Indoor/Urban range up to 300 ft (90 m). Dimensions are 24mm x 33mm x 9mm (0.94in x 1.3in x 0.3in)[6].

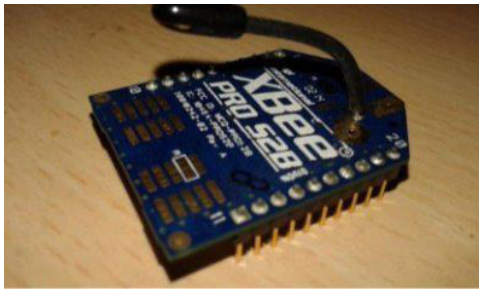

Fig 2. X Bee Module

The data from the sensor are transmitted to the destination using this ZigBee end devices, routers and reaches to the coordinator where the coordinator transmits the data to the centralized centre. The block diagram of a node is represented in fig 3 and the receiving end i.e. coordinator block diagram is represented in the Figure 4

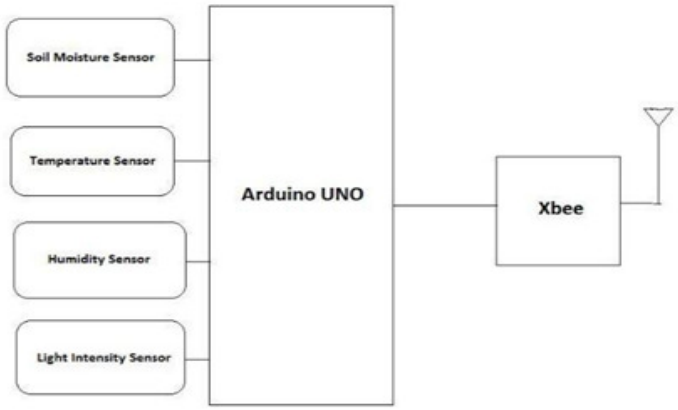

Fig 3. Wireless sensor network (end device)

Fig. 4: Receiver Section.

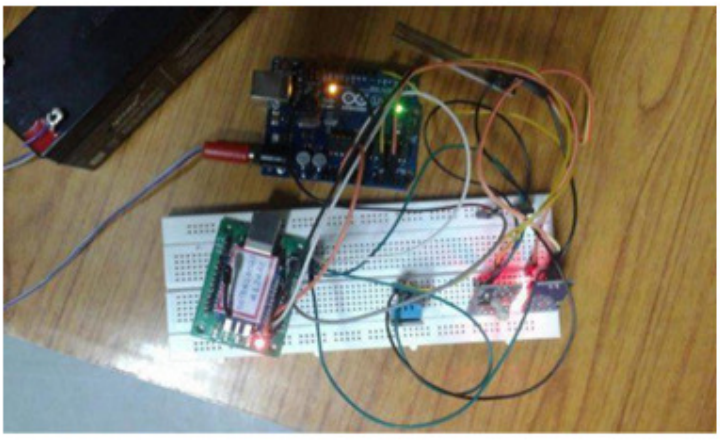

Fig. 5: Total set up of a node.

4. RESULTS

A reliable wireless sensor network is implemented. The output of the total setup designed can be observed in the computer to which the coordinator (receiver X Bee module) is connected. The output values of each sensor are displayed in the computer which is represented in the figure 6.

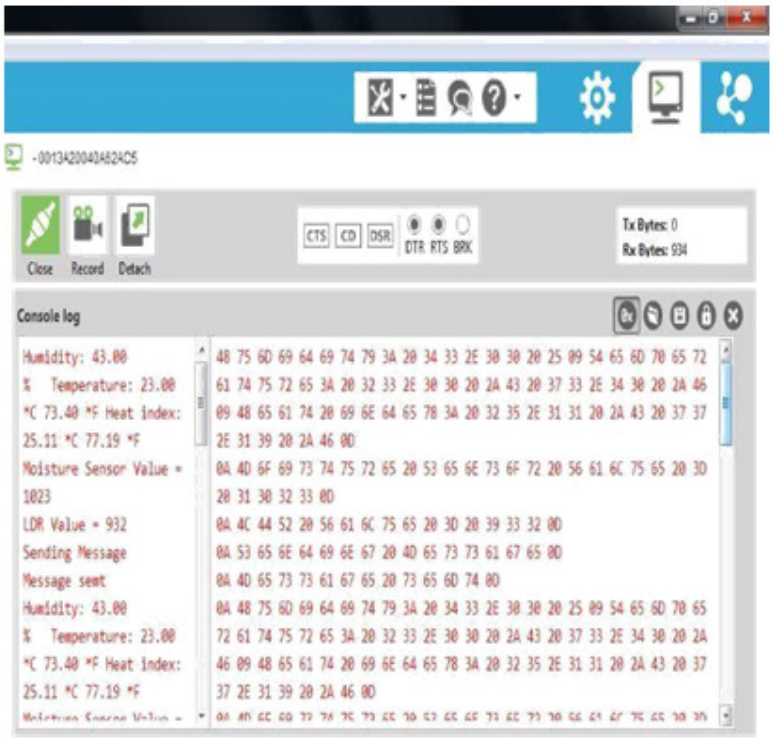

Fig. 6: The output of the work seen at the coordinator level.

Table 1: The values of the sensors

Sl no	Humidity	Temperature	Moisture	Light intensity
1	43.00	23.00	1023	932
2	57	30.00	523	995

5. FUTURE SCOPE

In this work, only one wireless sensor network is designed and implemented. For Precision agriculture, sensor values should be continuously tracked in a predefined time instances. The nodes should be kept in a predefined place. Those nodes should be synchronized and communicated properly in order to get effective results. If the crop needs pH [7] value then pH sensor should be added to the sensor node. The performance of the network depends on the performance of the node so the node should be arranged in an effective way where the nodes power consumption should be less [11].

6. ACKNOWLEDGMENT

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A COMPREHENSIVE STUDY ON BIG DATA APPLICATIONS AND CHALLENGES

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ABSTRACT

Big Data has gained much interest from the academia and the IT industry. In the digital and computing world, information is generated and collected at a rate that quickly exceeds the boundary range. As information is transferred and shared at light speed on optic fiber and wireless networks, the volume of data and the speed of market growth increase. Conversely, the fast growth rate of such large data generates copious challenges, such as the rapid growth of data, transfer speed, diverse data, and security. Even so, Big Data is still in its early stage, and the domain has not been reviewed in general. Hence, this study expansively surveys and classifies an assortment of attributes of Big Data, including its nature, definitions, rapid growth rate, volume, management, analysis, and security. This study also proposes a data life cycle that uses the technologies and terminologies of Big Data. Map/Reduce is a programming model for efficient distributed computing. It works well with semi-structured and unstructured data. A simple model but good for a lot of applications like Log processing and Web index building.

KEYWORDS

Big Data, HBase, Hadoop, MapReduce, Heterogeneity

1. INTRODUCTION

Big Data is proficient for business application and is rapidly escalating as a segment of IT industry. It has generated significant interest in various fields including the manufacture of health care machines, Banking transactions, Social media, Satellite imaging. Traditionally data is stored in a highly structured format to maximize its informational contents. Conversely, current data volumes are driven by both unstructured and semi structured data. Billions of individuals are various mobile devices and as a result of this technological revolution.

These people are generating tremendous amounts of data through the increased use of such devices. Particularly remote sensors continuously produce much heterogeneous data that are either structured or unstructured. This data also is termed as Big Data. Big Data is characterized by 3 aspects namely; (a) Numerous data (b) Categorization of data cannot be done in regular relational data bases (c) Processing of data can be generated and captured quickly. Consequently end to end processing can be obstructed by the translation between structured data in relational systems of DBMS and unstructured data for analytics. Big Data is a compilation of very huge

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data sets with a great diversity of types so that it becomes complicated to process by using state of the art data processing approaches.

In general a data set can be called a big data if it is formidable to perform capture, visualization, analysis at current technologies. The Essential characteristics of Big Data are followed with five V's namely, Variety, Velocity, Volume, Virality, viscosity. Volume is described as the relative size of the data to the processing capability. Viscosity measures the resistance to flow in the volume of data. Here the resistance may come from different data sources. Virality is described as faster distribution of information across B2B networks (Business to Business).Variety depicts the spread of data types from machine to machine and adds new data types to traditional transactional data. Velocity is described as a frequency at which the data is generated, Shared and captured.

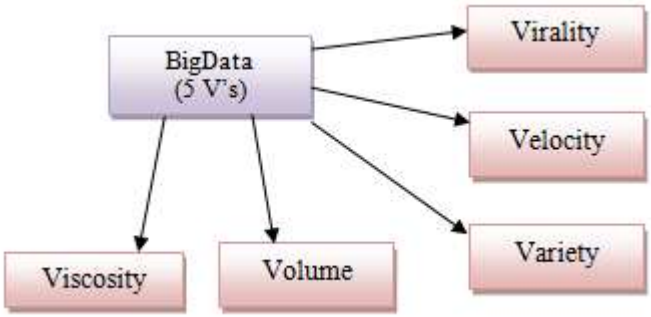

Fig 1: Essential characteristics of Big Data

2. BIG DATA ARCHITECTURE

The architecture of Big Data must be coordinated with the support infrastructure of the organization. Today, all of the data used by organizations are stagnant. Data is increasingly sourced from various fields that are disorganized and messy, such as information from machines or sensors and large sources of public and private data. Big Data technology improves performance, assists innovation in the products and services of business models, and provide decision making support. Big Data technology aim to lessen hardware and processing costs and to substantiate the value of Big Data before committing significant company resources. Properly managed Big Data are accessible, reliable, secure, and manageable. Hence, Big Data applications can be applied in various complex scientific disciplines (either single or interdisciplinary), including atmospheric science, astronomy, medicine, biology, genomics, and biogeochemistry.

2.1 Hadoop Ecosystem:

Hadoop is tranquil of HBase, HCatalog, Pig, Hive, Oozie, Zookeeper, and Kafka; however, the most common components and well-known paradigms are Hadoop Distributed File System (HDFS) and Map Reduce for Big Data. HDFS. This paradigm is applied when the amount of data is excessively much for a single machine. HBase is a management system that is open-source, versioned, and distributed based on the Big Table of Google. Zookeeper maintains, configures, and names large amounts of data. HCatalog manages HDFS. It stores metadata and generates tables for large amounts of data. Hive structures warehouses in HDFS and other input sources,

such as Amazon S3. The Pig framework generates a high-level scripting language (Pig Latin) and operates a run-time platform that enables users to execute Map Reduce on Hadoop. Mahout is a library for machine-learning and datamining. Oozie. In the Hadoop system, Oozie coordinates, executes and manages job flow. Avro serializes data, conducts remote procedure calls, and passes data from one program or language to another. Chukwa is a framework for data collection and analysis that is related to Map Reduce and HDFS. Flume is particularly used to aggregate and transfer large amounts of data (i.e., log data) in and out of Hadoop.

2.2 Hadoop Usage:

Explicitly used by

(1) Searching Yahoo, Amazon, Zvents
(2) Log processing Facebook, Yahoo,ContexWeb.Joost, Last.fm
(3) Analysis of videos and images New York Times, Eyelike
(4) Data warehouse Facebook, AOL
(5) Recommendation systems Facebook

2.3 System Architectures of Map Reduce and HDFS:

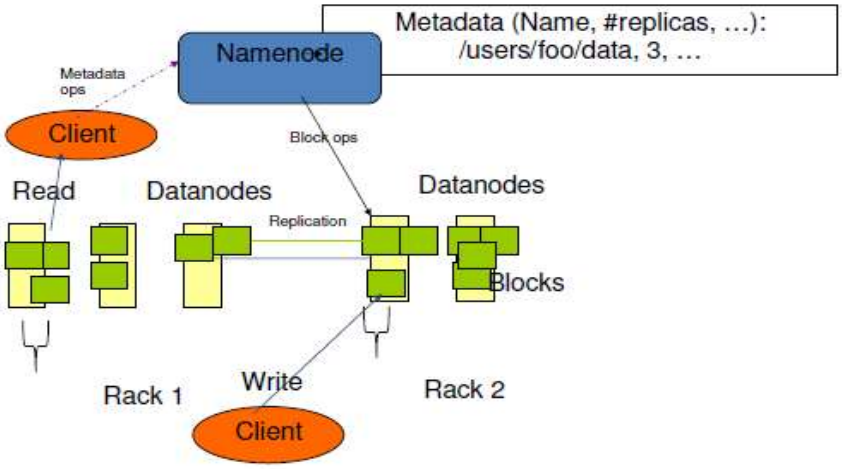

Fig 2: HDFS Architecture

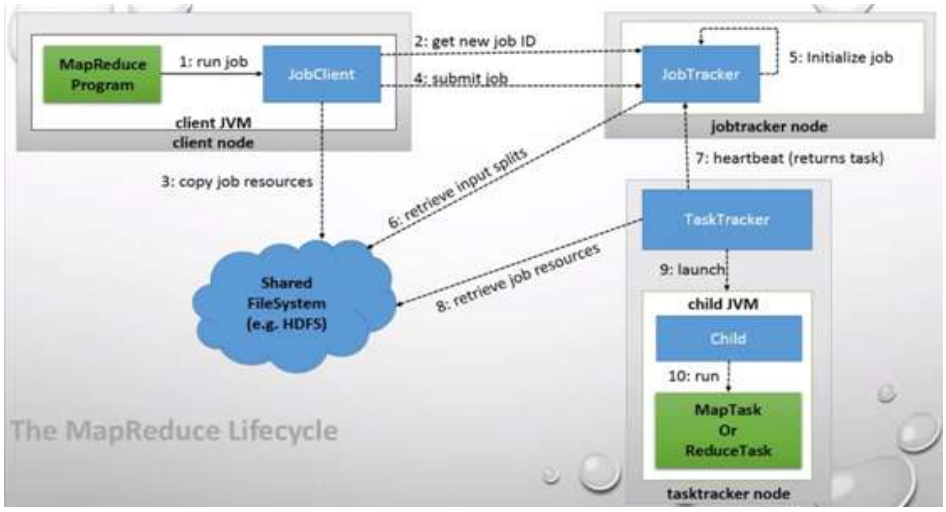

Fig 3: Map Reduce Life Cycle

Map Reduce is the hub of Hadoop and is a programming paradigm that enables mass scalability across numerous servers in a Hadoop cluster. In this cluster, each server encompasses a set of internal disk drives that are inexpensive. To improve performance, Map Reduce allocate workloads to the servers in which the processed data are stored. Data processing is scheduled based on the cluster nodes. A node may be consigned to a task that necessitates data foreign to that node.

2.3.1 MapReduce tasks:

(1) Input
- (i) Data are loaded into HDFS in blocks and dispersed to data nodes
- (ii) Blocks are replicated in case of failures
- (iii) The name node tracks the blocks and data nodes

(2) Job Submits the job and its details to the JobTracker

(3) Job initialization
- (i)The Job Tracker interacts with the TaskTracker on each data node
- (ii) All tasks are scheduled

(4) Mapping
- (i)The Mapper processes the data blocks
- (ii) Key value pairs are listed

(5) Sorting

The Mapper sorts the list of key value pairs

(6) Shuffling

(i)The mapped output is conveyed to the Reducers
(ii) Values are rearranged in a sorted format

(7) Reduction Reducers merge the list of key value pairs to generate the final result

(8) Result
(i) Values are stored in HDFS
(ii) Results are replicated permitting to the configuration
(iii) Clients read the results from the HDFS

Map Reduce essentially communicate to two distinct jobs performed by Hadoop programs. The first is the map job, which involves procurement of a dataset and transforming it into another dataset. In these datasets, individual components are reviewed into tuples (key/value pairs). The reduction task receives inputs from map outputs and further divides the data tuples into small sets of tuples. Redundant data are stored in multiple areas across the cluster. The programming model tenacities failures inevitably by running portions of the program on a choice of servers in the cluster. Data can be distributed across a very large cluster of commodity components along with associated programming given the redundancy of data. This redundancy also endures faults and facilitates the Hadoop cluster to repair itself if the component of commodity hardware fails, especially given large amount of data. With this process, Hadoop can delegate workloads related to Big Data problems across large clusters of reasonable machines. The Map Reduce framework is convoluted, predominantly when complex transformational logic must be leveraged. Attempts have been generated by open source modules to simplify this framework, but these modules also use registered languages.

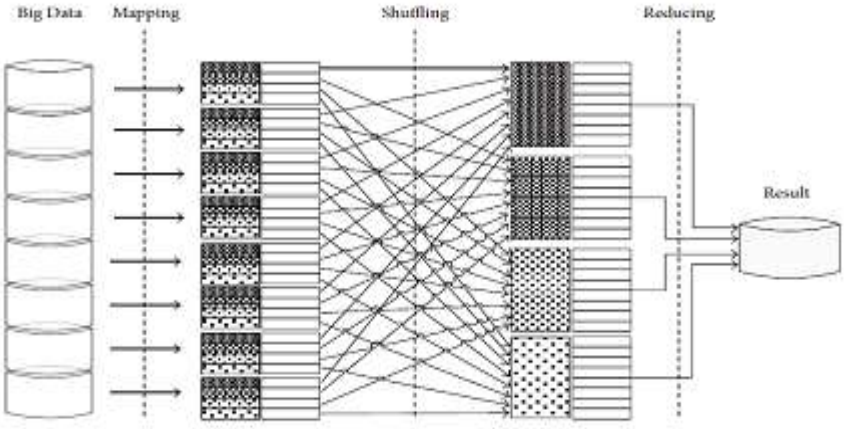

Fig 4: Map Reduce Architecture

2.3.2 Process flow

Record reader→Map→Combiner→Partitioner→Shuffle and sort→Reduce→Output format

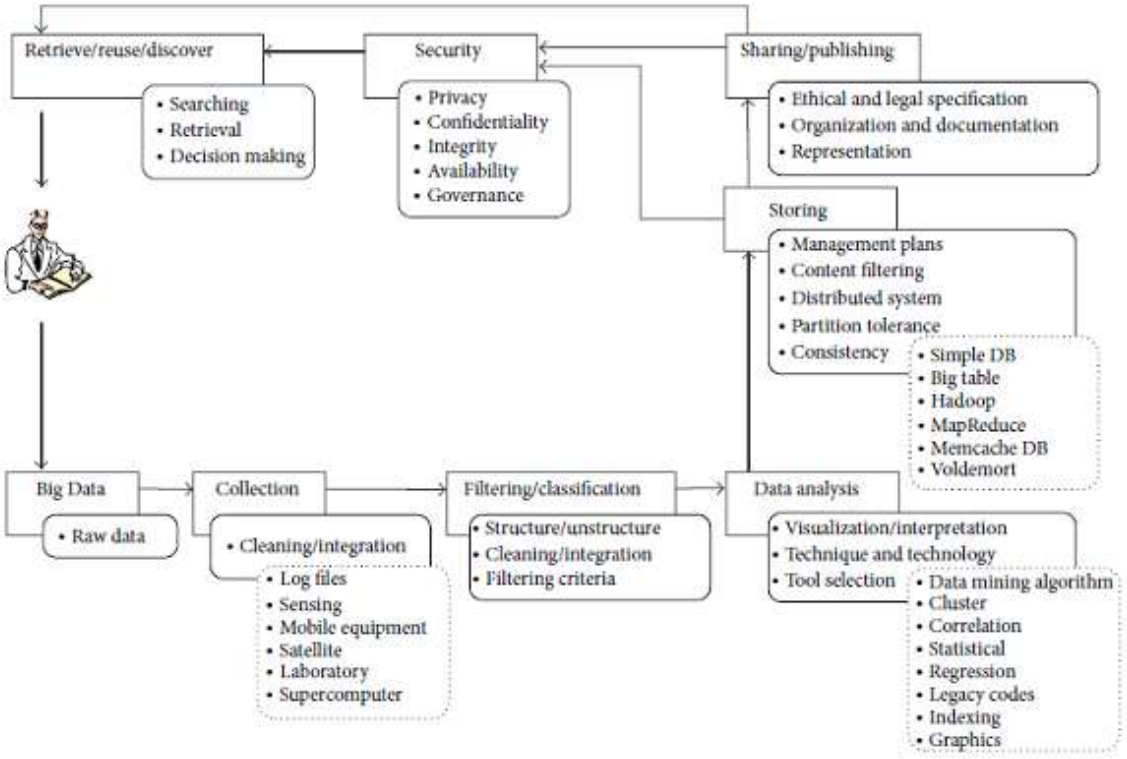

Figure 5: Proposed data life cycle using the technologies and terminologies of Big Data.

Raw Data. Researchers, agencies, and organizations integrate the collected raw data and increase their value through input from specific program offices and scientific research projects. The data are distorted from their initial state and are stored in a value-added state, including web services.

Collection/Filtering/Classification. Data collection or generation is generally the first stage of any data life cycle. Large amounts of data are created in the forms of log file data and data from sensors, mobile equipment, satellites, laboratories, supercomputers, searching entries, chat records, posts on Internet forums, and micro blog messages. Log files are utilized in nearly all digital equipment; that is, web servers note the number of visits, clicks, click rates, and other property registers the web users in log files.

Sensing. Sensors are often used to extent the physical quantities, which are then altered into comprehensible digital signals for processing and storage.

Mobile Equipment. The functions of mobile devices have under wired progressively as their usage rapidly increases. As the features of such devices are complicated and as means of data acquisition are enriched, various data types are produced.

Data Analysis. Data analysis enables an organization to handle abundant information that can affect the business. Data analysis has two main objectives: to apprehend the relationships among

features and to develop effective methods of data mining that can perfectly foresee future observations. Big Data analysis can be applied to special types of data.

Data Mining Algorithms. In data mining, hidden but potentially valuable information is extracted from large, incomplete, fuzzy, and noisy data.

Cluster Analysis. Cluster analysis groups objects statistically according to certain rules and features. For example, objects in the same group are extremely heterogeneous, whereas those in another group are exceedingly homogeneous.

Correlation Analysis. Correlation analysis regulates the law of relations amongst practical phenomena, including mutual restriction, correlation, and correlative dependence.

Statistical Analysis. Statistical analysis is established on statistical theory, which is a division of applied mathematics.

Regression Analysis. Regression analysis is a mathematical technique that can reveal correlations between one variable and others.

Heterogeneity. Data mining algorithms trace unknown patterns and homogeneous formats for analysis in structured formats.

Scalability. Demanding issues in data analysis embrace the management and analysis of huge amounts of data and the rapid increase in the size of datasets.

Accuracy. Data analysis is typically buoyed by relatively accurate data obtained from structured databases with limited sources.

Storing/Sharing/Publishing. Data and its resources are composed and analyzed for storing, sharing, and publishing to benefit audiences, the public, tribal governments, academicians, researchers, scientific partners, federal agencies, and other stakeholders (e.g., industries, communities, and the media). Large and extensive Big Data datasets must be stored and managed with reliability, availability, and easy accessibility; storage infrastructures must provide reliable space and a strong access interface that can not only analyze large amounts of data, but also store, manage, and establish data with relational DBMS structures. Storage capacity must be reasonable given the sharp increase in data volume; for this reason, research on data storage is necessary.

Security. This stage of the data life cycle describes the security of data, governance bodies, organizations, and agendas. It also clarifies the roles in data stewardship. Therefore, appropriateness in terms of data type and use must be considered in developing data, systems, tools, policies, and procedures to defend legitimate privacy, confidentiality, and intellectual property.

Retrieve/Reuse/Discover. Data retrieval warrants data quality, value addition, and data preservation by reusing existing data to discover new and valuable information. This area is specifically involved in various subfields, including retrieval, management, authentication,

archiving, preservation, and representation. The classical approach to structured data management is divided into two parts: one is a schema to store the dataset and the other is a relational database for data retrieval.

3. CHALLENGES

With Big Data, users not only face abundant attractive prospects but also come across challenges. Such complications lie in data capture, storage, searching, sharing, analysis, and visualization. Challenges in Big Data analysis include data inconsistency and incompleteness, scalability, timeliness, and security. Prior to data analysis, data must be well constructed. Understanding the method by which data can be preprocessed is important to improve data quality and the analysis results. Privacy is major concern in outsourced data. Recently, some arguments have discovered how some security agencies are using data generated by individuals for their own benefits without permission.

4. CONCLUSION

This paper presents the elementary concepts of Big Data. These concepts comprise the role of Big Data in the current environment of enterprise and technology. To augment the efficiency of data management, we have devised a data-lifecycle that uses the technologies and terminologies of BigData. The stages in this life cycle include collection, filtering, analysis, storage, publication, retrieval, and discovery. Data are also generated in different formats(unstructured and/or semi structured), which unfavorably affect data analysis, management, and storage. This deviation in data is accompanied by complexity and the development of further means of data acquisition. Big Data has developed such that it cannot be harnessed separately. Big Data is characterized by large systems, profits, and challenges. As a result, additional research is obligatory to address these issues and advance the efficient display, analysis, and storage of Big Data. To improve such research, capital investments, human resources, and pioneering ideas are the basic requirements.

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Intentional Blank

FAULT DETECTION IN MOBILE COMMUNICATION NETWORKS USING DATA MINING TECHNIQUES WITH BIG DATA ANALYTICS

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ABSTRACT

A collection of datasets is Big data so that it to be To process huge and complex datasets becomes difficult. so that using big data analytics the process of applying huge amount of datasets consists of many data types is the big data on-hand theoretical models and technique tools. The technology of mobile communication introduced low power ,low price and multi functional devices. A ground for data mining research is analysis of data pertaining to mobile communication is used. theses mining frequent patterns and clusters on data streams collaborative filtering and analysis of social network. The data analysis of mobile communication has been often used as a background application to motivate many technical problem in data mining research. This paper refers in mobile communication networking to find the fault nodes between source to destination transmission using data mining techniques and detect the faults using outliers. outlier detection can be used to find outliers in multivariate data in a simple ensemble way. Network analysis with R to build a network.

KEYWORDS

Mobile communication, Data mining, Big Data, R Language , fault detection & outlier

1. INTRODUCTION

1.1 Data Mining

Data mining can be viewed as a result of the natural evaluation of information technology. Data mining also named as knowledge mining from data or knowledge mining, because to extract knowledge information from huge amount of data. To generate large databases and extract huge data in various areas is the information technology development. The approach of decision making on database research and recent information technology is to store and manipulate huge data . Data mining techniques are used to sour huge databases in order to find novel and useful patterns. The process of knowledge discovery from data consists of data cleaning, integration, selection, transformation, data mining, pattern evaluation and knowledge presentation. The logical process of data mining used to search through large amount of data in order to find useful data. The goal of this technique is to find patterns that were previously unknown. Once these patterns are found they can further be used to make certain decisions for development of their businesses.

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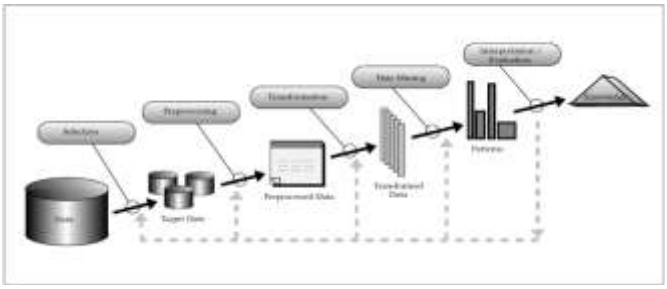
Figure 1 : Knowledge Discovery from data



Three steps involved are Exploration, Pattern identification, Deployment, Exploration: In the first step of data exploration data is cleaned and transformed into another form, and important variables and then nature of data based on the problem are determined. Pattern Identification: Once data is explored, refined and defined for the specific variables the second step is to form pattern identification. Identify and choose the patterns which make the best prediction. Deployment: Patterns are deployed for desired outcome. The data mining techniques Association ,classification, clustering, prediction and anomaly detection (anomalies or outliers) are used in data mining research projects. In association, a pattern is to find the items relationship between the same transaction. In Classification on mathematical techniques are used, that is decision tree induction, such as model overfitting and evaluation of classifier. To build classification models from simple techniques such as rule based and nearest-neighbor classifiers and more other advanced techniques such as support vector machines and ensemble methods.

2. MOBILE COMPUTING

The mobile computation process is mobile computing. A technology that allows transmission of data, via a computer, without having to be connected to a fixed physical link. Over the last few years various cellular networks on number of subscribers very rapidly increase the mobile communication. Cellular networks on small size portable computers are used to communicate or send and receive data easy and accurately. A rapid technology involves is the users transmit and receive data from remote area. In this article we give an overview of existing cellular networks and the CDPD Cellular digital packet data technology which allows data communications across these networks. Finally, we look at the applications of Mobile Computing in the real world. Group of distributed computing systems service providing servers participate connect and synchronize through mobile communication.

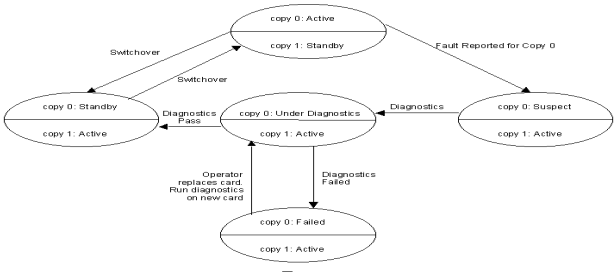
3.FAULT HANDLING TECHNIQUES

This article describes some of the techniques that are used in fault handling software design. A typical fault handling state transition diagram is described in detail. The article also covers several fault detection and isolation techniques.

3.1 Fault Handling Lifecycle

The following figure describes the fault handling lifecycle of an active unit in a redundancy pair.

Figure 2: fault handling life cycle



Assume that the system is running with copy-0 as active unit and copy-1 as standby.

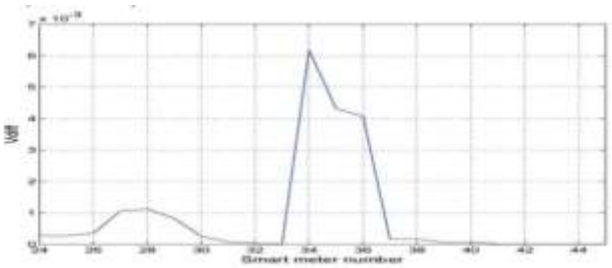
When the copy-0 fails, copy-1 will detect the fault by any of the fault detection mechanisms. At this point, copy-1 takes over from copy-0 and becomes active. The state of copy-0 is marked suspect, pending diagnostics. The system raises an alarm, notifying the operator that the system is working in a non-redundant configuration. Diagnostics are scheduled on copy-0. This includes power-on diagnostics and hardware interface diagnostics. If the diagnostics on copy-0 pass, copy 0 is brought in-service as standby unit. If the diagnostics fail, copy-0 is marked failed and the operator is notified about the failed card. The operator replaces the failed card and commands the system to bring the card in-service. The system schedules diagnostics on the new card to ascertain that the card is healthy. Once the diagnostics pass, copy-0 is marked standby. The copy-0 now starts monitoring the health of copy-1 which is currently the active copy. The system clears the non-redundant configuration alarm as redundancy has been restored.

The operator can restore the original configuration by switching over the two copies. protocol fault is the only fault reported, all the units in the path from source to estimation are probed for health.

3.2.Fault Detection

If the error occurred in the process is fault. Fault detection is indicating if there is a fault. Below graph shows the node fault.

Figure 3 : Fault Detection



Graph showing fault near to node 34

Important role of fault handling is eliminate fault immediately and try to process the fault isolation immediately or as soon as possible. Here are some of the commonly used fault detection mechanisms.

- **Sanity Monitoring:** A unit monitors the health of another unit by expecting periodic health messages. The unit that is being monitored should check its sanity and send the periodic health update to the monitoring unit. The monitoring unit will report faults if more than a specified number of successive health messages are lost.
- **Watchdog Monitoring:** This is the hardware based monitoring technique to detect hanging hardware or software modules.
- **Protocol Faults:** If a unit fails, all the units that are in communication with this unit will encounter protocol faults. The protocol faults are inherently fuzzy in nature as they may be due to a failure of any unit from the source to destination path. Thus further isolation is required to identify the faulty unit.
- **In-service Diagnostics:** Sometimes the hardware modules are so designed that they allow simple diagnostic checks even in the in-service state.
- **Transient Leaky Bucket Counters:** When the hardware is in operation, many transient faults may be detected by the system. Transient faults are typically handled by incrementing a leaky bucket counter. If the leaky bucket counter overflows, a fault trigger is raised.

3.2.1. Fault Table

Generally fault table represented as a matrix contains rows and columns , Let faults C_j represented as colums, test patterns R_i represented as rows, and $P_{ij} = 1$ if the test pattern R_i detects the fault C_j, otherwise if the test pattern R_i does not detect the fault C_j, $P_{ij} = 0$. Denote the actual result of a given test pattern by 1 if it differs from the precomputed expected one, otherwise denote it by 0. The result of a test experiment is represented by a vector where $s_i = 1$ if the actual result of the test patterns does not match with the expected result, otherwise $s_i = 0$. c_j of each column vector equivalent to a fault C_j correspond to a possible result at fault C_j case on test experiment.test experiments on the test patterns quality is depending upon three cases are given below.

a.The test result V matches with a single column vector c_j in FT. This result corresponds to the case where a single fault C_j has been located. In other words, the maximum diagnostic resolution has been obtained.

b.The test result V matches with a subset of column vectors $\{c_i, c_j \ldots c_k\}$ in fault table. This result corresponds to the case where a subset of indistinguishable faults $\{C_i, C_j \ldots C_k\}$ has been located.

c.No match for V with column vectors in fault table is obtained. This result corresponds to the case where the given set of vectors does not allow to carry out fault diagnosis. The set of faults described in the fault table must be incomplete (in other words, the real existing fault is missing in the fault list considered in FT).

Below given example on three test experiments results are V_1, V_2, V_3 explained. V_1 is first case located the single fault, V_2 is second case located the subset of two impossible to differentiate faults, and V_3 is third case located the no fault since the mismatch of V_3 with the fault table on column vectors.

Table 1: example for fault table

	C1	C2	C3	C4	C5	C6	C7
R1	0	1	1	0	0	0	0
R2	1	0	0	1	0	0	0
R3	1	1	0	1	0	1	0
R4	0	1	0	0	1	0	0
R5	0	0	1	0	1	1	0
R6	0	0	1	0	0	1	1

V1	V2	V3
0	0	1
0	1	0
0	1	0
1	0	1
1	0	1
0	0	0

fault C5 located

No match

faults C1 and C4 are not distinguishable

diagnosis not possible

3.2.2. Fault Dictionary

Fault dictionaries (FD) contain fault tables on same data. But the difference is it contains efficient/modernized data. The potential results of test experiments and the faults is mapped. That mapped represented in ordered form and more compressed is fault dictionaries. The given example table shows, the bit vectors columns represent the structured decimal codes or various type of compressed signature.

Table 2:Fault dictionary

No	Bit Vector	Decimal Number	Faults	Test results
1	000001	01	C7	-
2	000110	06	C5	V1=06
3	001011	11	C6	-
4	011000	24	C1,C4	V1=24
5	100011	35	C3	V1=38 No match
6	101100	44	C2	
7	110011	32	C8	

3.2.3 Fault Detection Isolation FDI

Fault isolation is determining where the faulty occurred. If the unit or the part of data is faulty then several fault triggers can be generated for that fault unit. The major purpose of fault isolation to correlate the fault triggers and identify the fault in the data. If fault triggers are fuzzy in nature, the isolation procedure involves interrogating the health of several units. For example, if protocol fault is the only fault reported, all the units of the pathway through source towards destination are survey for strength.

Figure : 4 fault isolation

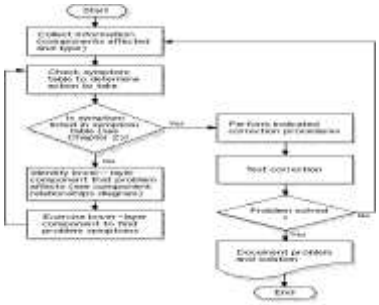
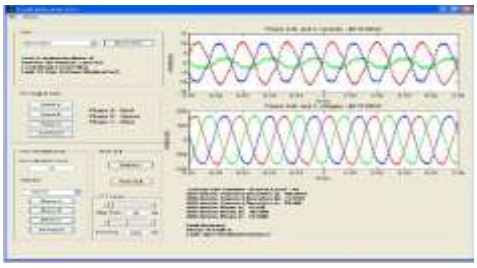


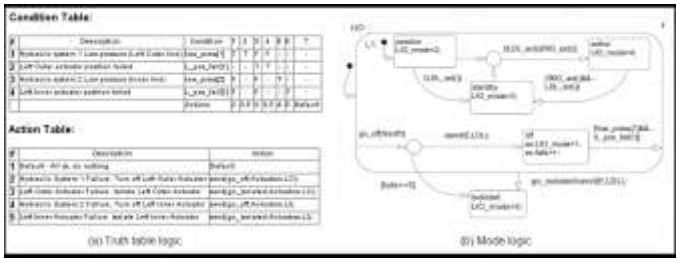
Figure5: fault detection



Fault identification is determine the size of the fault and time of the arrival of fault. Fault detection isolation on model based FDI techniques are used to decide the incident of the fault. The mathematical or knowledge based is the system model. Some of the model-based FDI techniques contain parity-space approach, observer-based approach and parameter based identification methods. There is another trend of model-based FDI schemes, which is called set-membership methods. These methods guarantee the detection of fault under certain conditions. The main difference is that instead of finding the most likely model, these techniques omit the models, which are not compatible with data.The example shown in the figure on the right illustrates a model-based FDI technique for an aircraft elevator reactive controller through the use of a truth table and a state chart. How the controller react to detect faults defines the truth table, and how the controller switches between the different modes of operation (passive, active, standby, off, and isolated) of each actuator defines the state chart.

For example, if in a hydraulic system 1 on fault is detected, then truth table send an incident to the state chart that the left inner actuator should be turned off. The model-based FDI technique most important benefit is reactive controller also connected to a continuous-time model of the actuator hydraulics and it allow the learning of switching transients

Figure 6: model based FDI for Aircraft example



3.3. Fault Diagnosis

Fault detection and fault isolation is the fault diagnosis. To trim down huge computational effort concerned in construct a fault dictionary, the detected faults are *dropped* from the set of simulated faults in fault simulation. Hence, all the faults detected for the first time by the same vector will produce the same column vector (signature) in the fault table, and will be included in the same equivalence class of faults. In this case the testing experiment can stop after the first failing test, because the information provided by the following tests is not used. Such a testing experiment achieves a lower diagnostic resolution. A tradeoff between computing time and diagnostic resolution can be achieved by dropping faults after k>1 detections. Example: In the fault table produced by fault simulation with fault dropping, only 19 faults need to be simulated compared to the case of 42 faults when simulation without fault dropping is passed out (the simulated faults in the fault table are shown in shadowed boxes). As the result of the fault dropping, however, the following faults remain not noticeable: $\{C_2, C_3\},\{C_1, C_4\},\{C_2, C_6\}$.

Table 3: fault diagnosis

	C1	C2	C3	C4	C5	C6	C7
R1	0	1	1	0	0	0	0
R2	1	0	0	1	0	0	0
R3	0	0	0	0	0	1	0
R4	0	0	0	0	1	0	0
R5	0	0	0	0	0	0	0
R6	0	0	0	0	0	0	1

4. DATA MINING FOR FAULT DETECTION

Data mining is an expanding area of research in artificial intelligence and information management whose objective is to extract relevant information from large databases .Data mining and analysis tasks include classification, regression, and clustering of data, aiming at determining parameter or data dependencies and finding various anomalies detection from the data.

4.1 Grid Computing: Grid computing has been proposed as a novel computational model, distinguished from conventional distributed computing by its focus on large-scale resource sharing, innovative applications, and, in few cases, high-performance orientation. Nowadays grids can be used as effective infrastructures for distributed high performance computing and data processing. A grid is a geographically distributed computation infrastructure composed of a set of heterogeneous machines that users can access via a single interface. Grids therefore, provide common resource-access technology and operational services across widely distributed virtual organizations composed of institutions or individuals that share resources.

4.2 Self-Organizing Map: SOM is an important unsupervised competitive learning algorithm, being able to extract statistical regularities from the input data vectors and encode them in the weights without supervision (Feher, K., 1995). Such a learning machine will then be used to build a compact internal representation of the mobile network, in the sense that the data vectors representing its behavior are projected onto a reduced number of prototype vectors (each representing a given cluster of data), which can be further analyzed in search of hidden data structures. The main advantages of their solution are the limited storage and computing costs. However, SOM requires processing time which increases with the size of input data.

4.3 Discrete Wavelet Transform: Discrete Wavelet Transform (DWT) is used to reduce the input data size, features of the data can be extracted without losing the significant data can be used for anomaly detection. Wavelets have been extensively employed for anomaly and fault detection DWT has also been integrated with SOM to detect system faults .

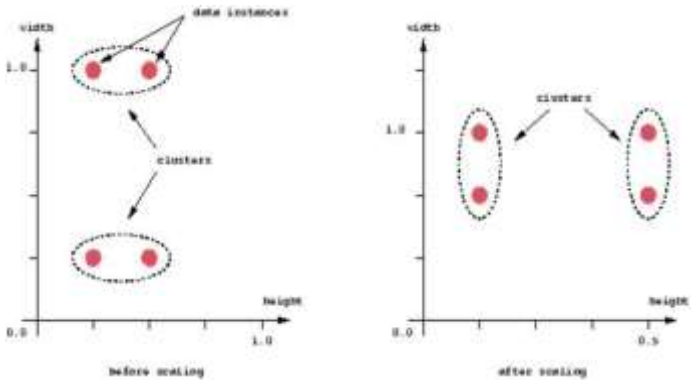
In particular, feature vectors of the faults have been constructed using DWT, sliding windows and a statistical analysis. DWT is a mathematical transform that separates the data signal into fine-scale information known as detail coefficients, and rough-scale information known as approximate coefficients.

Its major advantage is the multi-resolution representation and time-frequency localization property for signals. Usually, the sketch of the original time series can be recovered using only the low-pass-cut off decomposition coefficients; the details can be modelled from the middle-level decomposition coefficients; the rest is usually regarded as noises or irregularities.

4.4 Cluster Analysis: Clustering is a process which partitions a given data set into homogeneous groups based on given features such that similar objects are kept in a group whereas dissimilar objects are in different groups. With the advent of many data clustering algorithms in the recent few years and its extensive use in wide variety of applications, including image processing, computational biology, mobile communication, medicine and economics, has lead to the popularity of this algorithms. Main problem with the data clustering algorithms is that it cannot be standardized. Algorithm developed may give best result with one type of data set but may fail or give poor result with data set of other types. Although there has been many attempts for standardizing the algorithms which can perform well in all case of scenarios but till now no major accomplishment has been achieved. Many clustering algorithms have been proposed so far. However, each algorithm has

its own merits and demerits and cannot work for all real situations. Before exploring various clustering algorithms in detail let's have a brief overview about what is clustering.

Figure 9 : Clustering scaling

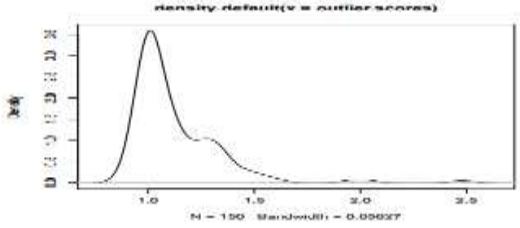


4.5 Outlier Detection by Clustering

The way to detect outliers is clustering. By grouping data into clusters, those data not assigned to any clusters are taken as outliers. For example, with density-based clustering such as objects are grouped into one cluster if they are connected to one another by densely populated area. Therefore, objects not assigned to any clusters are isolated from other objects and are taken as outliers. We can also detect outliers with the k-means algorithm. With k-means, the data are partitioned into k groups by assigning them to the closest cluster centers. After that, we can calculate the distance (or dissimilarity) between each object/nodes and its cluster center, and pick those with largest distances as outliers.

4.6 Outlier Detection with LOF LOF (Local Outlier Factor) is an algorithm for identifying density-based local outliers. With LOF, the local density of a point is compared with that of its neighbours. If the former is significantly lower than the latter (with an LOF value greater than one), the point is in a sparser region than its neighbours, which suggests it be an outlier. A shortcoming of LOF is that it works on numeric data only. Function lofactor() calculates local outlier factors using the LOF algorithm, and it is available in packages DMwR and dprep. An example of outlier detection with LOF is given below, where k is the number of neighbours used for calculating local outlier factors. Figure 10 shows a density plot of outlier scores.

Figure 10 : Density of outlier factors



5. BIG DATA

The most recent trend in the IT world and business right now is Big Data. The term that refers to combinations of data sets whose size, variability, and velocity make them difficult to be captured, managed, processed or analyzed by standard technologies and tools, these relational databases and desktop statistics, within the time necessary to make them useful. To analyse the datasets using R language. Clustering is a data mining technique that makes a meaningful or useful cluster of objects which have similar characteristics using the automatic technique. The upcoming new technologies Big Data ,if the failure occurred it should be within acceptable threshold. Thus the major task is to limit the probability of failure to an "acceptable" level. But it is very expensive to reduce the probability of failure.

6. CONCLUSION

The purpose of this paper is to use data mining tools for identifying defective parts in data communication. First find faults points in transmission nodes and then using data mining techniques detect the faults. Fault detection, isolation, recovery is a subfield of control engineering which concerns itself with monitoring a system, identifying when a fault has occurred, and pinpointing the type of fault and its location. To analysis of datasets use big data tools example R language. R is a programming language and software environment for statistical analysis, graphics representation and reporting. Very fast growing industry is mobile computing. Very limited patterns could be found from real data by human analysts thereby paving way for avenues of data mining research for pattern hunting in mobile communication data sets. Various data mining techniques are discussed for fault detection in mobile communication and further new technique will be introduced for fault detection. The paper also focuses on technical challenges with Big Data processing. using big data analytics faults also reduced.

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Intentional Blank

A WALLACE TREE APPROACH FOR DATA AGGREGATION IN WIRELESS SENSOR NODES

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ABSTRACT:

Wireless Sensor Networks (WSN) refers to a gathering of spatially scattered and committed sensors used for to sense the environmental and physical conditions. The WSN collects and aggregates the data from all the sensor nodes and send it to the sink. But the delay required for Radio transmission of collected information to the sink is very high. If the delay of the network is high then the power consumption may be high it leads to decrease in node life time. So to avoid that problem the delay of the network must be kept at minimum in order to increase the node lifetime. If number of computations required for data aggregation process are low then automatically the delay of the network is also very less. At present a carry look ahead adder with parallel prefix algorithm for data aggregation is used but with this approach is having the disadvantages like high latency and memory. To avoid all those disadvantages a novel tree approach is proposed. The expected results are reduced in latency that is it increase the speed of data aggregation process in Wireless sensor nodes along with less memory requirement for that Tree structure.

KEY WORDS

Nodes, Wireless Sensor Networks (WSN), Folded tree, Wallace Tree

1. INTRODUCTION

A wireless sensor network (WSN) is a network consisting of possibly low size and low complex devices termed as nodes that can sense the environment and monitor that information through Wireless links. The information sensed by the sensors is shared between the nodes through relays and send to the sink by using internet. Wireless sensor Networks are used in many consumer and industrial applications like area monitoring, object monitoring, logistics, intelligent building and medical applications[1] like patient health monitoring, due to the large developments in wireless sensor networks they are used as battlefield surveillance in military applications.

2. CHARACTERISTICS OF WSN'S

Wireless Sensor Networks are having a number of unique characteristics[9] some of them are:

Communication paradigm: In WSN's all nodes are communicated[1]with each other and aggregates data and it is send to the sink.

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Application specific: Depending upon the application Wireless Sensor Networks are developed to perform a specific task.

Scale and density: To cover large areas and to monitor the environmental conditions efficiently large number of nodes are placed[9] in one place that is density of the nodes are high.

Resource constraints: WSN nodes are small in size and battery so the power consumption must be low and delay of the network also kept at low for high speed of data aggregation. Like that WSN,s are having so many constraints.

Minimized Memory for data aggregation: The algorithms used for data aggregation[9] process in WSN,s are using the high memory. To avoid this problem memory required for data aggregation algorithms must be low.

3. REQUIREMENTS OF WSN'S

In order to make these sensor networks a reality, the node implementation and hardware should be optimized for the following three characteristics [9].

Low cost: The networks utility depends on high density of nodes. To make large scale deployments economically feasible, these nodes must be of very low cost.

Small size: The size of modules must be of small size in WSN networks in order to minimize power in sensor nodes.

Low power: WSN networks are having many nodes, battery replacement is very difficult and expensive or even impossible also. Nodes must have efficient energy [3] so that it can function for long periods without running out of power.

4. EXISTING WORK

WSN On-The Node Data Aggregation

Wireless sensor networks (WSN's) got researchers interest in recent years because those are used in wide range of applications. Wireless Sensor Networks could contain hundreds of sensors that collect and in some cases preprocess data before it is send to central node (Sink) for final processing. In most of the cases sensors are deployed to remote location then it is not possible to recharge or replace battery. In that cases solar and wind energy can be used, but such energy supplies are not practically suitable. Hence, increasing the life of wireless sensor networks is an very important issue.

Our existing work is developed with Prefix adder due to its less delay. In WSN ,sensors (nodes or programmable elements) are placed in sensing region. Those sensors are used to sense the data and send that data to sink (central location). All those programmable elements(PE's) are

connected in different structures. Those structures are known as trees which performs data aggregation also.

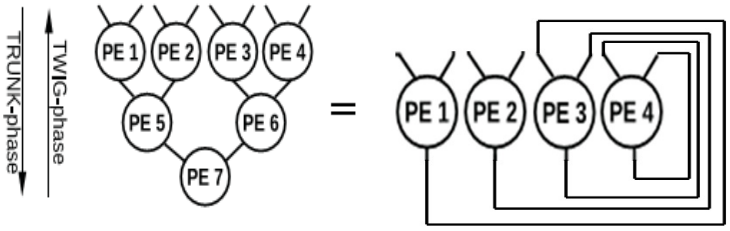


Fig. 1. Left: A binary tree with 7 PEs

Right: Folded tree with 4 PEs which is functionally equivalent to binary tree.

In binary tree 4 PE's (PE_1, PE_2, PE_3, PE_4,)are collected data and that data is added and send it to two PE's (PE_5, PE_6,) then those two data's are aggregated and send it to PE_7.Then PE_7 send that aggregated information to sink.(As shown in Fig.1.Top)

In normal binary tree[1] it requires 7 Programmable elements(PE's) to aggregate two 16 bit inputs and that produces one output but in folded tree structure only 4 PE's are enough to add two 16 bit numbers/data.(as shown in Fig.1.bottom)

Parallel Prefix adders

Prefix adders[7] are well suited for digital circuits to add two numbers then we get a Sum and Carry bit. Carry Look-Ahead Adder is developed by using parallel prefix operation we can categorize into three different stages. They are:-

First stage is the Pre-processing stage where we obtain the Group Generate and Group Propagate signals.

Second stage is the Carry generation stage where we generate the carry using the Group Generate and Group Propagate signals. ($Pi = Ai \oplus Bi$ and $Gi = Ai \cdot Bi$)
Third and Final stage is where we obtain the Sum bit using the Carry bit and the Propagate signal.

The steps illustrated above are as shown in the fig.2.
(P_i, G_i) $(P_{i+1}, G_{i+1})=(P_i.P_{i+1},G_i+P_i.G_{i+1})$ ○

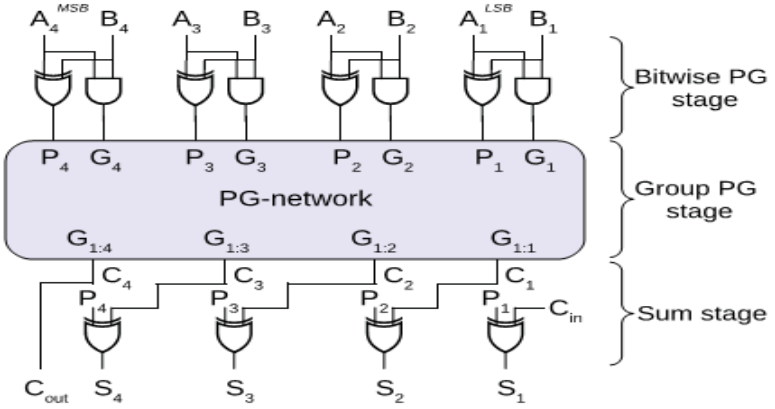


Fig. 2. Prefix adder Folded Tree

In Fig.1. binary tree is implemented in Blelloch's approach as shown in Fig. 1. It requires p = n – 1 PEs area for n inputs .To reduce area and delay, here a fold the tree back onto itself to reuse the PEs the it is called as Folded Tree. This folded tree requires p = ((n – 1)/2) PEs for n number of inputs that is number of PEs are reduced to half.

Folded Tree is implemented in two phases. Those are

Trunk Phase
Twig Phase

5. FOLDED TREE PROGRAMMING

First consider trunk-phase in Folded Tree as shown in fig.3.Bottom. At the Fig. 3.top, a folded tree is designed with four PEs in which PE3 and PE4 are connected differently. In Trunk phase of the folded tree functionality is equivalent to the binary tree that is center again shows how data moves from leaves to the root.

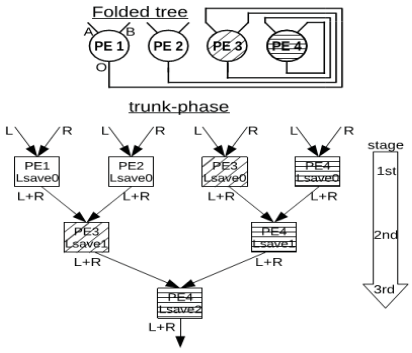


Fig. 3. Top: Four-PE folded tree &Bottom: The trunk-phase program code of the prefix-sum algorithm on a 4-PE folded tree.

In the this Trunk phase of folded tree[1] (as shown in fig.3.Bottom). The data flows by following the below steps :

The left value is stored as L save in Programmable element(PE).

The left and right values are added (L+R) and pass that output to next stage.

Now, the Twig-phase in Folded Tree is considered (as shown in Fig. 4). In Twig Phase the Folded Tree The tree operates in opposite direction to the Trunk phase.

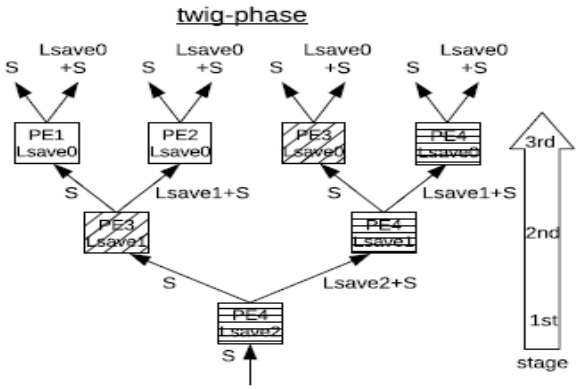


Fig. 4. Twig-phase of 4-PE folded tree.

According to Blelloch's approach in this Twig phase of Folded Tree the data flow is as shown in following steps , (as shown in fig. 4.)

The bottom value(S) is added with Programmable element value (Lsave +S) and propagate that value to right side of the PE.

At left side of the PE only bottom value(value entered into PE) is only propagated.

6. PROPOSED WORK

Our proposed architecture is Wallace tree that performs data aggregation by performing multiplication of data from various sensor nodes and send that multiplied output to the sink. In multiplication process Wallace tree reduces the number of partial products and those are added by using Sklansky adder structure.

Wallace tree:

The Structure of Wallace tree[2] has three steps. Those are,
Partial Product Generation Stage
Partial Product Reduction Stage

Partial Product Addition Stage

Partial Product Generation Stage

Partial product generation is the first step in Wallace tree multiplier. All these are the intermediate product terms generated based on the value of multiplicand and multiplier. If the multiplier bit is '1', then the multiplicand is copied as it is and forms a partial products row and if it is'0', then all the partial products in a row is also zero. From the 2nd bit multiplication onwards, each partial product row is shifted one unit to the left. In signed multiplication process, the sign bit is also extended to the left side. For a conventional multiplier Partial product generators consisting of a series of logic AND gates as shown in Fig.5.

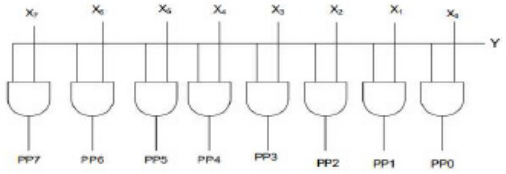


Fig.5. Partial product selection logic for simple

Partial Product Reduction Stage:

In the proposed architecture, partial product reduction is done by the use of 4:2, 5:2 compressor structures and the final stage of addition can be performed by a Sklansky adder. The latency or delay in the Wallace tree multiplier can be reduced by decreasing the number of adders in the partial products reduction stage.

The Wallace tree is constructed by considering all the four rows of input bits in each stage at a time and compress them by using compressors. Thus, compressors form the compulsory requirement of high speed multipliers. The area, speed and power consumption of the multipliers will be directly proportion to the efficiency of the compressors. Thus, in order to satisfy the requirement of speed and power this Wallace tree is developed by using these compressors.

4-2 Compressor:

4-2 compressor (as shown in Fig.6.) has four inputs X1, X2, X3 and X4 and two outputs Sum and Carry along with a Carryin (Cin) and a Carry out (Cout) as shown in Fig. 6. The input Cin is the output from the previous lower significant compressor. The Cout is the output to the compressor in the next significant stage.

5-2 Compressor:

The 5-2 Compressor (as shown in Fig.7.) block has 5 inputsX1,X2,X3,X4,X5 and 2 outputs, Sum and Carry, along with 2 input carry bits (Cin1, Cin2) and 2 output carry bits (Cout1,Cout2) as shown in Fig.7. The input carry bits are the outputs from the previous lesser significant

compressor block and the output carry is passed on to the next higher significant compressor block.

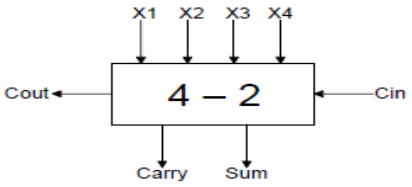


Fig.6. 4:2 compressors

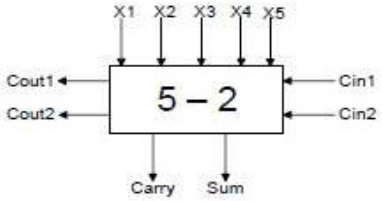


Fig.7. 5:2 compressors

Now the Fig.8. Shows the partial product reduction stage in Wallace tree by using 4:2,5:2 compressors.

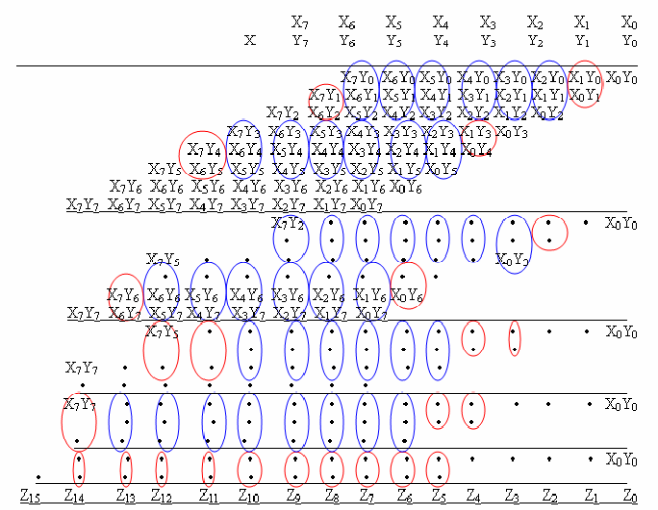


Fig.8. Partial product reduction stage in Wallace tree

Partial Product Addition Stage

Sklansky tree is commonly known as the divide-and-conquer tree it is as shown in Fig.9.

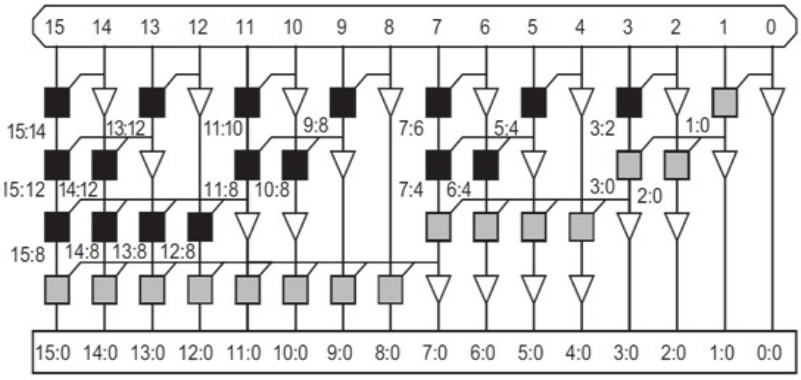
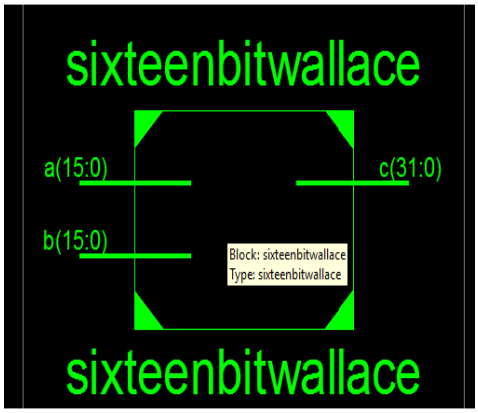


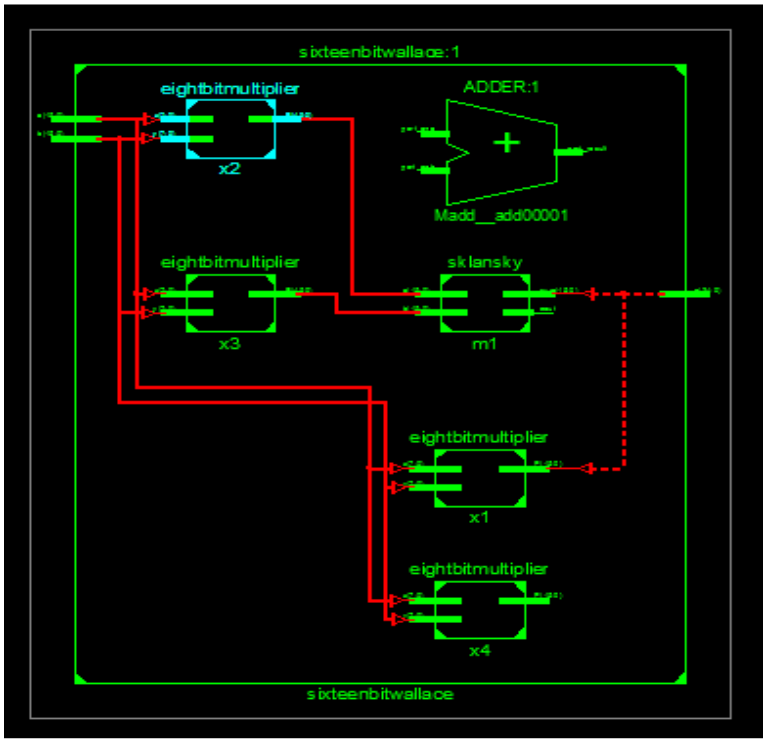
Fig.9. Structure of Sklansky adder

At the final stage of the Wallace Tree this Sklansky adder is used. It reduces the delay to log_2N stages. Hence delay of the Wallace Tree this Sklansky adder is very low.

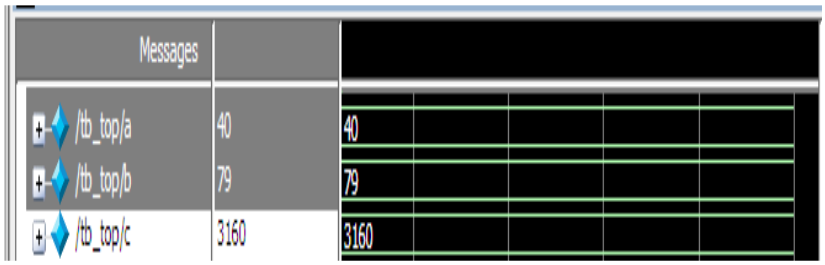
7. RESULTS

RTL Schematic Diagram for 16 bit Wallace tree with Sklansky adder:





Simulation Waveforms for 16 bit Wallace tree with Sklansky adder:



The table 1 describes that 16 bit Wallace tree is having less delay and memory compared to 16 bit folded tree.

Table 1: Comparison of 16 bit folded Tree and 16 bit Wallace Tree:

Parameter	Total values for 16 bit Folded Tree	16 bit Walla Tree in Sklansky adder
Delay(ns)	29.922	23.322
Memory(KB)	329720	179228

8. CONCLUSION

A 16 bit Wallace tree architecture was developed for data aggregation in Wireless Sensor Nodes.

This architecture gives better results compared to folded tree architecture. Those are

1. Less Delay (Speed of Data aggregation process is increases)
2. Memory of the Wallace architecture is also less.

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ANALYSIS OF INERTIAL SENSOR DATA USING TRAJECTORY RECOGNITION ALGORITHM

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ABSTRACT

This paper describes a digital pen based on IMU sensor for gesture and handwritten digit gesture trajectory recognition applications. This project allows human and Pc interaction. Handwriting Recognition is mainly used for applications in the field of security and authentication. By using embedded pen the user can make hand gesture or write a digit and also an alphabetical character. The embedded pen contains an inertial sensor, microcontroller and a module having Zigbee wireless transmitter for creating handwriting and trajectories using gestures. The propound trajectory recognition algorithm constitute the sensing signal attainment, pre-processing techniques, feature origination, feature extraction, classification technique. The user hand motion is measured using the sensor and the sensing information is wirelessly imparted to PC for recognition. In this process initially excerpt the time domain and frequency domain features from pre-processed signal, later it performs linear discriminant analysis in order to represent features with reduced dimension. The dimensionally reduced features are processed with two classifiers – State Vector Machine (SVM) and k-Nearest Neighbour (kNN). Through this algorithm with SVM classifier provides recognition rate is 98.5% and with kNN classifier recognition rate is 95.5% .

KEYWORDS

Trajectory recognition algorithm, Gesture trajectories, inertial sensor, Linear discriminant analysis, SVM, kNN Classifier.

1. INTRODUCTION

Gesture Recognition has become a rapid development search area and many techniques have been proposed to do the gesture trajectory recognition efficiently. Gesture recognition can be categorising into two: online and offline systems and these can be used for human wireless interaction with the computer.

Shengliet.al. [1] presented a Micro (IMU) based on (MEMS) sensor to sense the gesture motion information and mainly focused on human interaction with pc using characters and gesture recognition. Meenaakumariet.al. [2] presents pen with a MEMS accelerometer with three axes and a wireless zigbee transmission module for sensing, collecting and sending it to computer. Accelerations of hand gesture trajectories and display it on the computer. The drawback is displaying the gestures in seven segment display format. Renukaet.al. [3] processed the sensed data while it was under creation so this procedure falls under the category of online character recognition system. However, complexity increased because speed, pressure and strokes to generate a variety of motions differ for different users. Jeen-Shinget.al. [4] developed a portable pen-type device with accelerometer and RF transmission module and a trajectory recognition

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algorithm. Users can create hand gestures at comfortable level with ordinary velocity. Raw signal acquisition, signal preprocessing, obtaining features, selection of valid features, and feature extraction are the steps involved in trajectory recognition algorithm [5]-[12]. In the paper S.Zhang et.al acceleration signal detection, processing and recognition using Hidden Markov Model (HMM) have been performed. In the paper [13], PCA is applied on the features acceleration, speed and position to reduce the feature dimension size. Then HMM with DTW were applied to get the recognition accuracy is 90%. Krishnan et al. proposed to calculate the frequency and time domain attributes of the accelerated signal simultaneously, by placing the sensor on various places on hand of the user. To classify hand motions three techniques named HMM, AdaBoost and k-NN classifier were used, in that AdaBoost classifier achieved an accuracy of 86%.

Taking into consideration the entire literature survey this paper was an implementation of trajectory recognition using an inertial sensor (accelerometer and gyroscope), a microcontroller board, and a wireless zigbee transmission module which is embedded into a pen for sensing and data acquisition. The proposed algorithm used a process as sensing accession, pre processing of raw signals, feature generation, feature extraction and two classification techniques. The Trajectory recognition procedure initially extracts the features with respect to both frequency domain features and time domain features from the inertial sensor signals later performs a linear discriminant analysis to represent the features with reduced dimension set. The reduced features are sent to two classifiers –state vector machines and kNN for better recognition.

The contributions of the project can be pointed as follows:

1. Trajectory Recognition using matlab with two efficient classification techniques.
2. Comparison of types of SVM and kNN and deriving the conclusion of best classifier for better recognition of each Telugu alphabet**.**

3. PROPOSED SYSTEM

The proposed system involves the collection of the experimental data from the given experimental setup and then sending the data wirelessly using Zigbee transmission to the laptop which consists of MATLAB software.

Here, an offline gesture recognition system has been introduced which includes the following components:

- Digital pen
- Laptop with Zigbee receiver

The digital pen senses the hand motions for each handwritten digit or alphabet using an inertial sensor 6 DOF which contains an accelerometer sensor -3axis and gyroscope sensor-3axis and the sensed data is converted in to digital using a microcontroller and transmits the data wirelessly via ZIGBEE technology. Then laptop receives mathematical array of values for each handwritten digit taken from the user via ZIGBEE receiver. The dataset was prepared from various users and is loaded into Matlab. Then analyse the gesture trajectories using two classification techniques and checked for its recognition accuracy.

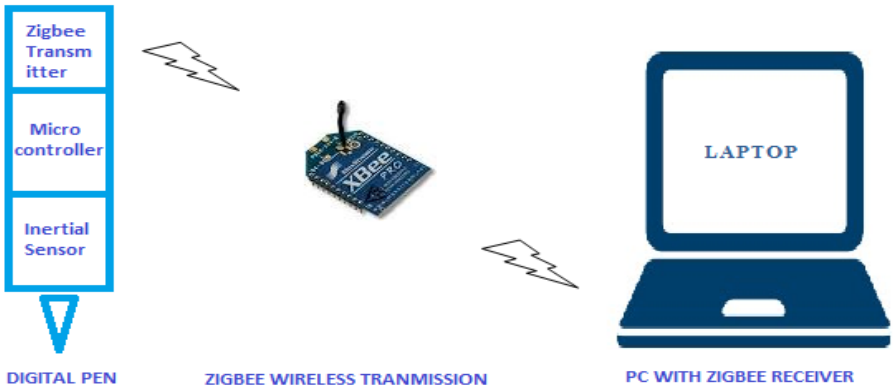


Figure1. Gesture Recognition System

3. SYSTEM FLOW

3.1 Raw Data

In this stage, the data corresponding to the different gestures are in the pattern of Telugu characters. These three gesture are considered for analysing our trajectory recognition algorithm and these patterns are collected from MPU6050. The database which is acquired consists of 300 samples for each letter per person built by attaining gestures from five persons.

i) /a/ ii) /e/ iii) /I/

Figure 2. Gestures written by various users

The figure 2 shows the gesture are in the pattern of Telugu alphabets taken from different users, these are the Telugu alphabets and their pronunciation is given as follows:

ii) /a/ ii) /e/ iii) /I/

The gesture trajectory starts from '.' and ends at the 'arrow' symbol. All users perform the gestures without any or with minimal tilting of the sensor. We constrained the area to a square of 30cm *30 cm and at a height from the ground is 75cm. The transmitter and receiver are separated by a distance of 490cm. At each and every position of the sensor while writing it results out as 6 values in that first three values are gyroscope x-,y-,z- axis and other three values are accelerometer x-,y-,z- axis. After collecting the data from inertial sensor by the movement of hand for a single pattern obtain the data size of 300*6 matrix in .txt format. The numerical data is

stored in the templates folder with names of A, AE, EE …etc. For training the system the data for each gesture is collected from eleven different people.

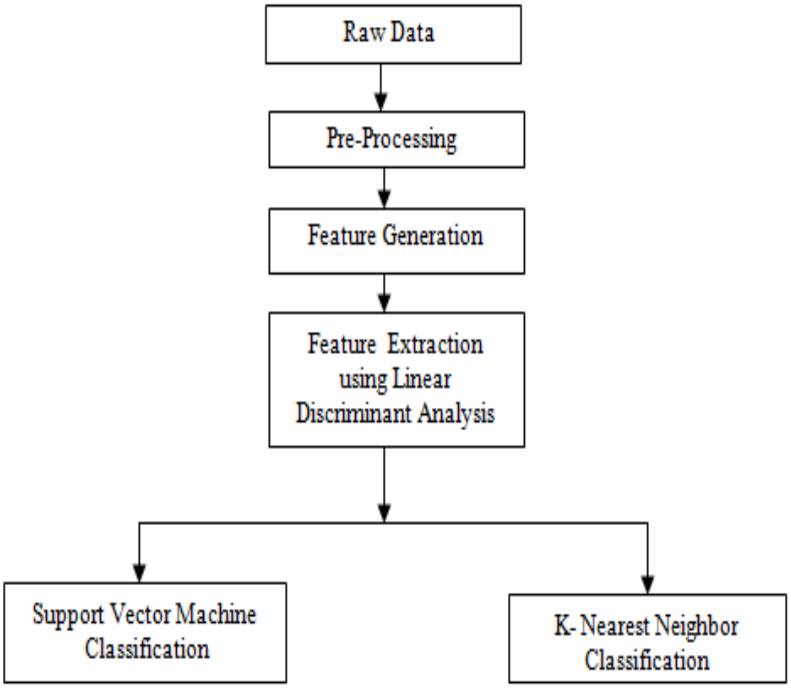


Figure 3. Hand Gesture Trajectory Recognition

The figure 3 illustrates step wise work flow of the entire gesture recognition system. The raw data matrix is initially loaded into matlab and it undergoes pre processing to discard high frequency noise and gravitational acceleration values. Then seven different features are generated and are represented in lower dimension using LDA for efficient classification using SVM and kNN techniques.

3.2 Preprocessing

3.2.1. Moving Average Filter

First, the obtained values undergo calibration for removal of drift errors and offsets. In signal pre processing stage utilizing moving average filter in order to reduce the high-frequency noise which present in the calibrated accelerations. Its functionality is, to produce a single output point by taking the average of N samples at a time. In this paper window size is eight for moving average filter.

3.2.2. High Pass Filter

A high-pass filter is utilised to eliminate the gravitational acceleration from the acceleration caused by hand movement. It is not applied on Gyroscope data.

3.3 Feature Generation

The process of taking disorganised data and defining features are used in analytical study of given data .The gathered features are more informative and non-Redundant when compared to raw data. Here, seven features are generated: Mean, standard deviation, variance, Inter quartile range, correlation, Mean absolute deviation, RMS.

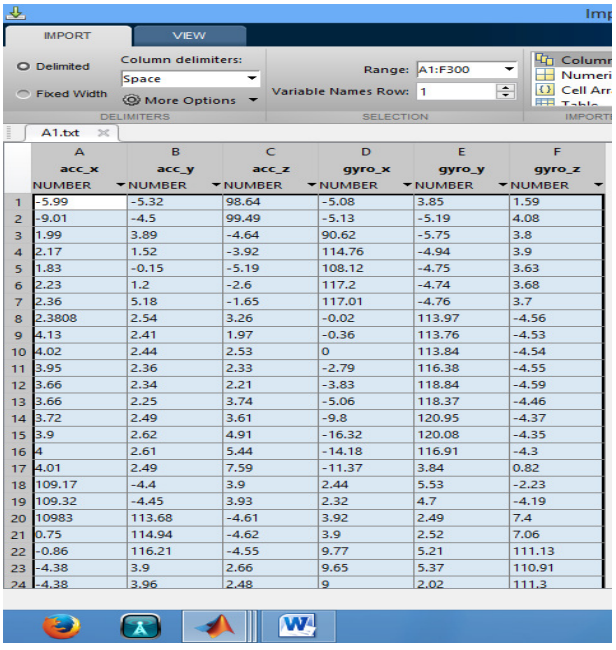
After all the features have been generated in feature extraction that's a special style of dimensionality reduction is applied to the info to get the foremost relevant data from the initial data and represent that information during a lower dimensionality area. It starts from an associate initial set of measured information and select the derived features meant to be more informative and non-redundant, leads to subsequent learning and generalization steps, and also resulting in higher human interpretations. There are many techniques available but in this Linear Discriminant Analysis is employed.

3.4 Classification

To the obtained dimensionality reduced feature vectors different classification techniques have been applied to classify the data into different classes. Comparison tables have been drawn for different classification accuracies have been drawn in the results below.

4. RESULTS

The figure 4 shows exporting the inertial sensor data of Telugu alphabet "ఐ".



	A acc_x NUMBER	B acc_y NUMBER	C acc_z NUMBER	D gyro_x NUMBER	E gyro_y NUMBER	F gyro_z NUMBER
1	-5.99	-5.32	98.64	-5.08	3.85	1.59
2	-9.01	-4.5	99.49	-5.13	-5.19	4.08
3	1.99	3.89	-4.64	90.62	-5.75	3.8
4	2.17	1.52	-3.92	114.76	-4.94	3.9
5	1.83	-0.15	-5.19	108.12	-4.75	3.63
6	2.23	1.2	-2.6	117.2	-4.74	3.68
7	2.36	5.18	-1.65	117.01	-4.76	3.7
8	2.3808	2.54	3.26	-0.02	113.97	-4.56
9	4.13	2.41	1.97	-0.36	113.76	-4.53
10	4.02	2.44	2.53	0	113.84	-4.54
11	3.95	2.36	2.33	-2.79	116.38	-4.55
12	3.66	2.34	2.21	-3.83	118.84	-4.59
13	3.66	2.25	3.74	-5.06	118.37	-4.46
14	3.72	2.49	3.61	-9.8	120.95	-4.37
15	3.9	2.62	4.91	-16.32	120.08	-4.35
16	4	2.61	5.44	-14.18	116.91	-4.3
17	4.01	2.49	7.59	-11.37	3.84	0.82
18	109.17	-4.4	3.9	2.44	5.53	-2.23
19	109.32	-4.45	3.93	2.32	4.7	-4.19
20	10983	113.68	-4.61	3.92	2.49	7.4
21	0.75	114.94	-4.62	3.9	2.52	7.06
22	-0.86	116.21	-4.55	9.77	5.21	111.13
23	-4.38	3.9	2.66	9.65	5.37	110.91
24	-4.38	3.96	2.48	9	2.02	111.3

Figure 4. Importing data array into Matlab

The saved text file from the PC can be imported into matlab using the shortcut import button on the matlab start window. Each column represents inertial sensors axis data:

Column1: acc_x Column4: gyro_x
Column2: acc_y Column5: gyro_y
Column3: acc_z Column6: gyro_z

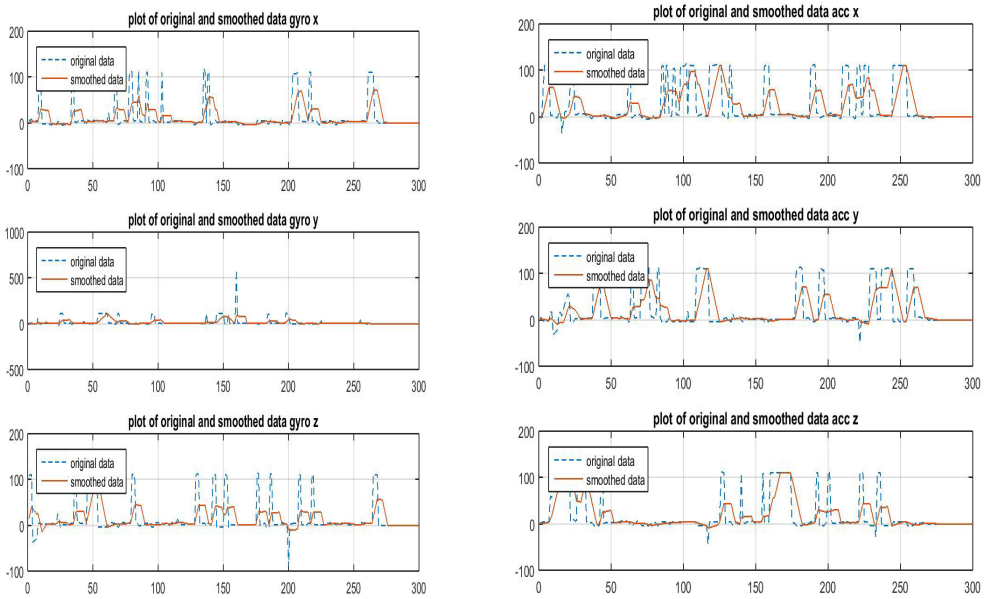


Figure 5. Gyro axis ouputs comparison before and after MVG filter

The figure 5 shows the graphically plotted gyroscopic sensor and accelerometer sensor each axis raw data compared with the moving average filtered data. Moving Average (MVG) Filter has been applied to each column in the obtained array and its functionality is to removes high frequency noise from the raw data.

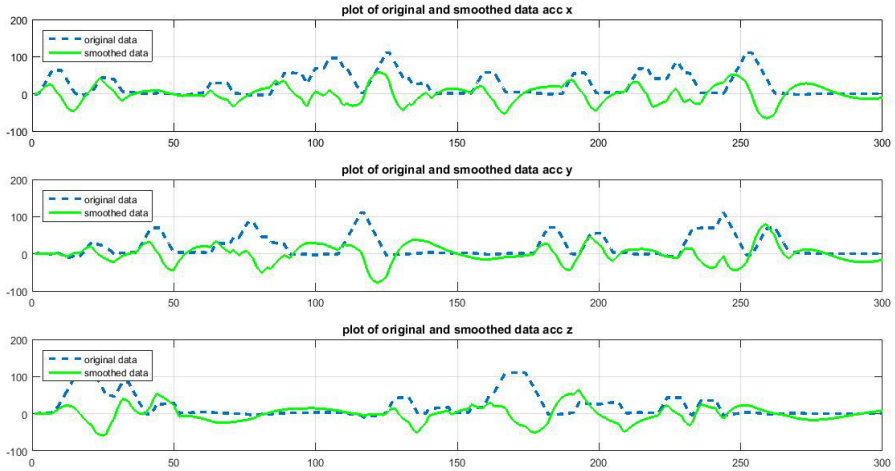
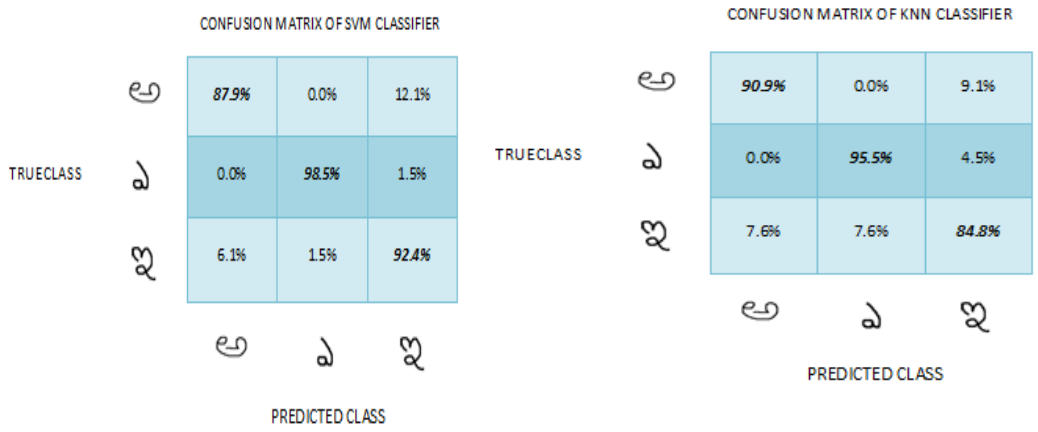


Figure 6. High pass filter output applied for only accelerometer data

The MVG filtered accelerometer data is passed through a High pass filter which removes gravitational acceleration. Above figure shows the comparison graphs of before and after filtering through high pass filter.

After the steps of preprocessing, Feature generation and extraction the Feature columns of eleven writers of each alphabet are concatenated and are taken as predictors and the classes of column is taken as response.



(a) (b)

Figure 7. Confusion matrix with (a) SVM classifier and (b) KNN classifier

Figure 7 shows the confusion matrix of each classifier which indiactes the percentage of correct classification of each gesture pattern. The classification of SVM for gesture /e/ is 98.5% and it is more when compared with KNN for the same gesture is 95.5%.

5. CONCLUSIONS

This paper proposed Telugu alphabet recognition system entirely relying on data from a 3-axis accelerometer and gyroscope. This paper has offered an efficient algorithm skeleton which can build constructive classifier for sensor based gesture recognition and handwriting. The proposed framework comprises hand motion acquisition, pre-processing of the sensing signal, feature generation and extraction, classification technique. With the decreased features, an SVM and KNN can be trained as powerful classifier. In this, we make use of two dimensional hand written Telugu character pattern gestures to validate the efficacy of the algorithm. The gesture recognition rate for SVM is 98.5% as well as for KNN is 95.5%. This end result empowers that the likelihood of usage of embedded pen as a powerful tool chain for computer human interaction applications.

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IMPEDANCE CARDIOGRAPHY FILTERING USING NON-NEGATIVE LEAST-MEAN-SQUARE ALGORITHM

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ABSTRACT

In general using several signal acquisition methods are applied to get cardio-impedance signal to analyse the cardiac output. The analysis completely based on frequency information obtained after applying frequency selection filters and frequency shaping filters. Here proposing a constructive approach involves a developed Non-Negative LMS (NNLMS) followed by filtering techniques to measure and overcome the limitations of commonly used approaches. The proposed technique performance is analysed by considering different types of noise environments like fundamental one white noise and also sum of sinusoidal noise. The simulation results are useful to measure the performance and accuracy under different noise environments also a comparative analysis is done with the proposed work with existing methods under different performance metrics by the help of quantitative analysis of algorithms. Simulation results are found to be satisfactory in the analysis of cardiac output.

KEYWORDS

NNLMS, Cardiac Output, excess mean-square error

1. INTRODUCTION

To acquire cardiac output many traditional approaches are available out of these methods the Impedance Cardio Graphy (ICG) is one acquisition technique. ICG acquisition method [3] involves a repetitive and non-invasive procedure on a beat-by beat basis. ICG is also cost effective and a very sensitive acquisition system of cardiac output. Out of many advantages of ICG methodology the major problem is it was very sensitive to the nose induced by shock or ventilation and movement of body while acquiring the cardiac signal. Based on the operation, the ICG signal Z = Z0 + ¢Z can be processed and analysed with its differential operator signal is processed directly in order to obtain fiducial points [3] like :Opening of aortic valves (B), aortic valve closure (X) and the maximum value of dZ/dt following the opening of valves (C) [3] as shown in figure 1. So many researchers are working towards the analysis of these methods to

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model a fine quantitative analysis and improvement in the performance analysis of cardiac output under different sensitive noise environments. In this work considered Non-Negativity is one of the limitations that can be applied on estimation of parameter [1] due to this physically unreasonable solutions can be avoid an can comply the characteristics of natural phenomena. This non negativity will also appear even in some processing schemes like audio processing, image processing, remote sensing and neuroscience [1]. The non-negativity constraints can be reduced by several processing schemes proposed namely NNLMS algorithms and its three different approaches like Normalisation, Exponential and Sign-Sign. Also transient behaviour and a recursive model analysis which is developed by weights behaviour of adaptive filters [1].

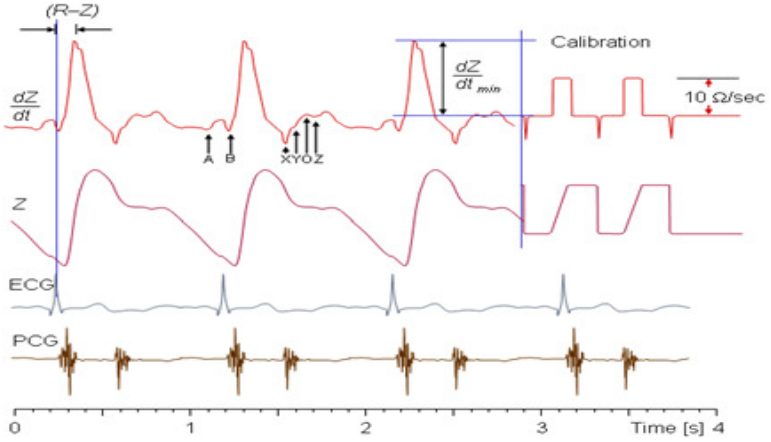

Figure 1: Sample ICG waveform taken from Ref [3].

2. SELECTED METHODOLOGY

2.1. An Artifact Canceller:

Initially impedance sensor is used to collect thoracic impedance signal z(n) which consist of respiratory artifact and Reference signal $r(n)$ is obtained from the respiratory sensor[2]. The respiratory sensor to acquire reference signal there has some delay with respect to the respiratory artifact due to the movement of thorax cage [2]. To equalize a delay is introduce in the impedance signal z(n). As illustrated in figure 2 an FIR filter and its weights are updated continuously to minimize the error e(n) with the help of adaptive algorithm namely Least Mean Square also name as statistical gradient search algorithm. Also the output of filter $\hat{r}(n)$ is subtracted from delayed input impedance signal z(n) there after applied continuously error minimization scheme with algorithms.

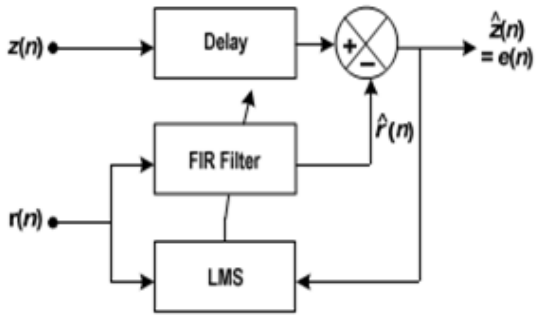

Figure 2: Artifact Canceller using Digital FIR

In this illustration the major purpose of algorithms is only to control or update the filter weights of Digital FIR filter in order to minimize the error.

2.2. Impedance Signal Analysis

The impedance sensor output is initially processed through a low pass filter as a part of eliminating high frequencies there by using 2-point differentiation we can obtain ICG waveform. Even after processing In ICG waveform there will be presence of respiratory artifact especially in the post-exercise recordings [2]. So in order to remove the artifact an artifact canceller illustrated in figure 2 was applied on impedance signal $z(n)$, by considering $\mu = 0.0044$ for adaptation. The results are found to be satisfactory for tap length $M \approx 200$ and sample delay ≈ 70. Because of large value of *dZ/dt* is a useful parameter in the evaluation of stroke volume the same data is processed through the filter with specified inputs of filters. The percentage error was then calculated between the peaks of the standard waveforms and the filtered data with various cut-off frequencies [4].

The peak of *dZ/dt* error values are illustrated with respect to different cut-off frequencies. The peak *dZ/dt* error in all environments is less than 2 percent for a cut off frequency of less than 50 per cent of the heart rate [4].

Assume a linear model of system with inputs and outputs as illustrated in the following equation

$$R(n) = \alpha^{*T} a(n) + z(n) \text{----------(1)}$$

The reference signal $R(n)$ and input signal $a(n)$ are assumed to be stationary and zero mean. The error also assumed to be stationary and minimum variance with zero mean. So based on physical constraints non negativity will be presented in the estimated coefficients to minimize that adaptive system is proposed with improved algorithms in order to minimize the Mean Squre Error with good number filter taps

$$\alpha^{o} = \arg\min_{\alpha} E\left\{\left[R(n) - \alpha^{T} a(n)\right]^{2}\right\} \quad \text{---------- (2)}$$

$$\text{subject to} \quad \alpha_{i} \geq 0, \forall i$$

The non-negativity problem can be solve by updating the Digital FIR filter weights using a NNLMS algorithm with the following weight update equation

$$\alpha(n+1) = \alpha(n) + \eta D_{\alpha}(n) e(n) a(n) \text{----------(3)}$$

The above weight update equation is further normalised in order to improve the performance of weight updating in process of minimisation of mean square error so the modified weight update recursive relation is given as

$$\alpha_{N}(n+1) = \alpha_{N}(n) + \frac{\eta}{x^{T}(n)x(n)} D_{\alpha_{N}}(n) e_{N}(n) x(n) \text{ ----------(4)}$$

So all the above quatitative analysis are very usefull to remove artifacts in ICG waveform threre by the analysis of cardiac data is very effective in application aspects.

3. SIMULATION RESULTS

In the following illustration the collected ECG from impedence sensors are given in figure 3 shows that the recorded $z(n)$ also the processed data using the proposed methodology is displayed in figure 4 shows that Mean Square Error analysis under different environments. ICG waveform obtained after processed by differentiation of $z(n)$ is shown as first one. The impedance waveform after adaptive cancellation of the artifact is shown as second one in Figure 4. ICG obtained by differentiating this waveform shows almost no effect of respiration, making it easy to detect the B and X points and these are found to be consistent with simultaneously acquired PCG [2]. After processed the data through the adaptive filter with algorithms support the performance comparison is illustrated in following tabulation which yields the NNLMS will be the optimised algorithms in the removal of artifacts in ICG for better analysis of cardiac data also in the tabulation given the normalised NNLMS SNR evaluation to compare the existing methods in table 1.

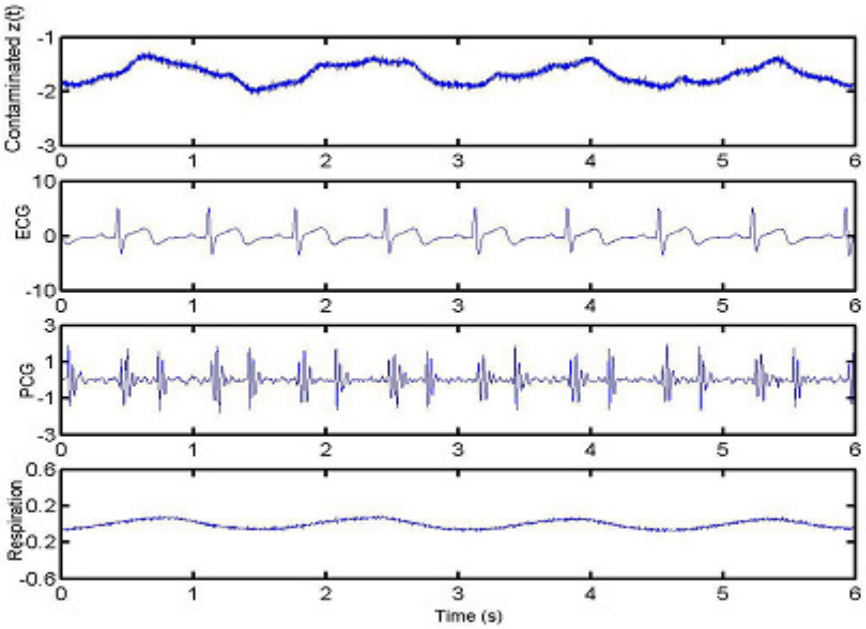

Figure 3. ICG, ECG,PCG in post exercise condition[2].

Table 1: SNR comparision with different algorithms in (a)ICG, (b)ECG, (c)PCG

	SNR dB	(a)	(b)	(c)
EA10	-10	-0.03	4.81	5.31
	-6	3.93	8.26	8.79
	-3	6.84	10.62	11.93
	0	9.74	14.15	13.73
	3	12.42	16.11	16.81
	6	14.89	17.1	18.06
	10	17,61	19.71	19.86

NN LMS-based	-10	12.43	2.63	1.23
	-6	16.5	3.32	4.17
	-3	18.97	6.18	6.92
	0	21.88	8.67	9.71
	3	24.51	11.12	12.47
	6	26.62	13.65	14.87
	10	29.21	17.32	17.62
Normalized NN LMS-based	-10	15.19	3.96	5.37
	-6	19.42	9.91	8.23
	-3	21.88	12.78	11.43
	0	25	16.48	14.59
	3	27.9	19.39	18.03
	6	29.76	21.62	20.82
	10	33.35	26.42	23.43

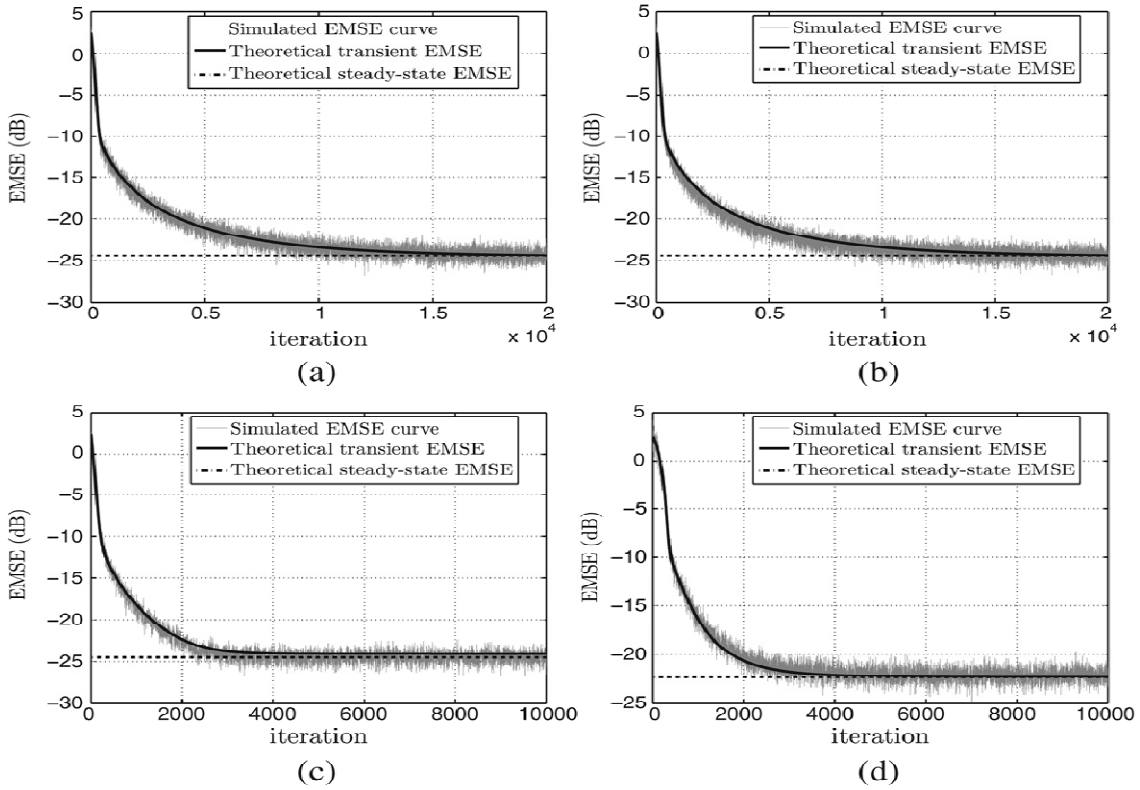

Figure 4: Different EMSE evaluation of NNLMS and its Types

4. CONCLUSION

In the proposed constructive approach in addition to the artifacts removal a performance comparisons made in the part of analysis of cardiac data under different noise environments. Also excesses Mean Square Error is observed on different cardiac data in steady state, transient using NNLMS and its variants. The quantitative analysis will provide the performance analysis of adaptive algorithms by weight updates under different filter taps environments. Finally the results are found to be satisfactory in few aspects like EMSE, filter taps and weight updating models.

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GENERAL KALMAN FILTER & SPEECH ENHANCEMENT FOR SPEAKER IDENTIFICATION

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ABSTRACT

Presence of noise increases the dimension of the information. A noise suppression algorithm is developed with an idea of combining the General Kalman Filter and Estimate Maximization (EM) frame work.This combination is helpful and effective in identifying noise characteristics of an acoustic environment. Recursion between Estimate step and Maximization step enabled the algorithm to deal any model of noise. The same Speech enhancement procedure in applied in the pre-processing stage of a conventional Speaker identification method. Due to the non-stationary nature of noise and speech adaptive algorithms are required. Algorithm is first applied for Speech enhancement problem and then extended to using it in the pre-processing step of the Speaker identification. The present work is compared in terms of significant metrics with existing and popular algorithms and results show that the developed algorithm is dominant over them.

KEYWORDS

Speech processing, Speech enhancement, Speaker identification, General Kalman filter and EM algorithm

1. INTRODUCTION

The two major applications of the speech processing namely speech enhancement and speaker identification are inter related in terms of the core techniques used for performing them. Speech enhancement directly resembles the pre-processing stage of the speaker identification procedure in most of the cases. The work depicts the relation and significance of developing an algorithm to address the core areas of their respective step wise procedure is the area of interest.

Speech and noise in a natural environment always finds in a combined form, Speech is every time degraded by the noise. General assumption is to always find an addiction of Gaussian noise to the speech information signal. This noise varies in its characteristics for different acoustic environments. The idea is to develop a robust algorithm to deal a noise of any environment that is degrading speech. Elimination of noise could be even possible through the transducers like microphone used to record the speech information and convert them to the electrical equivalent representation. There are techniques developed based on the number of microphones to be used

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to identify the noise components in the signal. The present work is based on Single microphone speech enhancement.

Noise in the problem is first modelled as an Auto Regressive process. This performed as in [3]. Estimate Maximization frame work is studied which involves speech enhancement and as well as parameter estimation. General Kalman Filter(GKF) is a time domain algorithm first studied for using it system identification problem like echo cancellation in [4]. In Echo cancellation echo path estimation is performed using GKF. For extending the General Kalman filter to the speech enhancement it has to be given with at least one among the knowledge of two characteristics of speech or noise. EM frame work helps in providing the noise characteristics.

The time domain implementation of the Kalman filter is difficult and not dominant. G.Enzner through his studies proposed the effective implementation of Kalman filter in frequency domain [2]. But GKF is time domain implemented version of Kalman filter and hence draws the attention. Speaker Recognition is a part behavioural characteristic of the Biometrics. The two major classifications are Speaker verification and Speaker identification namely. Speaker identification can be either text dependent or text independent. In this paper a text independent speaker identification method is considered with a pre-processing stage of developed algorithm.

2. DEFINITION OF THE PROBLEM AND RELATED CONCEPTS

$x(n)$ is a noisy speech signal, $s(n)$ and $v(n)$ are its two components.

$$x(n) = s(n) + v(n)$$

Clean speech signal is represented with $s(n)$ and it obtained by supressing additive noise $v(n)$ in $x(n)$.

2.1. Aim

Single microphone is used to record the degraded speech. The developed algorithm is aimed to use in studying then noise characteristics and suppression of the noise components from the signal. Thus to provide the speech quality enhancement and intelligibility.

2.2. General Kalman Filter

In [4] General Kalman filter is implemented with two estimation problems. The first is a hidden Markov modelled impulse response coefficient estimation and the second is the estimation of desired response with knowledge of the above estimated coefficients and far end signal. In this work the problem is redefined to fit for a speech enhancement problem. The similar coefficient estimation is equivalent to the change affecting the noise characteristics of the acoustic environment under consideration. And these are updated for find new noise model from previous effects as recursive process by applying estimate maximization frame work.

2.3. Estimate Maximization frame work

There are two steps in this process namely estimation step and maximization step. It is a recursive procedure. And the ending if the recursion is predefined or left to the intelligibility of the algorithm. General Kalman filter provides estimation of the required entity in estimation step. These parameters involved in the estimation are identified and updated in the maximization or parameter estimation step and again fed to estimation step. This repeats as an iterative process until the clean entity of interest is obtained.

2.4. Proposed Methods

The Figure 1 represent the block diagram of combined speech enhancement for speaker identification, the first half of the diagram illustrates the process flow of speech enhancement as follows

i. Noise degraded speech information is collected through single microphone.
ii. This is given to the speech enhancement stage.
iii. The first step of speech enhancement contains the segmentation of speech signal satisfying the stationary condition of the signal.
iv. Thus frames are extracted from the source information and each frame is now forwarded for noise suppression individually.
v. The AR model of the noise of the acoustic environment is acquired prior to the above steps and state space formulation is done to it.
vi. The estimation process starts by giving noise estimate and present speech frame to General Kalman filter to find optimum output.
vii. The parameters are updated in maximization step and again given to GKF for new estimation
viii. This Process continues until clean speech frame is obtained for a fixed number of iterations.
ix. Finally all the frames are concatenated to obtain clean speech.

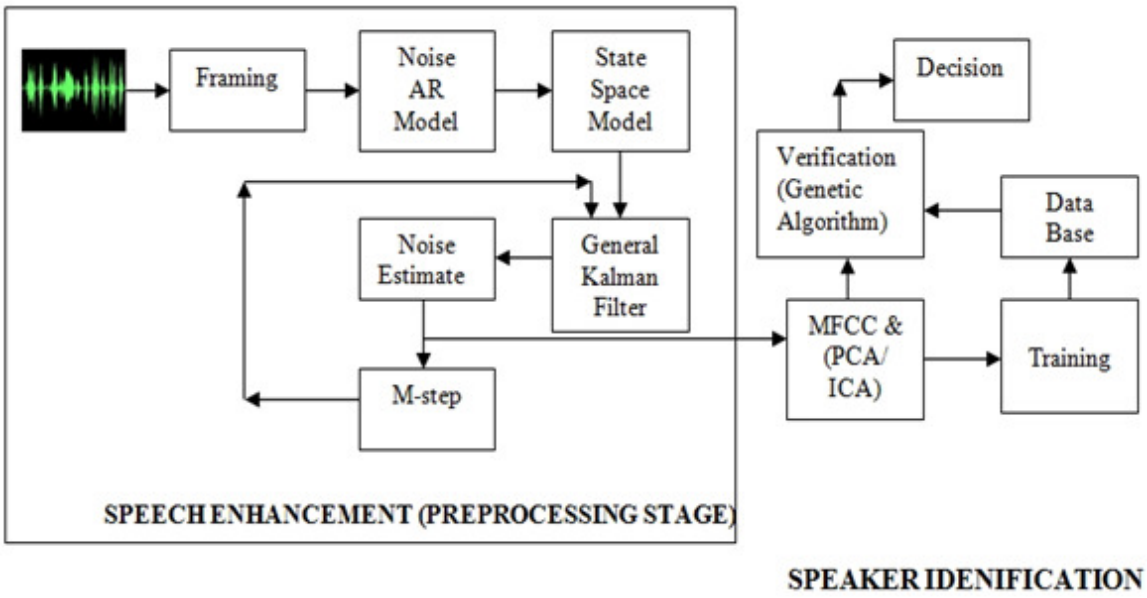

Figure1. Proposed Speech Enhancement for Speaker identification

Figure 1 represents the proposed method for Speaker identification

i. The initial stage of speaker identifications always be the speech enhancement stage. The output of the Speech enhancement stage is a clean speech.
ii. Training phase and Verification are two stages of identification. In training phase speech features of the concerned group are collected and stored in data base.
iii. In verification stage they are retrieved to compare with the features of persons speech waiting for authentication.
iv. If the matching criteria satisfies authentication is provided otherwise rejected.
v. In this paper Eigen features based speech features are extracted in feature extraction stage. MFCC range of frequencies is under consideration.
vi. Dimensionality reduction techniques like principal component analysis (PCA) and Independent Component analysis (ICA) used for reducing the feature space.
vii. Genetic Algorithm is used for verification procedure to provide optimum results and the cost function of it is defined below.

$$\sum_{m=1}^{L}\left(\max\left|R(m)\right|\right)^2+\lambda\sum_{m=1}^{L-1}\sum_{m=n+1}^{L}\left(\max\left|P(m,n)\right|\right)^2 \qquad (1)$$

R=Auto correlation (Correlation between each speech feature itself), P=Cross Correlation (Correlation between speech feature with other speech feature),L=Length of each speech feature,Weighing factor λ

3. ALGORITHM

3.1. Auto Regressive modelling of noise

Let us consider the problem in a discrete time index of n,

$$x(n) = s(n) + v(n) \tag{2}$$

Noise and speech are non-stationary. Hence, any one of them has to be known in order to go for formulation. Consider the speech absent periods to study noise characteristics,

$$x(n) = v_0(n) \tag{3}$$

Where $v_0(n)$ is signal collected by recording device when speech is absent and use as initial signal vector of noise. Noise is modelled as stochastic AR process:

$$v(n) = -\sum_{q=1}^{k} \lambda_q v(n-k) + \frac{g_v}{2} u_v(n) \tag{4}$$

$\lambda_1, \lambda_2, \ldots \lambda_k$ represents AR parameters of noise process and g_v represents power level. $u_v(n)$ is normalized (zero-mean unit variance),white Gaussian noise.

3.2. E-step

AR model of noise process is converted into state space formulation

$$v_k^{\ T}(n) = [v(n-k+1), v(n-k+2), ..., v(n)]$$

$$\Phi_v = \begin{bmatrix} 0 & 1 & 0 & 0 & ..... & 0 & 0 \\ 0. & 0 & 1 & 0 & ..... & 0 & 0 \\ . & . & . & . & & . & . \\ . & . & . & . & ..... & . & . \\ . & . & . & . & & . & . \\ . & . & . & . & ..... & . & . \\ -\lambda_k & -\lambda_{k-1} & -\lambda_{k-2} & -\lambda_{k-3} & ..... & -\lambda_2 & -\lambda_1 \end{bmatrix}$$ is noise transition matrix and k-

dimensional vectors $g_v^T = \begin{bmatrix} 0 & 0 & ..... & g_v \end{bmatrix}$.The below equation provides estimate of noise

$$v_k(n) = \Phi_v v_k(n-1) + g_v(n)u_v(n) \tag{5}$$

$$x(n) = s(n) + h_v^T(n)v_k(n) \tag{6}$$

$$s(n) = x(n) - h_v^T(n)v_k(n) \tag{7}$$

3.3. M-step

Parameters for estimate and AR model, GKF algorithm procedural steps results in finding the minimal error and optimal estimate. The following are the related equations

Initialize with $\hat{h}_v(n) = 0$ and $R_\mu(0) = \varepsilon I_q$ where ε is small positive constant

$$\hat{h}_v(n) = \hat{h}_v(n-1) + w(n) \tag{8}$$

$$x(n) = s(n) + h_v^T(n)v_k(n) \tag{9}$$

$$e(n) = x(n) - \hat{v}(n) \tag{10}$$

$$R_m(n) = R_\mu(n-1) + \sigma_w^2(n)I_q \tag{11}$$

$$R_e(n) = v_k{}^T(n)R_m(n)v_k(n) + \sigma_v^2(n)I_p \tag{12}$$

$$K(n) = R_m(n)v_k(n)R^{-1}{}_e(n) \tag{13}$$

$$e(n) = x(n) - v_k{}^T(n)\hat{h}_v(n-1) \tag{14}$$

$$\hat{h}_v(n) = \hat{h}_v(n-1) + K(n)e(n) \tag{15}$$

$$R_\mu(n) = [I_q - K(n)v_k{}^T(n)]R_m(n) \tag{16}$$

Where $R_m(n)$ is priori misalignment, $R_\mu(n)$ is posteriori misalignment correlation matrix, $K(n)$ is Kalman gain, I_q is identity matrix, $\sigma_w^2(n)$ is variance of $w(n)$, $R_e(n)$ is priori error vector correlation matrix and $e(n)$ is error between signal and estimated.

Let θ be the vector of unknown parameters and given as vector $\theta^T = \begin{bmatrix} \lambda^T & g_v \end{bmatrix}$

$$Z = v_q(n-1)v_q^T(n-1) \tag{17}$$

$$Y = v_q(n-1)v(n) \tag{18}$$

Where updated parameters are defined as

$$\hat{\lambda}^{(q+1)} = -\sum E[Z]\sum Y \tag{19}$$

$$\hat{g}_v^{(q+1)} = \sum\left[Z + \left(\hat{\lambda}^{(q+1)}\right)^T E[Y]\right]. \tag{20}$$

4. RESULTS

4.1. Simulation and Metrics

NOIZEUS speech corpus contains noisy speech signals. These are directly used to test the performance of the proposed algorithm. The similar experiments are conducted with popular algorithms and are used for comparison. Peak signal to Noise ratio and Mean square error are used to evaluate performance for Speech enhancement. Identification rate and elapsed time for a fixed number of generations are compared for Speaker identification. Simulations are performed in MATLAB platform and respective analysis is presented below.

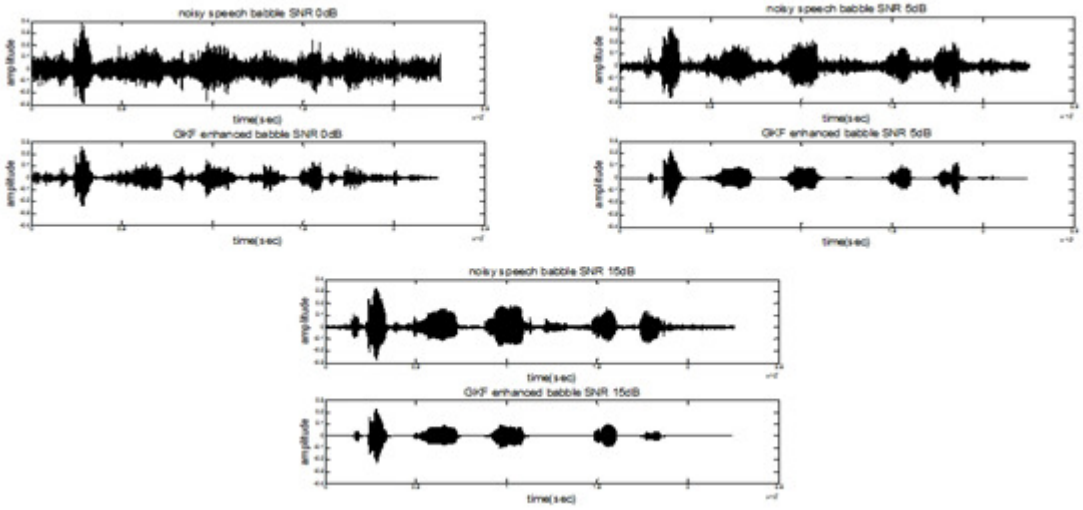

Figure 2. Noisy and GKF enhanced babble noise type of SNR 0dB, 5dB, 15dB

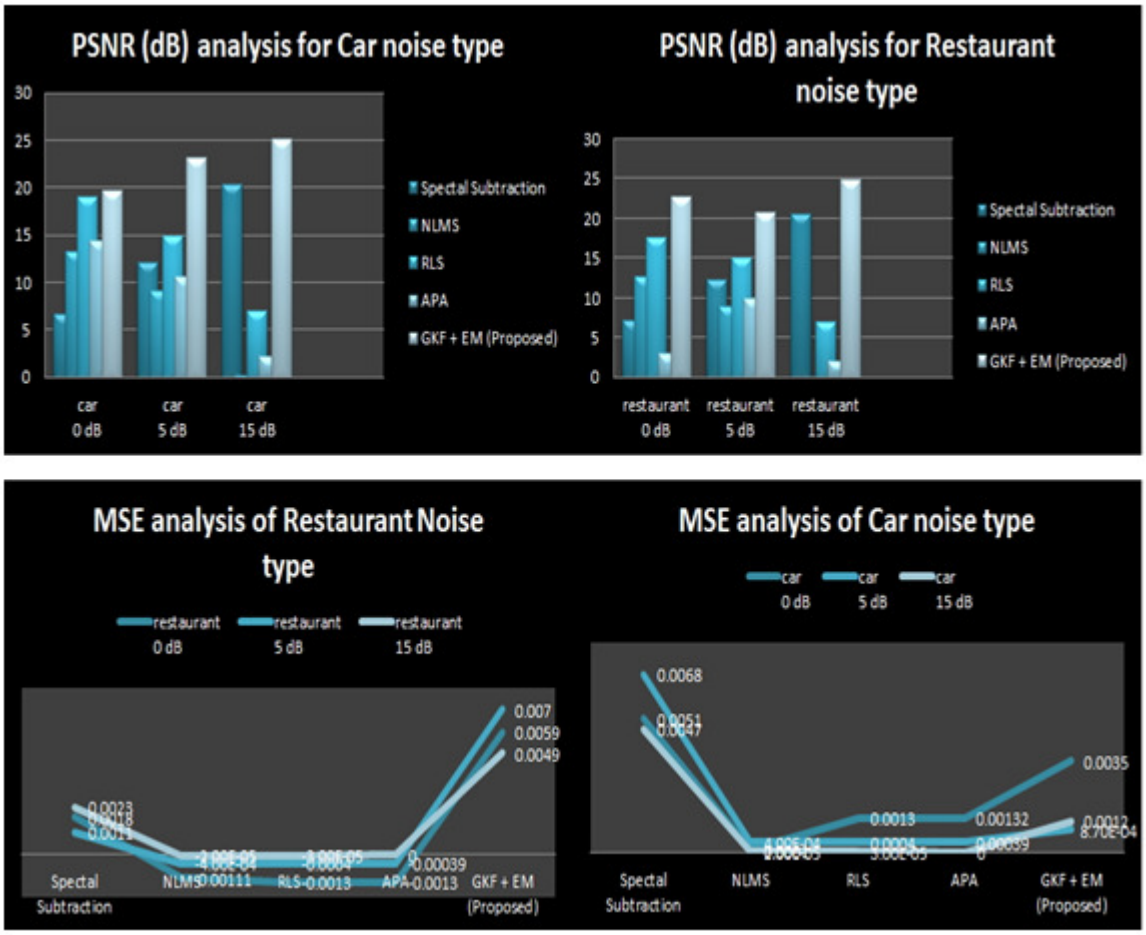

Figure 3.PSNR and MSE comparison of SS, NLMS, RLS, APA and GKF (Speech Enhancement)

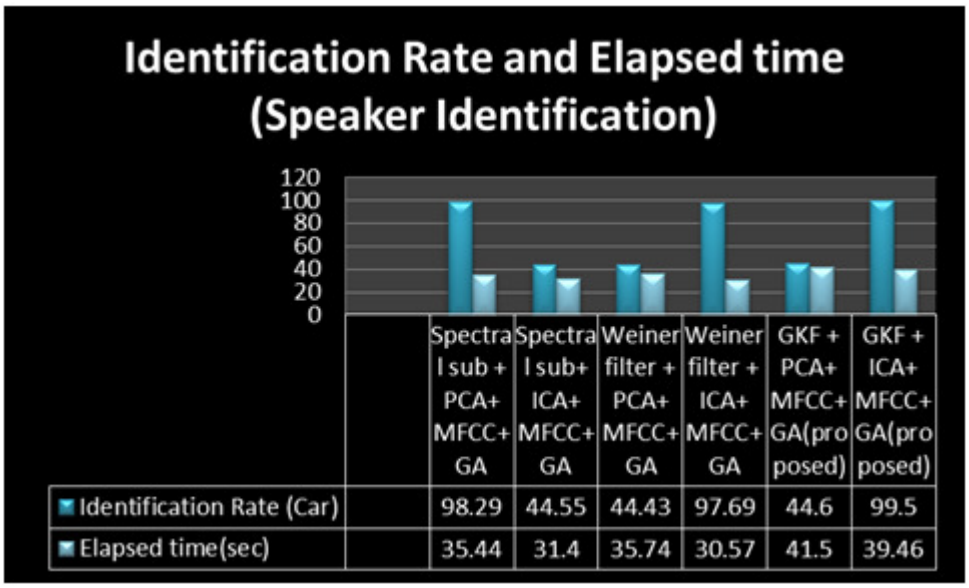

Figure 4. Identification rate comparison of different processing method combinations (Speaker Identification)

5. CONCLUSIONS

General Kalman filter resembles Affine projection algorithm (APA) for certain considerations but the combination with Estimate Maximization is more efficient for GKF. Figure 2 presents the MATLAB simulated results of babble noise type of various SNR levels. Figure 3 is the analysis of proposed algorithm, Normalized least mean square algorithm, Recursive least squares, APA and Spectral subtraction for Speech enhancement applications. Proposed algorithm has given better results in terms of Mean square error and Peak signal to noise ratio. Figure 4 clearly shows the dimensionality reduction effect on the speaker identification system with change in filtration scheme. The respective identification rates and elapsed time of different methods and combination under considerations presented in figure 4 shows GKF is optimum. This work could be further extended to real time and then performance has to analyzed to know its compatibility.

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SLOPE AT ZERO CROSSINGS (ZC) OF SPEECH SIGNAL FOR MULTI-SPEAKER ACTIVITY DETECTION

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ABSTRACT

Multi-Speaker activity (MSA) detection helps in detecting the presence of whether the speech signals has a single speaker or multiple speaker speeches in the speech signal. It is easy to calculate the slope at ZCs (zero crossings) of the speech signal and makes a comparison with a suitable threshold (Th). Multi-speaker is declared as and when the zero crossing value exceeds the threshold. The impact of the proposed technique is compared to the existing technique by calculating the sample-by-sample ZCR (Zero crossing rate) value is demonstrated. Experimental results prove that the proposed ZCR technique achieves accurate results than the traditional techniques for MSA detection that uses the cepstrum resynthesis residual magnitude (CRRM) in the literature.

KEYWORDS

Feature Extraction, Multi-Speaker Activity Detection, Zero Crossing Rate.

1. INTRODUCTION

The task of Multi-Speaker activity (MSA) detection from speech refers to whether the input speech has single speaker speech or a multiple number of speakers speech. Many studies have tried to address this problem [1]. There are a number of applications for MSA detection ranging from speaker identification or recognition to speech recognition in multi-speaker speech scenario [2]-[4].

MSA detection task is useful in speaker recognition [5], [6], in the sense that if the input speech has either single or multiple number of speakers. First there is a need for identifying the input speech whether it has a single speaker or multiple speakers speech and then after identifying the multi-speaker. Separation of the speech of the individual speakers from that of the multi-speaker speech signals are essential [7].

Once the region of multi-speaker speech is identified, there is a need for detecting the number of speakers available in the multi-speaker speech information [8]-[9]. This problem is referred in the literature as a detecting number of speakers from the speech signal. For this problem, a number of speaker detection, the task of MSA detection is like preprocessing stage before detecting the number of speakers.

Once the number of speakers are identified, we can separate each speaker speech information for speaker recognition or speech recognition. Generally, from the studies [10], we can observe that

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there is a need for enhancing each speaker speech before further proceeding for speaker recognition or speech recognition. The study of literature shows voice activity detection in multi-speaker speech scenarios such as data available at meetings, cocktail party problem, etc [11].
In [12], the authors have presented Double talk (DT) detection method in Acoustic sound cancellers (AEC). Handling DT detection is the major issue that has been renamed at the forefront is AEC development. If both the speakers speak simultaneously, then DT happens. In order to cancel far-field echo, an adaptive filter is developed in an AEC. The convergence is strongly influenced by the very presence of near-field signal. In the commercial AECs, DT detectors are commonly available. DT detector methods can be reviewed in [13]-[17].

Recently in [18], the authors have approached a method based on the measurement of the ZCR. A comparison has been done for DT detection. They employed normalized least-mean square (NLMS) formed AEC for DT detection method and is therefore, zero crossing rate is estimated over a samples of window and then it is updated. This method requires cost effective and its convergence rate is slow.

In this study, we have chosen the solution using the slope at ZCR of the speech signal. It is observed that, lower number of ZCR can be seen for a single speaker, whereas the higher number of ZCR is observed for multiple speakers.

The outline of the paper is as follows: The database used for this study is presented in next Section. In Section III, the feature extraction methods which include ZCR and cepstrum resynthesis residual magnitude (CRRM) are discussed. The proposed methodology for ZCR is presented in Section IV. The detailed experimental results are presented in Section V. Finally, the conclusion of the present work is mentioned Section VI.

2. DATABASE USED FOR STUDY

The database consists of 280 speech samples recorded by 28 speakers. Each speaker utters an isolated digit ranging from 0 to 9 (10 digits), in English. Out of 28 speakers, 14 are male and 14 are female. This database includes five conversations for each of the single male, single female, male-male, female-female, and male-female (mixed) speaker conversations. In this study, we considered multiple speakers data as male-male (14 combinations), female-female (14 combinations), and male-female (14 combinations) speech data. Hence, total 42 multiple speaker speech data are considered. The speech samples are recorded directly over an android cellular phone in a sound proof room. All the audio signals are stored in the Wav format with an 8 kHz sampling rate, bit rate of 16 bits and in mono (single channel) format. The average duration of the samples is about 3 seconds per speaker.

3. FEATURE EXTRACTION

3.1. Zero Crossing Rate (ZCR)

In discrete-time signals, when 2 successive samples show against signs, zero crossing happens. The total number of zero crossings per sample is measured by ZCR. In an analysis, M samples of window size are used. The window size is calculated using ZCR divided by M. The ‘i’ is an instance of time, the ZCR of a discrete-time signal x(i) and slope (μ) are described as

$$ZCR(y(i)) = \frac{1}{2M} \sum_{j=i-M+1}^{i} \left| \sin(y(j)) - \sin(y(j-1)) \right| . W(i-j) \quad (1)$$

Where signum (sin) function is given as

$$\sin(y(i)) = \begin{cases} 1, & y(i) \geq 0 \\ 0, & y(i) < 0 \end{cases} \quad (2)$$

$$Slope(\mu) = \frac{1}{ZC} \sum_{i=1}^{ZC} \left| y(i+1) - y(i-1) \right| \quad (3)$$

Here the ZC is number of zero crossings and window parameter is $W(i)$. When 2 signal samples have different sign and absolute function is equivalent to 2, then zero crossing occurs. The right-hand side summation of equation (1) is equal half of the ZCR. After deciding zero crossing rates from one end to other of M window samples, get the next estimate of short-time window by incrementing K samples.

The short-time autocorrelation and short-time energy are not only used to show time-domain signals, but also for ZCR. In past, zero crossings have been employed to show the discrimination between speech and speaker. Frequency approximation of sinusoidal signals is one of the prime importances of ZCR. If there is a higher frequency, it results in higher short-time ZCR, and if there is a low-frequency signal, it results low short-time ZCR.

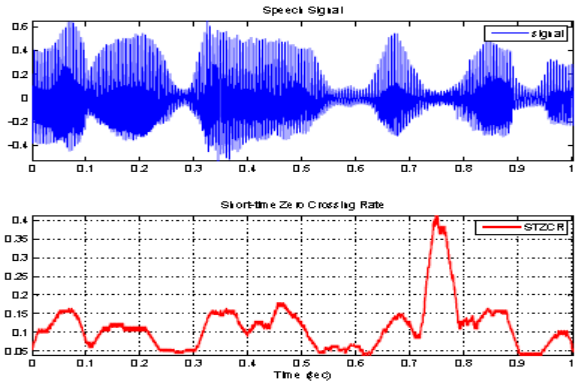

Figure 1. Speech signal and its short-time zero crossing rate for a single female speaker.

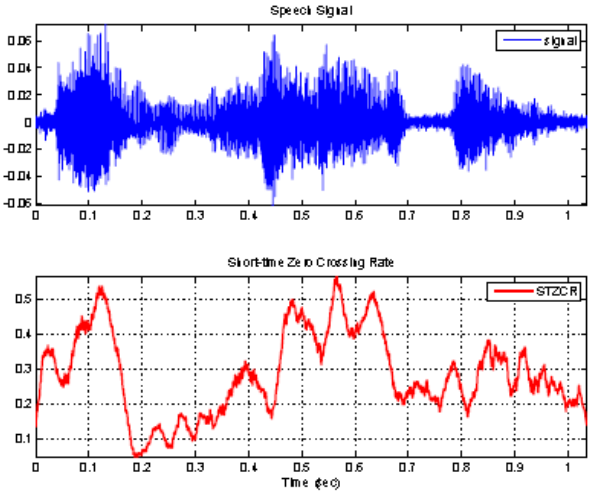

Figure 2. Speech signal and its short-time zero crossing rate for a single male speaker.

Zero crossing rate (ZCR) means the number of times the signal level crosses 0 during a constant period of time (i.e 1sec.) and is used not only for speech but also used for different detection applications. Similarly to amplitude level, a ratio of the input frame to noise is used for this feature. For this application rate at which zero crossing happens was calculated by taking a window of 20 msec. For an illustration, we show a single female speaker speech signal and its corresponding ZCR in Figure 1. Here the first Figure is a speech signal and the next Figure is a short-time zero crossing rate (STZCR). Similarly, we show a single male speaker and mixing of two male speaker speech signals and its corresponding STZCR in Figure 2 and Figure 3.

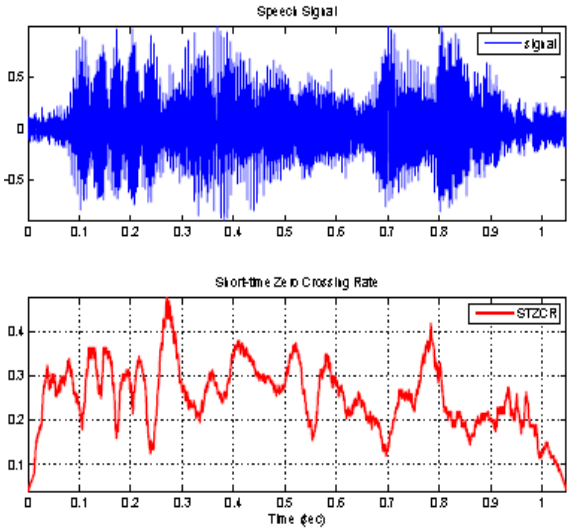

Figure 3. Speech signal and its short-time zero crossing rate for mixing of two male speakers

2.2. Cepstrum Resynthesis Residual Magnitude (CRRM)

CRRM is outlined as the L2-norm of the distinction between the absolute of the smoothed spectrum (M) and the Short Time Fourier Transform spectrum (S) evaluated at a speech sound frame. M is calculated using the real cepstrum (C):

$$C = real(FFT^{-1}(\log(|S|))) \tag{4}$$

$$C^1 = C.W \tag{5}$$

$$M = \exp(FFT(C^1)) \tag{6}$$

Here W is a window function with value 0 or 1. Only the first 'n' coefficients and the latest 'n' coefficients of C are considered. A 1048-point Fast Fourier Transform is performed on C and an 8 kHz sampling rate with n = 50 is used. M is basically a low pass filtering of the spectrum (S), so that is a better fit for noise signals than for harmonic signals is obtained.

4. METHODOLOGY

The Sequence of steps in the proposed method for detection of a single speaker or multi-speaker is shown in Table 1. The speech signal was first split up into non-overlapping short-term windows (frames) of 20 msec. length. The updated and calculated zero crossing rate for every entering sample, using M = 256 rectangular window samples corresponds to 20 msec. with 8 kHz sampling rate. For instance, the authors in [19] calculate 2 ZCRs, first one is for the far-field speech signal and the other is for the near-field speech signals that are then compared to the happening of multiple speakers. For a given input speech signal, the ZCR was calculated using equation (1). From Table 1, it was observed that if the input speech signal has a single speaker, the number of zero crossings is less. Similarly from Figure 2 and Figure 3, it was clear that if the input speech signal has multiple speakers, the number of zero crossings is high. In this study, we considered two speakers data as multiple speakers data for the analysis and evaluation of the proposed method. Based on this logic, we implemented Multi-Speaker activity (MSA) detection method shown in Table 1.

Table 1. Algorithm: Steps for incorporating multi-speaker activity detection

[1]. Record the Speech signal
[2]. Read the Normalization of the speech signal
[3]. Perform the segmentation (window) for the normalization of the speech signal
[4]. Compute the ZCR and slope
[5]. Assign the average Zero crossing (ZC) value is equal to the Zero crossing threshold(ZCTH) and average slope value as STH
[6]. If (ZC value < ZCTH) and (slope < STH) \ * ZCTH=500 and STH= 6 */
Mode= Single Speaker
else
Mode= Multi-Speaker

5. EXPERIMENTAL RESULTS

The performance of zero crossing rate methodology is decided by the parameters threshold (Th), K, and M. A window length M which is smaller contributes to less smoothening and there is every possibility to take incorrect decision. A larger window contributes to a smoothened ZCR and assists in overcoming any error as ZCR is nearer to the threshold, particularly in identifying the actual begin and end of regions. Experimental results proved that 256 samples sized window is more suitable. When ZCR gets updated the K parameter defines the number of samples. Once zero crossing rate is changed by every entering sample, usually K equal to 1 is expected. M bits are required, if K is equal to 1, to cache M zero crossing choices. Computational savings and memory are created when K exceeds 1 is selected. Lastly, the Th value is rigorously selected to prevent any warning or misdetection. Throughout this study, signals that are tested proved that, when window size M = 256 is more suitable for the threshold = 500.

Table 2. Number of zero crossings on number of speakers with gender

Number of speakers	ZCR
single male	398
single female	464
Two male (mixing of two signals)	763
Two female (mixing of two signals)	915
single male + single female (mixing of two signals)	837

The result of the study has been presented in Table 2. Here, the recognition rate is outlined as the ratio of the number of relevant speakers identified to the total number of speakers tested. The percentage of a correctly classified speech signal is given in Tables 3, 4, 5 and 6 respectively. Table 3 shows performance obtained when using the features for male speakers. Table 4 presents performance obtained when using the features for female speakers. Table 5 shows performance obtained when using features for mixed speakers. Finally, Table 6 shows that the performance comparison of the proposed ZCR method is compared with the cepstrum resynthesis residual magnitude (CRRM) method. Considering the three Tables, the differences in terms of recognition rate between the cross-testing are small, indicating that the classification scheme in use as a good generalization behavior. The results are also compared with CRRM of the speech signal. It is observed that slope with zero crossing rate (ZCR) outperforms the CRRM.

Table 3. Recognition rate for male speakers

No. of speakers	Recognition rate (%)
Single	85.51%

Multiple	87.72%

Table 4. Recognition rate for female speakers

No. of speakers	Recognition rate (%)
Single	86.38%
Multiple	89.95%

Table 5. Recognition performance for male-female (mixed) speakers

No. of speakers	Recognition rate (%)
Single	83.71%
Multiple	89.89%

Table 6. Comparing the Performance of proposed method with an existing method

Measure	Male	Female	Mixed
ZCR+Slope	86.61%	88.16%	86.6%
CRRM [1]	82.18%	83.75%	79.08%

6. CONCLUSIONS

In this work, we have presented a feature extraction methodology for slope at ZCR for multi-speaker activity detection and discussed with other existing feature extraction techniques. The zero crossing rates are very easy to calculate and proved that as an efficient discriminant of multi-speaker activity detection. The 3 parameters M, K, and Th are simple to modify and need a nominal tuning. It has also shown improved performance over the single speaker or multiple speakers activity detector. In this paper, finally, it is observed that multi-speaker activity detection using ZCR outperformed with the cepstrum resynthesis residual magnitude (CRRM) method. The results have been presented on the multi-speaker activity detection evaluation.

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TARGET DETECTION USING MULTI RESOLUTION ANALYSIS FOR CAMOUFLAGED IMAGES

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ABSTRACT

Target detection is a challenging problem having many applications in defense and civil. Most of the targets in defense are camouflaged. It is difficult for a system to detect camouflaged targets in an image. A novel and constructive approach is proposing to detect object in camouflage images. This method uses various methodologies such as 2-D DWT, gray level co-occurrence matrix (GLCM), wavelet coefficient features, region growing algorithm and canny edge detection. Target detection is achieved by calculating wavelet coefficient features from GLCM of transformed sub blocks of the image. Seed block is obtained by evaluating wavelet coefficient features. Finally the camouflage object is highlighted using image processing schemes. The proposed target detection system is implemented in Matlab 7.7.0 and tested on different kinds of images.

KEYWORDS

Canny edge detection, Region growing, seed block, Wavelet decomposition

1. INTRODUCTION

Target detection in camouflaged images is one of the most important applications of computer vision. Target detection in camouflaged images is an approach by which we identify one or group of target objects in scene. It is very easy for a human to identify different objects in image but it's difficult for a computer program to identify different objects [2]. In target detection in camouflaged images, images are of different types such as visual, Aerial, IR, etc and they are under different categories (stationary target, moving target) and environments (atmospheric turbulences). It is difficult for a computer program to detect target in these restrictions [3]. Till now so many researches are going on this approach. Some of those approaches [8] are like using pattern recognition, wavelets, texture, connectivity component based approach, descriptors based methods and traditional thresholding methods so on. In developing a system, there are many difficulties like recognition accuracy, occupation of size (image) and execution time so on. These are the things that motivated me to solve some of those issues. My concentration is towards the approach that based on wavelet decomposition and wavelet coefficient features.

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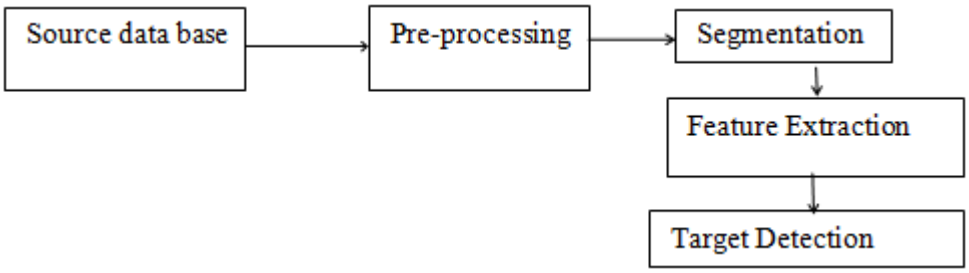


Figure 1. Simplified model for target detection system

The approach of this paper is to build a constructive approach for target detection in camouflaged images that recognize the targets in different kinds of images. To make a system that can able to take images of any size, colour or gray, and related to different environments. It should able to detect targets of any size and in any environment. Target detection in camouflaged images can be done using several approaches; a simplified model is shown in figure 1. Wavelet transform is chosen as it is one of the novel techniques for solving target detection problem.

Camouflage is a natural phenomenon of many animals in the nature. It is an advantage to them, so that they can protect themselves from their enemies. The similar camouflage technique is used in military applications. Generally in military applications, camouflage paint patterns are used for concealing soldiers and their equipment from being detected by the enemy, making them appear to be part and parcel of the natural environmental conditions surrounding them. The extent to which we can camouflage will only be limited by our imagination. Different items are used for these purpose but the ones that standout are face painting, leaves also some fabrics are dyed in shades of green, tan, black, brown so as to make the wearer indistinguishable from the surroundings. Wearer may be a human being, or any other equipment.

Different camouflage paint patterns are used depending on the seasonal changes and the type of terrain used. The standard camouflage colors are blue, regular, desert and woodland. From these basic colors we can come up with desert sand, forest green, light green, white, earth yellow among other colors. Colors should always be chosen from the base color followed by the highlights. The surrounding areas will always determine the type of pattern and colors to use.

2. SCOPE OF APPROACH

Under different types of atmospheric turbulences and different kinds of targets under different environments with the help of seed blocks it is possible to recognize the objects in images. So all these approaches are characterize with the help of multi resolution analysis, similarly by the technique of canny edge detection invented by canny is using to extract the edges of target in the camouflaged kinds of images as explained above.

3. SELECTED METHODS

There are many methods provided by researchers for recognition of objects. In those few of methods are met their requirements. Based on the advanced computer vision approaches here we

suggested the approach like using multi resolution analysis with traditional edge detection and seed block approaches.

Filter bank structure is the simple implementation of 1-D DWT, whereas image processing applications requires two dimensional implementation of wavelet transform [4]. Implementation of 2-D DWT is also referred to as „multidimensional" wavelet transform. The multiresolution analysis as shown in Figure 3.1 This process continues until some final scale is reached.

Figure 3.1: (a) One level wavelet transform (b) Two level wavelet transform

From the obtained gray level co-occurrence matrix, significant wavelet coefficient features (WCFs) preferably contrast, cluster shade, and cluster prominence are evaluated [1]. The features are selected for logarithmic normalization on their dynamic range of values. Several parameters associated with the co-occurrence matrix are contrast, energy, entropy, cluster prominence, cluster shade, and local homogeneity. As we know how the GLCM from the Harlick suggested method. From the obtained gray level co-occurrence matrix, significant wavelet coefficient features are computed using the formulae given below [2]

Coming to the edge detection technique the traditional technique is The Canny edge detection operator was developed by John F. Canny in 1986 this method works better compared to sobel and prewitt operators. The Canny edge detection algorithm is known to many as the optimal edge detector. Canny proposed some criteria to improve the earlier edge detection methods. An image and its canny detected image are shown in the following figures 3.3.

Figure 3.3: Original and Canny edge detected image

4. PROPOSED METHOD

Identification of object in camouflaged images is a difficult approach due to the stochastic nature of background from the foreground. So traditional approaches and processing schemes is will not provide a satisfactory results due to its randomness in order to solve the problem in camouflage images object identification proposing a constructive approaches witch will overcome the problems in traditional processing schemes. In the proposing approach the results are found to be satisfactory. The block diagram for the proposed Target Detection in Camouflaged images system [1, 2] is given in the **figure4.1** Input image. Similarly the **Process flowchart** shows all the steps involved in this proposed method is shown in **figure 4.2**

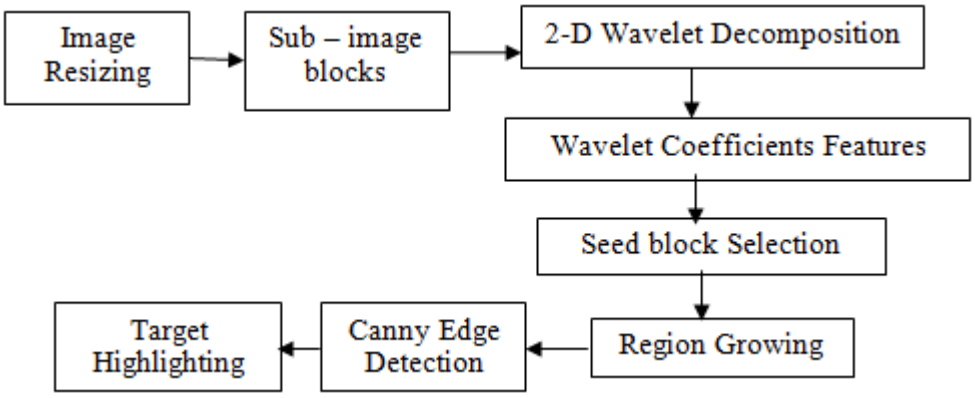


Figure 4.1: Target detection system

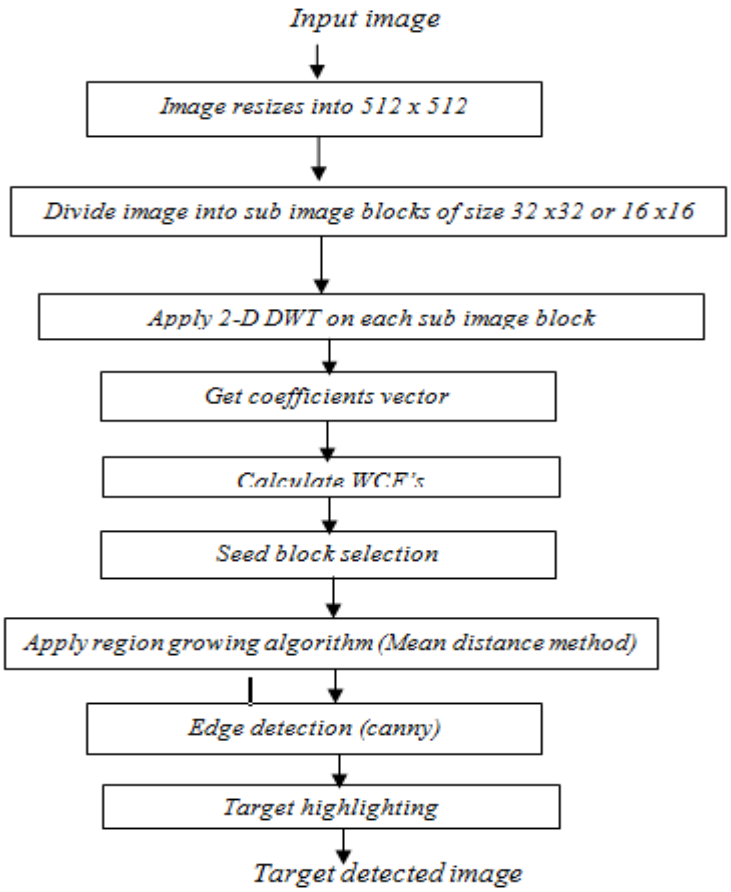


Figure 4.2: Flow chart of proposed target detection system

A. Image resizing:

Consider a camouflage image of different dimensions such that we can divide it into 32 x32 or 16 x16 in the next step. Generally in this system we resizes into 512 x512. If the assumed image is color image convert it in to gray scale image for better processing. Then in the further steps we can process easily and able to calculate GLCM [7]. It is shown in the figure 4.3.

(a) (b)

Figure 4.3: (a) Original image of size 356 x 355 x 3, (b) Resized image of size 512 x512

B. Making sub image blocks:

This proposed system works on the principle of fixed window size technique. If image is resized into 512 x512, and if we divide into sub images of each size 32x32, we get 256 sub images. If we divide into 16 x16, we get 512 sub images. Block size depends up on the dimension of the object and the image.

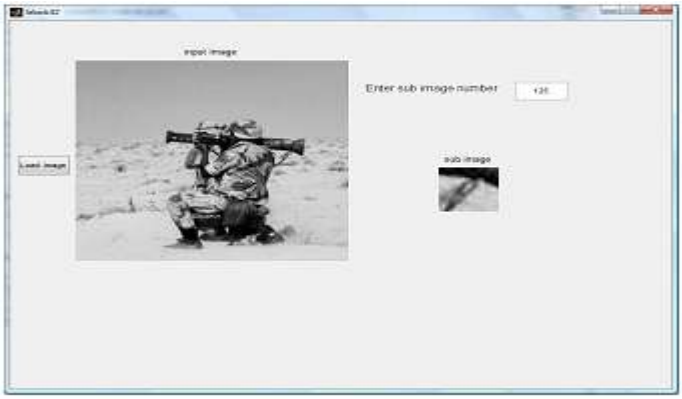


Figure 4.4: Sub image block

Once sub images are obtained, we have to process each sub image separately in the further steps. Finally we have to select seed block i.e., sub image block having the highest sum of wavelet coefficient features. Using the seed block, processing techniques are used to detect the target

C. DWT Decomposition:

After dividing input image into sub image blocks, each sub image block is decomposed using 2-D DWT. Different wavelets are there to apply such as Haar, Daubechies, Meyer, Morlett and Symlets. In the proposed method Daubechies wavelet is used which is of order 2. It is represented as db2. If the size of sub block is more the level of decomposition is to be large in number if it is not so then small number level of decomposition is enough for multi resolution analysis purpose. Level of decomposition is 2 for this system. After decomposition, we get wavelet coefficients. The lower level in decomposition gives coarse level of coefficients which means approximation coefficients and higher levels give finest scale wavelet coefficients which means detail coefficients.

If image is resized into 512 x 512 and divided into sub images of size 32 x 32, 256 sub images are obtained. Then after applying DWT decomposition 256 wavelet coefficients vectors are obtained.

D. Feature extraction:

From the transformed sub block of camouflage image features are evaluated by statistical means to find the seed block details from set of sub blocks to process further. The feature are calculating

by using gray level co-occurrence matrices which is a statistical model based on the probability of occurrence of gray tone values. The statistical features based on GLCM which are cluster prominence, cluster shade and contrast used to evaluate seed block from a set of sub block. The seed block is identified by highest sum of statistical features in each sub block.

Region growing process:

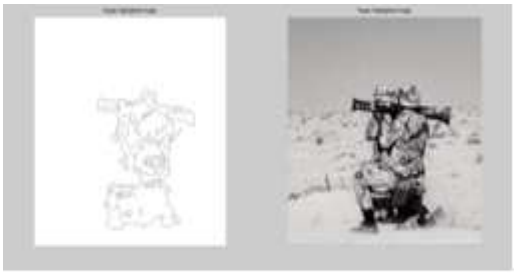
Region growing is a region based segmentation process in which sub regions are grown into larger regions based on predefined criteria such as threshold and adjacency. In developed approach, the region growing algorithm is based on mean distance method [1].

In this method, the first step is to sort the feature values of all the windows, that is, sub image blocks in ascending order so that the window whose value is the largest would be the seed window. The threshold is determined by finding the average (A) of the first n% of the windows, which are adaptively chosen depending upon the target image. Now, the statistical feature values like (cluster details and contrast) of all the 8-adjacent blocks are compared with the average value, A, and the S_{high} value. The window whose value is closer to S_{high} (obtained from the seed block) value will be merged with the seed window. This process is repeated for all 8 adjacent blocks. If no window is merged from the 8 adjacent blocks, then the algorithm terminates. If at least one window is merged from the 8 adjacent blocks, then the above procedure will be repeated with the 16 adjacencies and so on.

Figure 4.5: Image after applying region growing process.

E. Edge detection and Target highlighting

Canny edge detector was one of the good edge detection technique to extract edge information. Now we apply canny edge detection algorithm to find the edges in the region grown image. It will give all the edges present in the region grown image. It gives edges of the target in the scene. This step is used to highlighting step. Image after applying canny edge detection is shown in the figure 4.6



(a) (b)

Figure 4.6: (a) Canny edge detected image (b) Target highlighted image

Canny edge detected image is presently in gray level type. This is converted to indexed image and then converted to RGB image. Then it is added to the original image to highlight the target in the scene.

5. SIMULATION RESULTS

The simulation of the proposed Target Detection in Camouflaged images system is simulated on Matlab 7.7.0 (R2008b). The proposed approach is tested on different kind of images, which are of different sizes and in different environments. The input images may be colour or gray scale and are of any resolution. These images contain different type of targets such as camouflaged soldiers in war environment, camouflaged tankers, aero planes, birds and statues

1. Camouflaged soldiers in war environment
2. Camouflaged soldier in green fields

The simulation result for image 1 is discussed in the previous section. Now the simulation result for image 2 is explained here. For every input image we have resized image, target extracted image, Canny edge detected image, target highlighted image. Sizes of original image, resized image, seed block, seed point (x, y) are calculated. Profiles of wavelet coefficient features such as cluster features and contrast are shown. Details of the seed block (sub image block) are given

1. Camouflaged soldiers in green fields

This is an image contains a soldier camouflaged (disguised) in green fields. For this wavelet coefficient features are calculated and then seed block is found. Details of the seed block are given and its sub image block is shown.

Size of the original image = 180 x 150 x 3
Size of the resized image = 512 x 512

(a) (b)

Figure 5.1: (a) Original image of size 180 x 150 x 3(b) Resized image of size 512 x512

A. Wavelet coefficient features

After applying wavelet decomposition to all sub image blocks, we get coefficients vector. Gray level co-occurrence matrix is calculated from transformed coefficients. Then statistical features are evaluated for further processing techniques

Now WCF‟s are calculated for all the sub image blocks and they are plotted as above. Contrast is normalized linearly and the other two are normalized logarithmically. Sub image with maximum of the sum of the features is treated as a seed block. Seed point is the centre point of the seed block. Seed point is used in the region growing algorithm. Now WCF‟s are calculated for all the sub image blocks and they are plotted as above. Contrast is normalized linearly and the other two are normalized logarithmically. Sub image with maximum of the sum of the features is treated as a seed block. Seed point is the centre point of the seed block.

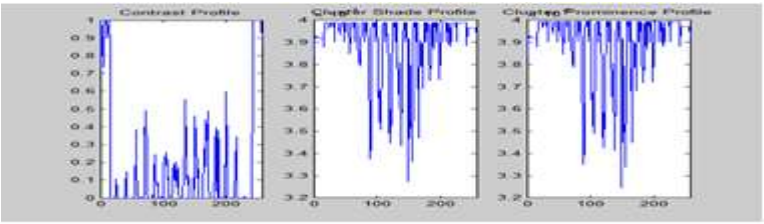


Figure 5.2: Profiles of wavelet coefficient features

B. Seed block details:

Figure 5.3: GUI of Seed block

Seed block = 242th sub image block
Seed point on the resized image = (497, 49)
Wavelet coefficient features for the seed block shown above:
Contrast = 490
Cluster_shade = 2.2379e+011
Cluster_prominence = 3.0319e+014

C. Region grown, canny edge detected, and target highlighted image:

Figure 5.4: Region grown image

Figure 5.5: Canny edge detected image

Figure 5.6: Target highlighted image

D. Tabulations:

Proposed Target Detection in Camouflaged images system is implemented on Matlab7.7.0 (R2008b) and tested on these images. All these information is calculated in the above shown simulation. Seed block number, seed point and wavelet coefficient features for different images are tabulated as shown in the table given below:

S. No	Image	Seed Block	Seed Point	Contrast	Cluster shade	Cluster promin- ence
1	Camouflaged soldiers in war environment	107	(209, 337)	750	1.2827e+011	1.4436e+014
2	Camouflaged soldier in green fields	242	(497, 49)	490	2.2379e+011	3.0319e+014

The proposed method is tested on different kinds of images in different environments

1	Aero plane	103	(209, 209)	47	1.9077e+011	2.4506e+014
2	Bird	106	(209, 305)	202	2.5880e+011	3.6802e+014
3	Statue	1 70	(337, 305)	77	1.6634e+011	2.0414e+014
4	Ship	217	(433, 273)	446	9.4556e+010	9.6129e+013

6. CONCLUSIONS AND FUTURE SCOPE

The proposed techniques for detecting targets in camouflaged images and is tested on different kinds of images. Wavelet based approach is adapted to encounter the multiresolution analysis problem in images like camouflaged images due to randomness in scene. Statistical features are used as performance metrics in this implementation. These metrics are very useful in the object detection for camouflaged images. Canny edge operator is appropriate to detect the edges of the extracted image. The proposed system is implemented on Matlab 7.7.0 (R2008b). Performance of the algorithm is tested on images of arbitrary sizes, gray or colour, and related to different environments and the results are convincing. In future, the proposed method can be extended further at different steps. After resizing the original image, we can divide into sub image blocks of different dimensions according to the size of the object. Based on the features of the obtained target we can classify it. It can be extended to detect multiple targets in an image. Performance of the algorithm can be assessed by changing the wavelets and level of decomposition.

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Intentional Blank

GLAUCOMA DISEASE DIAGNOSIS USING FEED FORWARD NEURAL NETWORK

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ABSTRACT

Glaucoma is an eye disease which damages the optic nerve and or loss of the field of vision which leads to complete blindness caused by the pressure buildup by the fluid of the eye i.e. the intraocular pressure (IOP). This optic disorder with a gradual loss of the field of vision leads to progressive and irreversible blindness, so it should be diagnosed and treated properly at an early stage. In this paper, thedaubechies(db3) or symlets (sym3)and reverse biorthogonal (rbio3.7) wavelet filters are employed for obtaining average and energy texture feature which are used to classify glaucoma disease with high accuracy. The Feed-Forward neural network classifies the glaucoma disease with an accuracy of 96.67%. In this work, the computational complexity is minimized by reducing the number of filters while retaining the same accuracy.

KEYWORDS

Glaucoma, IOP, Wavelet transform, Texture features, Feed Forward neural network, Fundus images

1. INTRODUCTION

Glaucoma is found to be the second leading cause of irreversible visual loss and global blindness. Over the past decade, millions of cases of blindness have increased worldwide,gradually, of which 12.3% are of glaucoma. It has been estimated that nearly 80 million individuals around the world will suffer with glaucoma by the year 2020. Glaucoma is an ocular disease which causes progressive and irreversible changes in the visual field loss, optic nerve head, or both. The damage to the optic nerve is usually caused by raising Intraocular pressure (IOP) which is normally associated with increased fluid (aqueous humor) pressure in the eye (above 21mmHg). The first sign of glaucoma is peripheral vision loss which often occurs gradually over a long period of time, so it is often called as "silent thief of sight", and symptoms only occur when the disease is quite advanced which requires early detection to sustain the vision without any further loss.

Different glaucoma detection tests include, Tonometry to determine IOP; Gonioscopy for finding the angle in the eye where the iris meets the cornea; Ophthalmoscopy/Funduscopy, it is a dilated eye examine for obtaining the shape and color of the optic nerve; Visual Field test (Perimetry) to check the missing areas of the field of vision; and Corneal Pachymetry for obtaining the thickness of nerve fiber layer. In this work, Ophthalmoscopy/Funduscopytest is considered asdiagnostic tool for the disease identification. Generally, the retinal fundus images are acquired by dilated eye test by exposing it to the light source and the images are captured using a fundus camera and microscope.

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Many studies have been made for the development of automated clinical decision support systems (CDSSs) in ophthalmology, such as CASNET/glaucoma [1] and [2], which are designed for decision support system for disease identification in the eye.The features that can be extracted from the retinal fundus images which are used in these systems include structural and texture features. The frequently referred structural features are disk, rim and cup areas; disk and cup diameters and also the cup to disk ratio of the optic. The texture features measurement is based on the spatial variations of pixel intensity (gray-scale values) across the image[3]. In thesesystems, the proper orthogonal decomposition (POD) is one of the method that uses structural features for glaucoma identification [4]. The author in [5], used the texture and higher order spectra (HOS) features for glaucomatous image classification, in which HOS derives amplitude and phase information while texture provide measures such as smoothness, coarseness and regularity. The wavelet-Fourier analysis (WFA) [6] is used for obtaining the anatomic changes in the glaucoma where DWT used the symlets (sym4) wavelet filters for feature extraction by analyzing the abrupt changes in the signal while the fast Fourier transform (FFT) is applied to the detailed components, whose amplitudes are combined with the DWT normalized approximation coefficients to form the feature set.

The aim of this work is to automatically classify normal and glaucomatous eye images based on the wavelet based average and energy texture features obtained by applying the two wavelet family filters. Hence, the objective is to evaluate and select the potential features for improved specificity, sensitivity, precision and accuracy of the glaucomatous image classification. The proposed work uses the well-known wavelet family filters, the daubechies (db3), symlet (sym3) and reverse biorthogonal (rbio3. 7) combination filters are used to compute the wavelet average and energy features of the detailedcoefficients. The features which exhibits p-value < 0.0001 are chosen and are subjected to z-score normalization to aid the convergence of feed forward neural network classifier. The paper is organized in the following way. Section 2 contains an explanation of the dataset. Section 3 contains a detailed description of the steps involved to detect glaucoma disease. Section 4 contains implementation and results along with the performance parameters employed in proposed methodology. In the end, the paper concludes with Section 5 with a conclusion.

2. DATASET

The fundus images of the retina used for this work are obtained from DRIVE and STARE databaseswhich are publicly available. All the images with resolution of 512 x 512 are taken in lossless JPEG format. The whole dataset comprises of30 digital fundus images of which 15 are normal, which are taken from the DRIVE and other 15 are glaucomatous images taken from STARE database. The resulting retinal image shows the optic nerve, fovea, and the blood vessels. Figure 1 (a) and (b) representsnormal and glaucoma images, respectively.

(a) Normal (b)Glaucoma

Figure 1.Retinal Fundus Images

3. METHODOLOGY

The dataset containing all the images were initially preprocessed by subjecting them to standard histogram equalization. The processed images are then subjected to the following detailed procedure for feature extraction, feature selection and classification as shown in Figure 2.

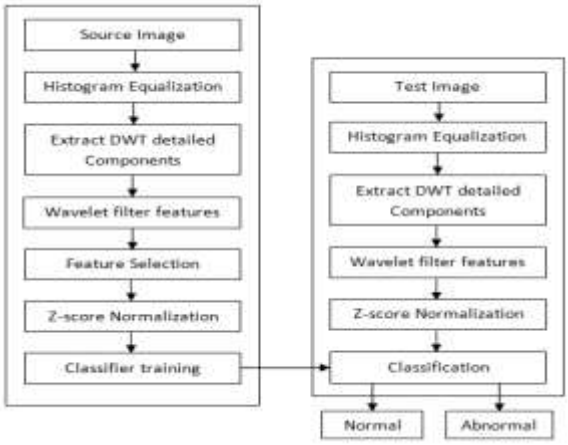

Figure 2. Flow of the methodology

3.1. Preprocessing of images

The dataset containing 30 images are preprocessed using standard Histogram equalization [7]. It is an image enhancement process and is required as the images are obtained from different subjects which have different orientations and intensity values so it is used to specify the input image pixel's intensity values, such that the output image contains intensity values which are uniformly distributed and also, the dynamic range of the image histogram is increased.

3.2. Discrete Wavelet Transform based features

Two dimensional Discrete wavelet transform (2D-DWT) is applied to the dataset to obtain the approximate and detail coefficients used for wavelet feature extraction. The one-level decomposition structure of an image of size m x n would result in four subimagesA1, Dh1, Dv1 and Dd1 each of size m/2 x n/2 resolution and preserved scale.Here, the well-known wavelet family filters daubechies (db3)and reverse biorthogonal (rbio3.7) or symlets (sym3) and reverse biorthogonal (rbio3.7) combination filters are used for the feature extraction. Since the wavelet coefficient matrices obtained have a number of elements, to represent a feature in this work only a single value is required in orderto decrease the computation. Thus, these single-valued wavelet features are determined based on the averaging method using the DWT detailed coefficients are given by equations (1), (2) and (3) by averaging the intensity values. The equations (1) and (2) give the average features, while (3) gives the energy features. Here, p x q is the size of the subimages.

$$Average\_Dh1 = \frac{1}{p*q}\sum_{x=\{p\}}\sum_{y=\{q\}}|Dh1(x,y)| \quad (1)$$

$$Average\_Dv1 = \frac{1}{p*q}\sum_{x=\{p\}}\sum_{y=\{q\}}|Dv1(x,y)| \quad (2)$$

$$Energy\_Dv1 = \frac{1}{p^2*q^2}\sum_{x=\{p\}}\sum_{y=\{q\}}(Dv1(x,y))^2 \quad (3)$$

3.3. P-values

In this proposed work, 6 average and energy features each are extracted from the wavelet transformed fundus eye images for both the db3 & rbio3.7 and sym3 & rbio3.7 combination filters. Among them, 6 features were chosen out of 12 features as it was proven to be clinically significant by using the p-value method which are same for both filter combination are tabulated in Table 1. P-value method is a non-traditional statistical method used for hypothesis testing by comparing the two sample averages. In general, a p-value is the probability measure to determine the two mean differences which happened by chance.The statistical hypothesis is as follows:

$$H_n: \mu_1 - \mu_2 = 0 \qquad (4)$$
$$H_a: \mu_1 - \mu_2 \neq 0$$

where, H_n is the Null hypothesis which is the mean of the normal samples is the same as the mean of the Glaucoma samples and H_a is the alternative hypothesis which is the mean of the normal samples is different than the mean of the Glaucoma samples. μ_1 and μ_2 are the means of normal and glaucoma samples.

Table 1. Selected Features

Features	Normal	Glaucoma	P-Values
db3_Dh_Average	6.6415±0.8642	4.3.088±1.0183	<0.0001
db3_Dh_Energy	0.0008±0.1758E-03	0.3620E-03±0.1493 E-03	<0.0001
db3_Dd_Energy	0.0001±0.0383 E-03	0.0741E-03±0.0345 E-03	<0.0001
rbio3.7_Dh_Average	9.4660±1.2445	6.0005±1.4257	<0.0001
rbio3.7_Dh_Energy	0.0015±0.3525 E-03	0.7278E-03±0.3145 E-03	<0.0001
rbio3.7_Dd_Energy	0.0008±0.1958 E-03	0.4031E-03±0.1886 E-03	<0.0001

A two-sample t-test calculates the test statistics using equation (5) and (6) to estimate whether the mean of each of the average and energy features has significant clinical difference between the two groups, as

$$t - stat = \frac{\overline{y_1} - \overline{y_2}}{\sqrt{std_p^2\left(\frac{1}{n_1} - \frac{1}{n_2}\right)}} \qquad (5)$$

$$std_p^2 = \frac{(n_1-1)s_1^2 - (n_2-1)s_2^2}{n_1+n_2-2} \qquad (6)$$

where, $\overline{y_1}$ and $\overline{y_2}$ are the means of the each class sample and n_1 and n_2 represents the sample sizes and $std_p$is the pool variance given as follows with s_1 and s_2 are the variances of the classes. Using the t-statistics, the p-value is calculated which is the area under the t-distribution curve past the t-stats are compared with the level of significance (α=0.0001), the lower the p-value indicates that there is a clinical significantly greater difference between the two classes. Generally,H_n is rejected, if the p-value<0.0001 corresponding to 0.01% chance of null hypothesis being true. Hence, for further analysis the features which exhibit p-values less than 0.0001 are selected.

3.4. Z-score Normalization of features

The z-score is a normalization process used for rescaling the features i.e. the average and energy feature into the same units. The 6 features selected are normalized using z-score normalization. In this process, a vector sample consisting of 6 features is transformed to unit variance and zero mean. The z-scores are computed using equation (7) with v_{old} as the original value in the vector

and $v_{new}$is its obtained new z-score value, and m and Std are the mean and standard deviation of the original data range, respectively.

$$v_{new} = \frac{v_{old} - m}{Std} \tag{7}$$

3.5.Classification - Feed Forward Neural Network

A network structure having only the advancing flow of information without any feedback is called a feed forward neural network(FFNN) [8]. One of the most widely preferred is multi-layered feed forward network with back propagation shown in Figure 3, as a single artificial neuron cannot model well for classifications that are non-linearly separable.

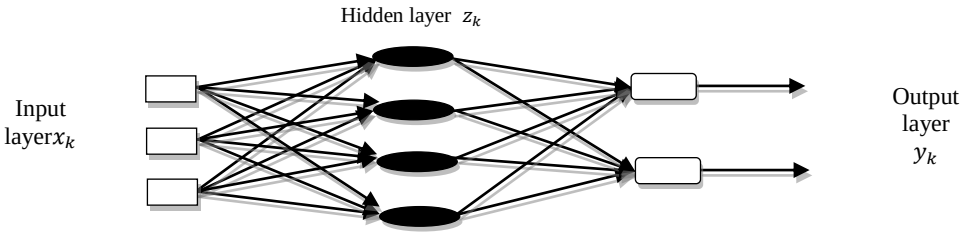

Figure 3.Multi layered feed forward network architecture

In this work, the features which are extracted are non-linear and are to be classified, so multi layered neural network is employed. From the figure it is clear that the network architecture has three layers that are input layer, hidden layer and output layer, where the hidden layer can be of any number depending upon the user usage,which can compute the input representation that will make the problem more linearly separable. This multi-layered network uses extended gradient-descent based delta-learning rule, commonly known as a back propagation rule as training algorithm. The training is performed by using a supervised learning technique, where back propagation is used for altering the weight using an activation function for learning a training set has been proved to be computationally efficient method and the total mean squared error of the weights are minimized using the gradient descent method.During this training process an iterative based flow of training data is followed for the weight vectors establishment, using which the network learns to identify particular classes by considering the characteristics of the input trained data and the backward links are present during training only. Finally, the activation function used is a linear sigmoid function, using which the output is as specified:

$$y = f(x) = \frac{1}{1+ e^{-x}} \tag{8}$$

Using the sigmoid activation function binary classification can be performed as it will squash allthe output values between 0 & 1, such that the neuron will always be positive, bounded and is strictly increasing. The errors in the output nodes are propagated backward through the network after each training case and the system adjusts the weights of the net so that the total mean squareerror calculated using the delta rule is minimized. Once the system is optimized by training with the input pattern to obtain the trained features, the test images can be given which follow the same procedure, except the backward links, for detection of the image class i.e. glaucoma or normal retinal images can be achieved by categorizing them as either 0 or 1.

4. IMPLEMENTATION AND RESULTS

The proposed method for glaucoma detection was tested on a publicly available DRIVE and STARE database. The 6 wavelet features were extracted from each retinal image (1 x 6 matrix) and thus for the whole dataset a 30 x 6 feature matrix was formed where each row corresponds to each image input and the 6 columns represents the selected features extracted from each image.This input vector of 30 x 6 feature matrix is then fed to the FFNN system with 120 hidden layers and a target matrix as the identity matrix of size 30, since 30 image samples are used to classify the normal and glaucomatous image. Thus, after the network training phase, the test images are given whose features are extracted by undergoing the same procedures and then the trained set features are compared with the test features for classification of glaucoma.

The performance of the system is analyzed by evaluating the 4 parameters Sensitivity (TPR), Specificity (SPC), Positive Predictive Accuracy (PPV) or Precision and Accuracy (ACC) are calculated with respect to the four conditions which form the four entries of the confusion matrix are TP (true positive) for glaucoma is correctly identified, FP (false positive) for glaucoma is incorrectly identified, TN (true negative) for normal is correctly rejected, and FN (false negative) for normal is incorrectly rejected; where positive (P) and negative (N) corresponds to glaucoma and normal case respectively. The test results can be positive or negative corresponding to the identification or rejection of image pattern respectively. The equations for calculating these performance parameters are given below:

$$TPR = TP / (TP + FN) \quad (9)$$

$$SPC = TN / (FP + TN) \quad (10)$$

$$PPV = TP / (TP + FP) \quad (11)$$

$$ACC = (TP + TN) / (P + N) \quad (12)$$

Sensitivity and specificity are both are the measures of the fraction of positives and negatives which wereidentified correctly by the classifier, respectively. Precision determines the fraction of samples that are positive in the group which has been declared as a positive class by the classifier. Accuracy is the whole system parameter which is used as a statistical measure to determine how well a binary classifier identifies or rejects a test sample. A system having 100% sensitivity and specificity is considered as a perfect predictor, evenso, theoretically some minimum error usually exists in any predictor.For the neural network systems, the obtained four conditions and performance parameters are tabulated in the Table 2.

Table 2. Performance parameters comparison

Filter Combinations	TP	FP	TN	FN	TPR (%)	SPC (%)	PPV (%)	ACC (%)
5 - Filters	14	1	15	0	100	93.75	93.33	96.67
2 - Filters	14	1	15	0	100	93.75	93.33	96.67

In this research work an effort is made to reduce the number of wavelet filters to two, while retaining the accuracy of 96.67% for glaucoma image classification using five wavelet filters[10].In the proposed work, the computational complexity is reduced as the number of wavelet filters employed are less. In a two wavelet filter combination daubechies (db3) and reverse biorthogonal (rbio3.7) or symlets (sym3) and reverse biorthogonal (rbio3.7) filters are usedand in the five filter combination includes daubechies (db3), symlet (sym3) and reverse

biorthogonal (rbio3.3, rbio3.5 and rbio3.7) wavelet filters are employed [9][10].The two sets of two filter combinations using daubechies and symlets produces the same accuracy as both have same filter coefficient and filter lengths, so any one of the combination can be employed. These filters are biorthogonal filters with high pass and low pass filter lengths of L_1 and L_2, then the number of additions, A, and multiplications, M, required for performing the filter operations are computed [11] using the equation (13) and (14).These formulas compute the computational complexity of one dimensional signal, in order to calculate for a two-dimensional signal i.e. in case of an image, the formulas are multiplied by 2 to relate to the separable filtering of horizontal and vertical filtering. The complexity comparison for the filter combinations is shown in the Table 3.

$$M=L_1 + L_2 \quad (13)$$

$$A=L_1 + L_2 - 2 \quad (14)$$

The work is implemented using MATLAB. Using a Graphical user interface (GUI), the image is selected for analysis is first preprocessed using histogram equalization and applied to daubechies and reverse biorthogonalwavelet filters. The option feature extraction provides the list of average and energy features which can be extracted from the images. The created GUI has two tables, one corresponding to all the texture features of the images in the database and the other displays the selected average and energy feature based on the p-value criteria as shown in the Figure 4.The classification option is selected to display the classification window to classify the images using the FFNN classifier where the tables shown in the Figure 5 and 6 are the four conditions to calculate the performance parameters. FFNN classifies the dataset images with an accuracy of 96.67%, which is displayed on the GUI by selecting the accuracy option. The GUI also displays a message for glaucoma detection of the input retinal fundus images.

Table 3. Computational Complexity Comparison for 2D signal (image)

Filter Combinations	Computational Complexity		
	Multiplications	Additions	No. of Computations
5 - Filters	72	52	124
2 - Filters	32	24	56

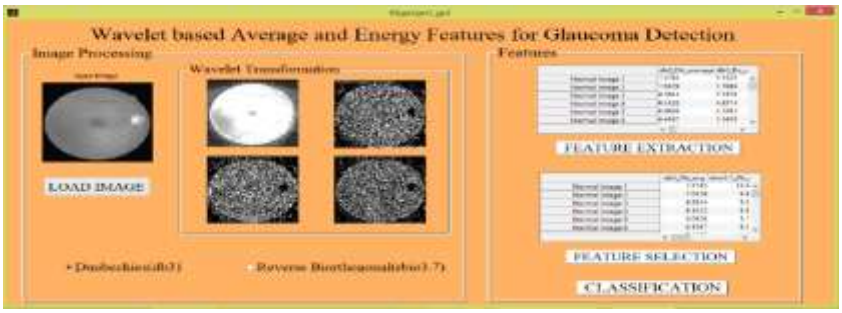

Figure 4. GUI for Glaucoma Detection

Figure 5. Glaucoma Image classification results

Figure 6. Normal Image classification results

CONCLUSION

This study illustrates that the selected features extracted from the two wavelet filters have been fed to a Feed Forward Neural Network. The texture features obtained from the detailed coefficients of the two wavelet filters are used to discriminatenormal and glaucomatous images by retaining the same accuracy of 96.67% as that of five filter combination and also reduces the computational complexity required for the classification

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Intentional Blank

SHIFT INVARIENT AND EIGEN FEATURE BASED IMAGE FUSION

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ABSTRACT:

Image fusion is a technique of fusing multiple images for better information and more accurate image compared input images. Image fusion has applications in biomedical imaging, remote sensing, pattern recognition, multi-focus image integration, and modern military. The proposed methodology uses benefits of Stationary Wavelet Transform (SWT) and Principal Component Analysis (PCA) to fuse the two images. The obtained results are compared with exiting methodologies and shows robustness in terms of entropy, Peak Signal to Noise Ratio (PSNR) and standard deviation.

KEY WORDS:

Fusion, multi-focus image integration, SWT, PCA.

1. INTRODUCTION

Image fusion is for obtaining more accurate information by combination of two or more images. The fusion has many applications like biomedical imaging, air traffic control, robotics, remote sensing, pattern recognition, multi-focus image integration, and modern military environmental monitoring [1].

The image fusion can be achieved in spatial domain or frequency domain. Jiayi Ma et al., proposed a technique of fusing infrared image and visible image. The fusion of two images is depended on Gradient Transfer Fusion (GTF), GTF is a combination of gradient transfer with minimization of total variation. Jiayi Ma et al., are succeeded image fusion without any registration of source images [5]. Yanfei and Nong [6] proposed a multi sensor image fusion technique based on hierarchical multi resolution along with attention. Important areas are identified by using visual attention model and maximum entropy. Based on adoptive weighing rules, first level of fused image is obtained from visible image and infrared image. Finally Non Subsampled Counterlet Transform (NSCT) is used to obtain final fused image. Huafeng Li [7] also proposed for the fusion of multi sensor image combination based on NSCT. Jun Lang and Zhengchao image fusion technique [8] provides less spectral distortion and good spatial resolution based on discrete fractional random transform and adaptive pulse coupled neural network (PCNN).

Principal Component Analysis (PCA) [2] increases the spatial resolution and the flaw is creation of distortion in spectrum in remote sensing image fusion. SWT advantage translation invariance over DWT and DWT advantage is time frequency localization. The paper set as follows, in section 2 proposed methodologies, its flow diagram and information about techniques used

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presented. In section 3, results and performance calculations and analysis are presented. Finally conclusions along with future directions are given in section 4.

2. PROPOSED METHOD

The proposed technique uses the advantage of SWT and PCA. Initially, the input images of any size are registered into same size, and then given to SWT separately. The SWT converts an image into four different subbands A, H, V and D. In figure1 A1 and A2, H1 and H2, V1 and V2, D1 and D2 are approximate coefficients, horizontal details, vertical details, diagonal details of image1 and image2 respectively. The approximate coefficients are fused based on PCA, similarly horizontal details, vertical details and diagonal details also fused individually. After fusion of respective coefficients, the fused coefficients are given to ISWT, which results final required fused image.

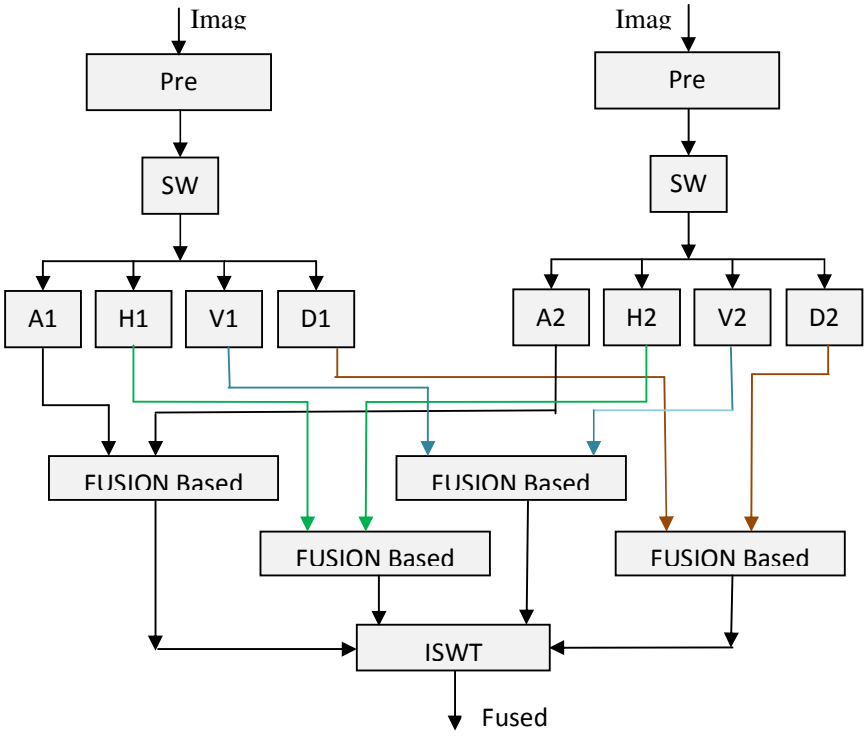

Fig1: Flow diagram of proposed method

2.1 Stationary Wavelet Transform

The drawback in discrete wavelet transform is translation invariance is overcomes in stationary wavelet transform. Due to presence of up-samplers and down-samplers in DWT, it lacks translation invariance and this effect is eliminated in SWT by removing the up-samplers and down-samplers, so SWT also called as Translation invariant wavelet transform. The outcome of SWT consist same number of samples as the input, so it is also called redundant wavelet transform.

2.2 Principal Component Analysis

PCA is a statistical procedure based on orthogonal transformation; to convert set of structure of possible correlated variables into set of linearly uncorrelated variable called "principle components". Output after PCA consists of less number of Eigen features when compared to original input spectral feature. In this method initially need the mean values which is given in Equation (1) of spectral features later Calculate the covariance matrix in Equation (2), based on this covariance matrix find the feature vectors. To find out the Eigen features by using singular value decomposition (SVD) method in Equation (3).

$$E(X) = \frac{1}{k}\sum_{i=1}^{k} x_i \quad (1)$$

$$Cov_i(X) = (X_i - \mu)\,(X_i - \mu)^T \quad (2)$$

$$A = U \sum V^T \quad (3)$$

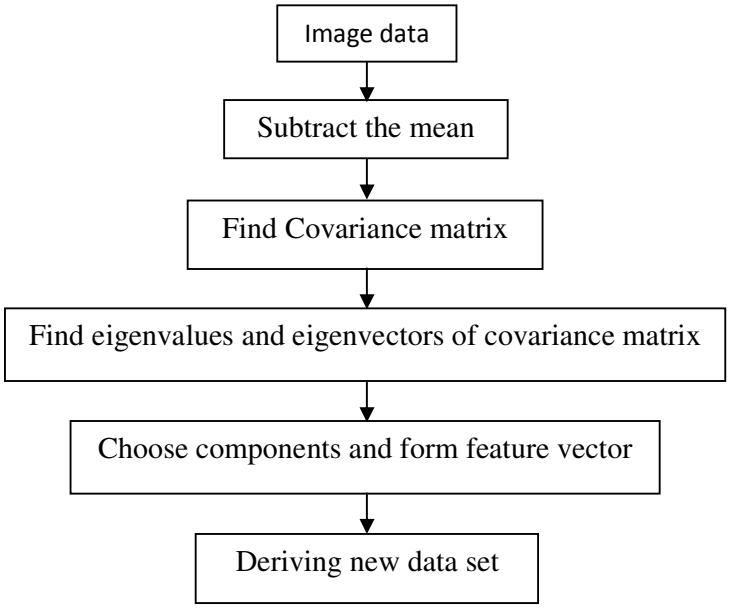

Fig.1 Flow diagram of PCA

1. Results

The results of proposed methodology are displayed in below tables and here the testing database downloaded from standard organizations [9], [10]. Table 1 displays, proposed method results from dataset 1 [10].Table 2 displays, proposed method results from dataset 2 [9]. All the process done on personal computer with RAM 2GB, Matlab version 2013.

Table1: Comparison of Fused results for dataset1.

Image\Measurement	**ENTROPY**			**STANDARD DEVIATION**		
	PCA	SWT	PCA+SWT	PCA	SWT	PCA+SWT
Pair1(DU)	6.25	6.99	7.40	25.62	25.98	29.73
Pair2(NU)	6.08	6.59	7.43	11.99	13.32	15.70
Pair3(FLY)	4.66	4.65	5.68	41.87	42.19	41.89

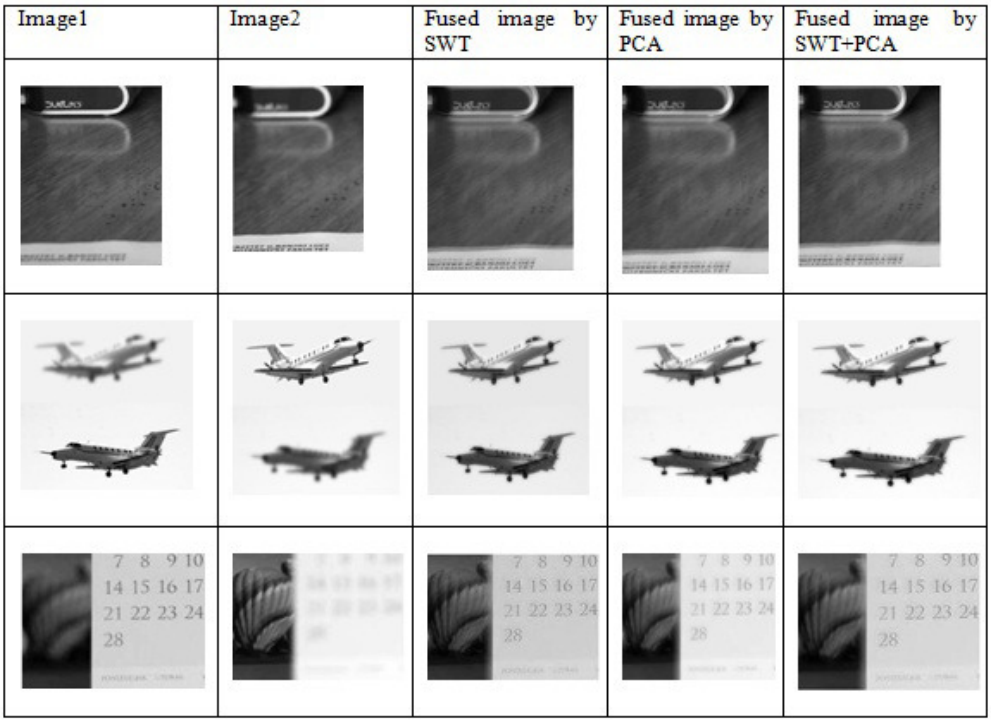

Table2: Comparison of Fused results for dataset2.

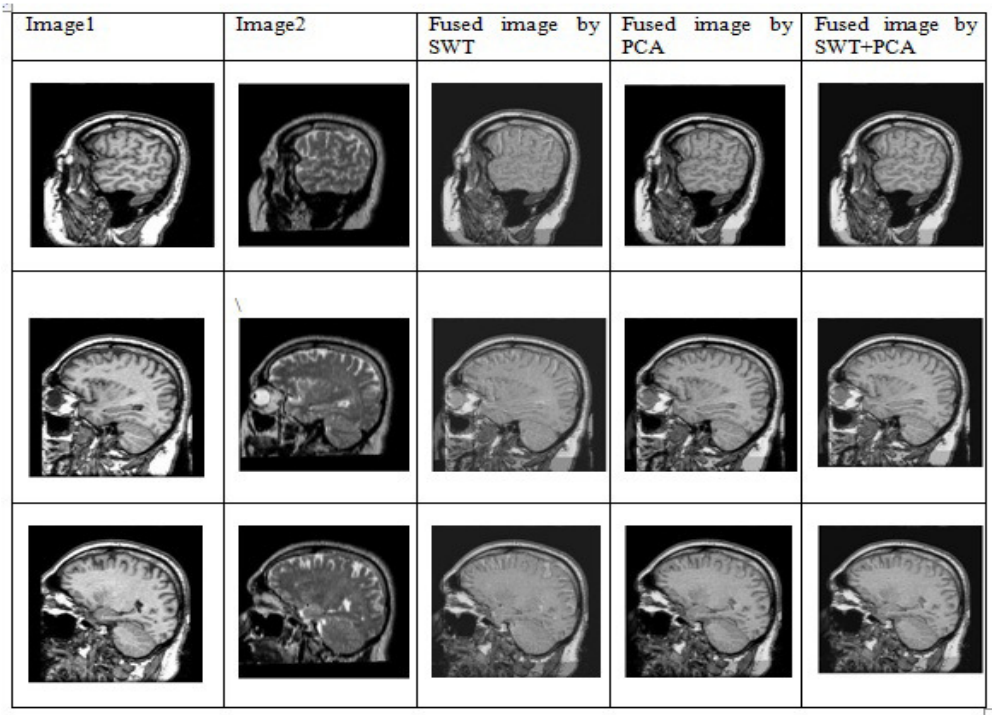

Table3: Performance calculations comparison in PSNR.

Performance Calculations

For testing of proposed methodology, PSNR, Standard Deviation and Entropy are used [4], [3]. The performance calculations are presented in below table3 and table4. PSNR1 represents for peak signal to noise ratio of fused image with image1 and PSNR2 for peak signal to noise ratio with image2.

Image\Measurement	**PSNR 1**			**PSNR 2**		
	PCA	SWT	PCA+SWT	PCA	SWT	PCA+SWT
Pair1(DU)	23.00	22.86	33.60	21.20	21.19	31.80
Pair2(NU)	20.84	27.00	39.27	23.29	17.21	38.98
Pair3(FLY)	26.65	24.19	38.45	26.70	24.23	36.99

Table4: Performance calculations comparison in Entropy and Standard Deviation.

CONCLUSIONS

The proposed fusion methodology is done by the help of SWT and PCA, SWT has the advantage of shift invariance over Discrete Wavelet Transform. The comparative analysis of performance calculations showing robustness over remaining two techniques. The future idea is to fuse infrared images.

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COPY MOVE FORGERY DETECTION USING GLCM BASED STATISTICAL FEATURES

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ABSTRACT

The features Gray Level Co-occurrence Matrix (GLCM) are mostly explored in Face Recognition and CBIR. GLCM technique is explored here for Copy-Move Forgery Detection. GLCMs are extracted from all the images in the database and statistics such as contrast, correlation, homogeneity and energy are derived. These statistics form the feature vector. Support Vector Machine (SVM) is trained on all these features and the authenticity of the image is decided by SVM classifier. The proposed work is evaluated on CoMoFoD database, on a whole 1200 forged and processed images are tested. The performance analysis of the present work is evaluated with the recent methods.

KEYWORDS

GLCM, CMFD, SVM Classifier, Detection rate

1. INTRODUCTION

Digital images have a significant role in conveying the information. Digital Image manipulation became very easy with the availability of advanced photo editing tools. But, due to the manipulation the trustworthiness of digital images is lost. Hence, detection of image forgery is important and is achieved in passive mode without embedding any signature in the original image. Passive image forgery detection works on the discrepancies in the statistical features of the forged image. Copy-Move tampering is a very common method of tampering digital image where in some portion of an original image is copied and pasted at some other location in the same original image. In general, this is done with intent to conceal a region in the image. The copied portions are within the image, so the changes in texture, variations in intensity or any statistical property may match with the remaining portion of the original image. Hence, it is challenging for detecting the forged portion based on HVS [1]. An exhaustive search can be used to identify the significant features of copied and pasted portions on the tampered image. This mechanism needs more time for detection and is computationally complex [2]. Therefore, similarity measure can be used on the identical image regions for detecting the forgery successfully [2]. Figure 1(a) and 1(b) illustrates Copy move forgery.

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a.Original Image b. Copy-Move Forged Image

Figure 1. Illustration of copy-move forgery

A comprehensive report on passive methods for forgery detection in images is available in [3]. Here, the works based on textural features are reviewed. Shikha Dubey et al. [4] used local descriptors for textural features and block matching is performed using clustering technique. In [5], the Gabor magnitude of the image is computed and a histogram is formed as a feature vector. Gabor Wavelets and Local Phase Quantization [6] are used to extract texture features for image forgery detection. In [7], features are extracted based on GLCM and Histogram of Oriented Gradient (HOG) and KNN classifier is used for image forgery detection.

2. METHODS

2.1. GLCM

GLCM is the key process of this work. The Gray Level Co-occurrence Matrix (GLCM) provides information on the occurrence of various combinations of pixel intensities in a gray image. It is a statistical approach [8] of exploring the spatial relationship among pixels. GLCM computes in what a way a pixel with intensity i occur horizontally, vertically or diagonally to a pixel with intensity j.

GLCM exhibits certain properties regarding the spatial relationships of gray intensities in the image.

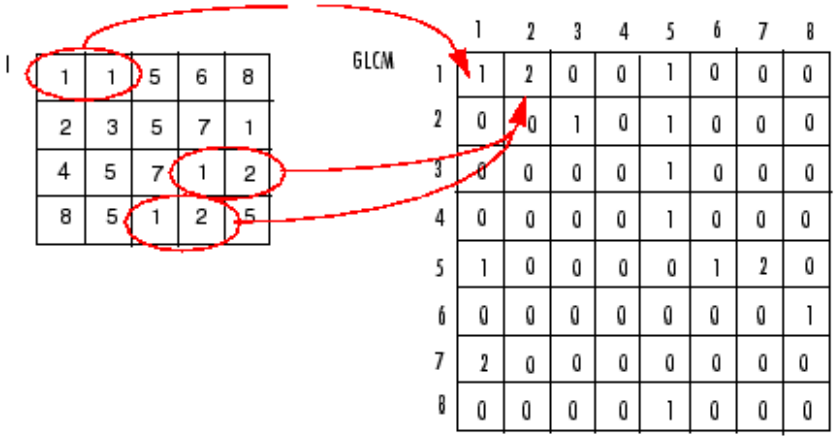

Figure 2. Formation of GLCM

The process involved in GLCM formation is shown in Figure 2. The statistical features that are computed from GLCMs are as follows:

$$Energy = \sum_{i,j} P(i,j)^2 \tag{1}$$

$$Entropy = -\sum_{i,j} P(i,j)\log P(i,j) \tag{2}$$

$$\text{Homogeneity} = \sum_{i,j} \frac{1}{1+(i-j)^2} P(i,j) \tag{3}$$

$$\text{Inertia} = \sum_{i,j} (i-j)^2 P(i,j) \tag{4}$$

$$\text{Correlation} = -\sum_{i,j} \frac{(i-\mu)(j-\mu)}{\sigma^2} P(i,j) \tag{5}$$

$$Shade = \sum_{i,j} (i+j-2\mu)^3 P(i,j) \tag{6}$$

$$\text{Prominence} = \sum_{i,j} (i+j-2\mu)^4 P(i,j) \tag{7}$$

$$\text{Variance} = \sum_{i,j} (i-\mu)^2 P(i,j) \tag{8}$$

$$where\ \mu = \mu_x = \mu_y = \sum_i i \sum_j P(i,j) = \sum_j j \sum_i P(i,j)$$

$$\text{and}\ \sigma = \sum_i (i-\mu_x)^2 \sum_j P(i,j) = \sum_j (j-\mu_y)^2 \sum_i P(i,j)$$

$$\text{Contrast} = \sum_i \sum_j (i-j)^2 P(i,j) \tag{9}$$

$$\text{Angular Second Moment} = \sum_i \sum_j \{P(i,j)\}^2 \tag{10}$$

$$\text{Inverse Difference Moment} = \sum_i \sum_j \frac{1}{1+(i-j)^2} \{P(i,j)\} \tag{11}$$

$$\text{Autocorrelation} = \sum_i \sum_j (ij) P(i,j) \tag{12}$$

$$\text{Dissimilarity} = \sum_i \sum_j |i-j| P(i,j) \tag{13}$$

$$\text{Maximum Probability} = \max_{i,j} p(i,j) \tag{14}$$

$$\text{Sum Entropy} = -\sum_{i=2}^{2N_g} P_{x+y}(i)\log\{P_{x+y}(i)\} \tag{15}$$

$$\text{Difference Variance} = Variance\ of\ p_{x-y} \tag{16}$$

$$\text{Difference Entropy} = -\sum_{i=0}^{N_{g-1}} P_{x-y}(i)\log\{P_{x-y}(i)\} \tag{17}$$

$$\text{Information Measures of Correlation} = \frac{HXY - HXY1}{\max\{HX, HY\}} \tag{18}$$

$$= (1-\exp[-2.0(HXY2 - HXY)])^{1/2} \tag{19}$$

$$\text{Inverse Difference} = \sum_i \sum_j \frac{1}{1+|i-j|} \{P(i,j)\} \tag{20}$$

2.2. Support Vector Machine

Vapnik proposed SVM [9], basically a statistical learning concept. The SVM works on the fundamental principle of inserting a hyperplane between the classes, and it will keep at highest distance from the nearest data points. Data points appear nearest to the hyperplane are defined as Support Vectors. Popular kernels are Linear kernel, Polynomial kernel of degree'd', Gaussian radial basis function (RBF), and Neural Nets (sigmoid). Here, in this work, the RBF kernel is used.

3. PROPOSED METHOD

A Copy-Move Forgery Detection (CMFD) method is proposed using GLCM and SVM. The proposed method is detailed below and is shown in Fig.3.

i. The standard database CoMoFoD consists of original, forged and processed images is considered in the performance analysis.
ii. The images in the database are converted to gray scale.
iii. The statistical features are computed on GLCMs developed from the gray scale images.
iv. The Support Vector Machine is trained with those 20 statistical features for every image in the database using RBF kernel.
v. Statistical features of the testing image are obtained in similar process using steps 2 and 3.
vi. The SVM classifier classifies the image either to be authentic or forged.

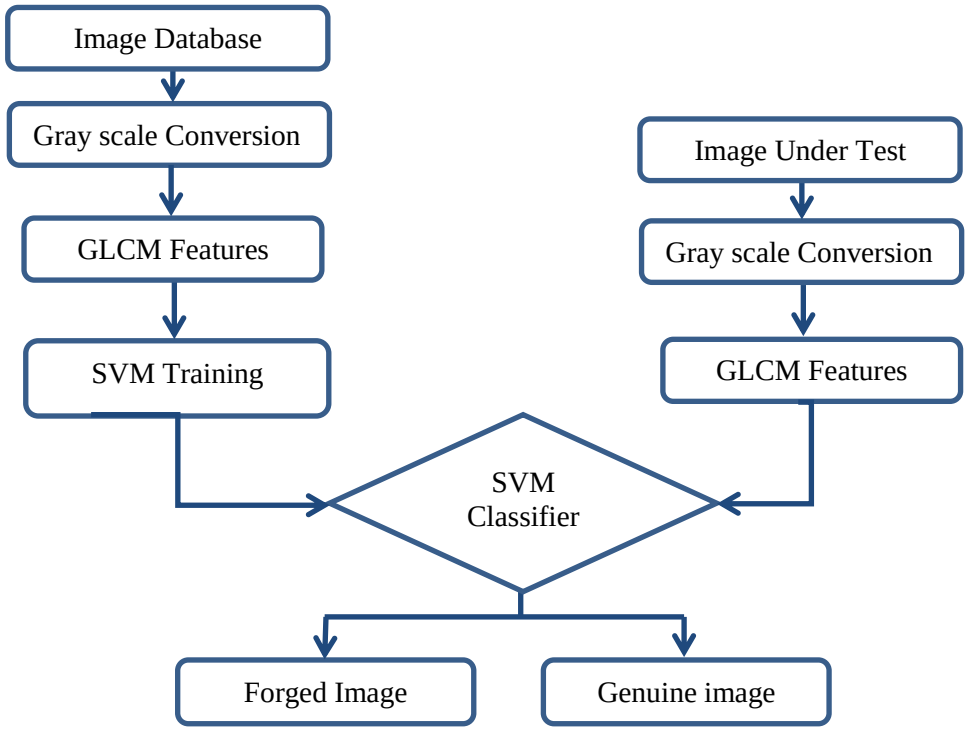

Figure 3. Process Flow of Proposed Method

4. EXPERIMENTATION AND RESULTS

The proposed method is evaluated on a standard database CoMoFoD [10] using the parameters TPR and FNR. This database contains original, forged and post-processed images after forgery.

True Positive Rate (TPR) = (Forged images declared Forged) / Forged Images
False Negative Rate (FNR) = (Forged images declared Genuine) / Forged Images

In the proposed method, 200 images of size 512x512 are considered. The operations such as scaling and rotation are performed before pasting the copied portion. It is evident from the Table 1 that the TPR value reduces if the copied portion is rotated much. As well, for small scaling factors the TPR is less and when the scaling factor is high TPR is high.

Table 1: TPR Values for Rotation and Scaling attacks

Rotation		Scaling	
Rotated angle	TPR	Scaled factor in %	TPR
3	95.31	40	75
5	75	70	84.37
40	68.75	95	89.5
90	62.50	105	96.87

The post-processed images with the below attacks are considered for evaluation.

i. "JC" - JPEG compression with quality factor ranging from 20 to 100,
ii. "IB" - Image Blurring with mean = 0, variance values of 0.009, 0.005 and 0.0005,
iii. "NA" - Noise Addition with averaging filter masks 3x3, 5x5, 7x7,
iv. "BC" - Brightness Change varies between 0.01- 0.95, 0.01- 0.9 and 0.01- 0.8,
v. "CR" - Color Reduction 32, 64, 128 levels per color component
vi. "CA" - Contrast Adjustments varies between 0.01- 0.95, 0.01- 0.9 and 0.01- 0.8.

The present method is appraised by considering 50 forged images in each post-processing attack category, so at the outset 1200 forged and processed images are tested.

Table 2: TPR and FNR of our proposed method for various post-processing attacks

Attack Description	TPR in %	FNR in %
No Attack	100	0
Brightness Change (0.01, 0.95)	92	8
Brightness Change (0.01, 0.9)	100	0
Brightness Change (0.01, 0.8)	100	0
Contrast Adjustment (0.01, 0.95)	66	34
Contrast Adjustment (0.01, 0.9)	68	32

Contrast Adjustment (0.01, 0.8)	76	24
Color Reduction 32	98	2
Color Reduction 64	94	6
Color Reduction 128	94	6
Image Blurring $\mu = 0, \sigma 2 = 0.009$	60	40
Image Blurring $\mu = 0, \sigma 2 = 0.005$	68	32
Image Blurring $\mu = 0, \sigma 2 = 0.0005$	88	12
Noise Adding 3x3	100	0
Noise Adding 5x5	96	4
Noise Adding 7x7	78	22
JPEG Compression QF=20	70	30
JPEG Compression QF=30	74	2
JPEG Compression QF=40	74	26
JPEG Compression QF=50	80	20
JPEG Compression QF=60	90	10
JPEG Compression QF=70	94	6
JPEG Compression QF=80	100	0
JPEG Compression QF=90	100	0
JPEG Compression QF=100	100	0

It is evident from Table 2 that the proposed method withstand attacks JPEG compression, Image blurring, Color reduction, brightness change and Noise addition in a better manner when compared to the attacks Contrast adjustment and Image blurring. It is evident from Table 3 that our method outperforms the other two methods [4, 6] in terms of TPR under no attack.

Table 3: Comparative Analysis of the proposed method

Method	Robust to Affine attacks	TPR %
Method in [4]	RST invariant	95.48
Method in [6]	No	99.83
Proposed Method	RST Invariant	100

5. CONCLUSIONS

In recent times, GLCM features are exploited to identify forgery related to Human faces in digital images. But, in our proposed method it is explored for all kinds of images such as buildings, plants, vehicles, people and textures. The simulation results indicate that our proposed method withstands all the post-processing attacks except Contrast Adjustment and Intensity Blurring. The proposed method outperforms the two methods [4, 6]. Proposed method is also invariant to

rotation and scaling attacks to some extent. In future, the work can be extended to localize the tampered regions.

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Intentional Blank

DWT BASED AUDIO WATERMARKING SCHEMES:A COMPARATIVE STUDY

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ABSTRACT

The main problem encountered during multimedia transmission is its protection against illegal distribution and copying. One of the possible solutions for this is digital watermarking. Digital audio watermarking is the technique of embedding watermark content to the audio signal to protect the owner copyrights. In this paper, we used three wavelet transforms i.e. Discrete Wavelet Transform (DWT), Double Density DWT (DDDWT) and Dual Tree DWT (DTDWT) for audio watermarking and the performance analysis of each transform is presented. The key idea of the basic algorithm is to segment the audio signal into two parts, one is for synchronization code insertion and other one is for watermark embedding. Initially, binary watermark image is scrambled using chaotic technique to provide secrecy. By using QuantizationIndex Modulation (QIM), this method works as a blind technique. The comparative analysis of the three methods is made by conducting robustness and imperceptibility tests are conducted on five benchmark audio signals.

KEYWORDS

Discrete Wavelet Transform (DWT), Double Density DWT (DDDWT) and Dual Tree DWT (DTDWT), Quantization Index Modulation (QIM)

1. INTRODUCTION

The swift growth in multimedia technology and the usage of internet, the major problem facing by the owners is unauthorized copying, transmission and distribution of multimedia content.The most common solutionfor protection of copyright is digital watermarking [1, 2]. Watermarking is the process, in which watermark content is embedded into the digital content. Digital content may be audio, image or video. Developing audio watermarking algorithms are not that much easy [3,4] compared to image and video watermarking,. Firstly, Human Auditory System (HAS) is much sensitive than Human Visual System (HVS). Therefore, even small changes in audio are also recognized by the human ear. Secondly, video files are large compared to audio files in terms of size. Hence, data hidden in audio files is quietly large compared with the image or video and this high payload tends to degrade the audio quality. Therefore, trade-off exists between robustness and imperceptibility.

Recently, several audio watermarking algorithms are developed. Most of the algorithms are based on either time domain [5,6] or transform domain [7,8,9,10,11]. Watermarking in time domain is easier to implement and needs less computational resources thanwatermarking in transform domain [3,8] but, it is less robust against common signal processing attacks when compared to transform domain watermarking. Generally, Fast Fourier Transform (FFT)[11], Discrete Cosine Transform (DCT) [9], and Discrete Wavelet Transform (DWT)[10] are explored for transform domain audio watermarking.

Still, there is a need for robust and high secured audio watermarking algorithms. In this paper, the chaotic Gaussian map is used to encrypt the watermark image. The Logistic chaotic sequence is used to develop synchronization code. Then, the watermark is embedded in DWT/DDDWT/DTDWT coefficients of audio signal using QIM.

2. METHODS

2.1. Discrete Wavelet Transform (DWT)

The analysis filters (a1 and a2) decomposes the input signal x(n) into two sub-bands i.e., low-pass frequency band (c(n)) and high frequency band (d(n)) and each of which is then down-sampled by 2. The two sub-bands (c(n) and d(n)) are up-sampled by 2 and the synthesis filters (s1 and s2) combines the two sub-bands to acquire a single signal y(n)[12] shown in Figure 1.

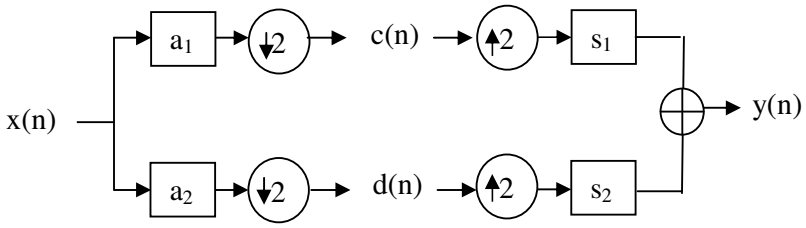

Figure 1. DWT decompose and combined process.

2.2. Double Density DWT (DDDWT)

Double –Density DWT [12] makes use of two distinct wavelets and a single scaling function. The analysis filters decomposes the x(n) signal into three bands, and every sub-band is down-sampled by 2. The filter bank for analysis consists of one low-pass filter (a1) and two high pass filters (a2 and a3). The synthesis filter bank consists of one low-pass filter (s1) and two high pass filters (s2 and s3). These3 sub-band coefficients pass through the system are up-sampled by two, synthesized and then combined to develop the signal y(n) shown in Figure 2.

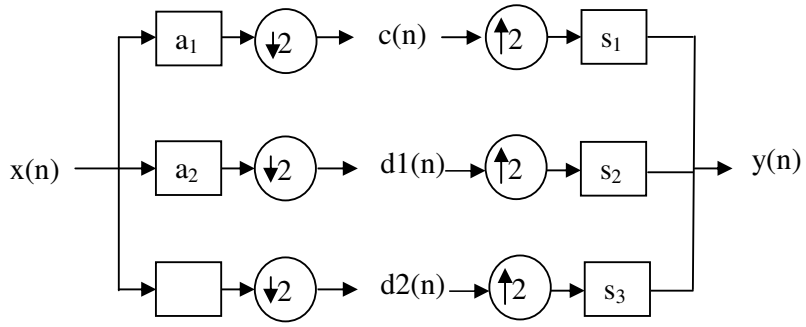

Figure 2. DDDWT decompose and combined process.

2.3. Dual Tree DWT (DTDWT)

The dual tree DWT of a signal x(n) is a parallel combination of two DWTs [13]. Therefore, it is 2-times expensive than DWT. The filters are chosen in a way that the upper DWT can be inferred as real part of the wavelet and lower DWT can be inferred as imaginary part of wavelet [14] and is shown in Figure 3.

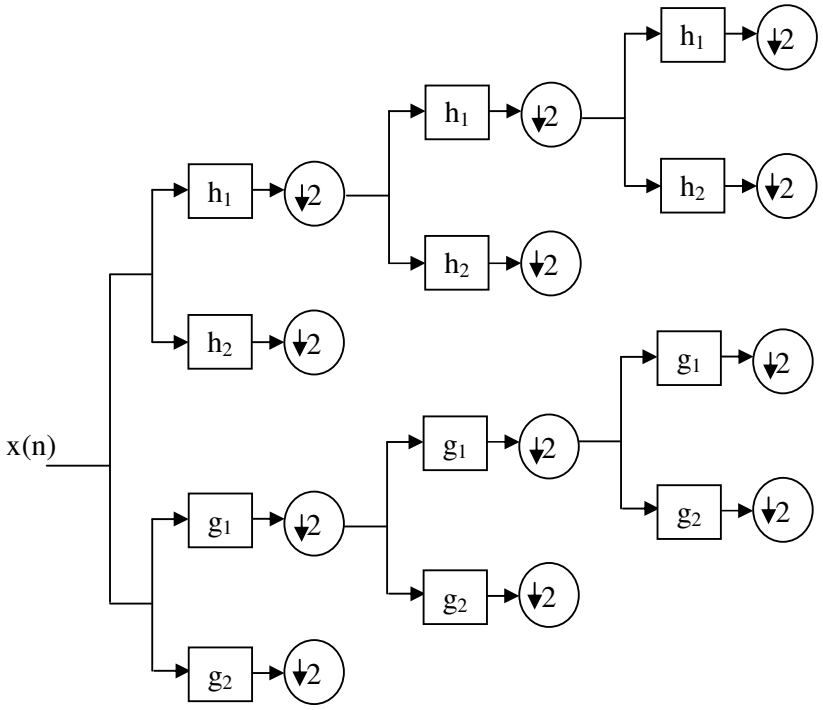

Figure 3. DTDWT decompose and combined process.

3. SYNCHRONIZATION CODE GENERATION AND INSERTION

The synchronization code [7,8,9] is used to resist the de-synchronization attacks. Desynchronization attack means the watermark cannot be recognized from the watermarked audio because of lack of synchronization. Desynchronization attacks are cropping, shifting and MP3 compression, they will change the audio signal length, which leads to unsuccessful extraction of the watermark.To overcome this problem, exact location of the watermark should be identified before the extraction process. For synchronization code generation, the logistic chaotic sequence is used, that is defined as:

$$y_{n+1} = \gamma y_n(1 - y_n) \quad (1)$$

Where y_n is the initial value that is from 0 to 1, γ is the real parameter.

Synchronization code is generated using eq(1) based on the following condition.

$$S_n = \begin{cases} 1, & if y_n > 1/2 \\ 0, & otherwise \end{cases} \quad (2)$$

The host audio A is divided into two parts A_S and A_w. Synchronization code that is generated from the eq(2) is hosted into the first part of audio signal A_S with length LS is embedded as follows:

$$A'_S(n) = \begin{cases} round\left(\frac{A_S(n)}{\delta}\right) * \delta, & if S_n = 0 \\ (floor(\frac{A_S(n)}{\delta}) * \delta) + \frac{\delta}{2}, & if S_n = 1 \end{cases} \quad (3)$$

where δ is the embedding strength.

Embedded and attacked watermarked audio signal is also split into two parts. From first part of watermarked signal A''_S synchronization code will be detected with following condition.

$$S'_n = \begin{cases} 0, & if \delta/4 \le mod(A''_S(n), \delta) < 3\delta/4 \\ 1, & otherwise \end{cases} \quad (4)$$

4. WATERMARK EMBEDDING AND EXTRACTION

4.1. Pre-processing of a Watermark

To improve the security and robustness, watermark image must be pre-processed by using chaotic scrambling technique. Gaussian map [11] is one of the chaotic encryption methods. Gaussian map chaotic encryption technique is defined as:

$$z_{n+1} = e^{(-\alpha(z_n)^2)} + \beta \quad (5)$$

Where z1 is the initial value that ranges from 0 to 1. α and β are the real parameters.

$$v_n = \begin{cases} 1, & if z_n > Th \\ 0, & otherwise \end{cases} \quad (6)$$

Where Th is the predefined threshold. Two dimensional binary watermark is converted into a vector w_n of size M X M. This w_n is encrypted by v_n using following condition:

$$G_n = XOR(w_n, v_n) \quad (7)$$

4.2. Watermark Concealing Procedure

The watermark concealing procedure is given in Figure 4 . In this procedure, total audio signal is segmented into two parts. The synchronization code is insert in audio signal first part to overcome the de-synchronization attacks. The audio signal second part is used to host the pre-processed watermark image.

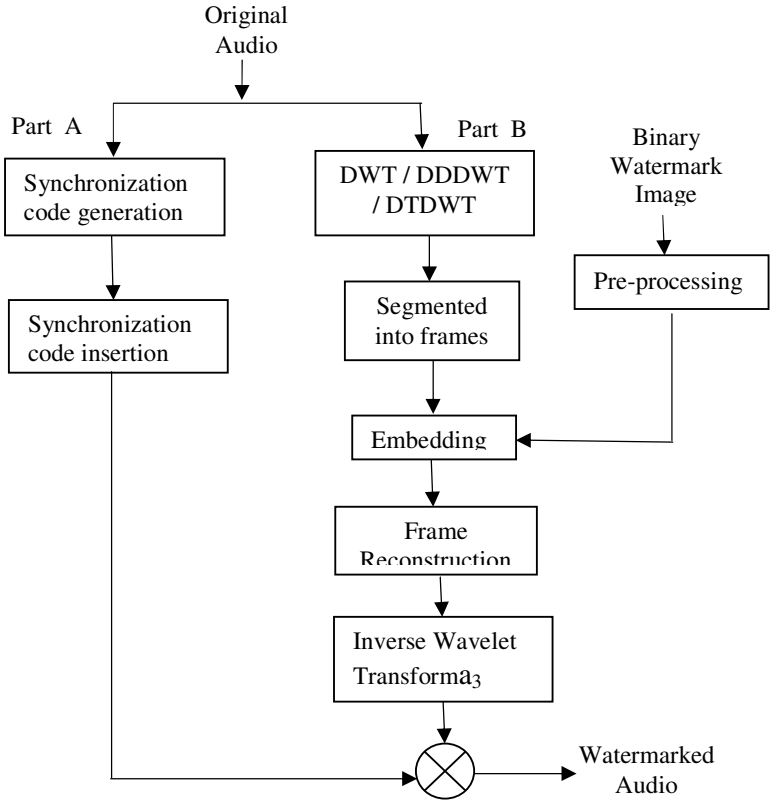

Figure 4. Flowchart of watermark embedding process.

The concealing procedure is detailed as follows:

Step 1: Apply DWT/DDDWT/DTDWT on second part of audio signal.
Step 2: Wavelet coefficients are segmented into frames, and number of frames must be greater than the watermark size.
Step 3: The pre-processed watermark is embedded into each frame using the following rule.

$$F_w'(n) = \begin{cases} round\left(\frac{F_i(n)}{Q}\right) * Q, & if G_n = 0 \\ (floor(\frac{F_i(n)}{Q}) * Q) + \frac{Q}{2}, & if G_n = 1 \end{cases} \quad (8)$$

where Q is the embedding strength.
Step 4: Reconstruct the modified frames.
Step 5: Apply inverse wavelet transform on watermarked audio.

4.3. Extraction Algorithm

The process of extraction is the exact reverse process of concealing process and the algorithm is given below:

Step1: Apply DWT/DDDWT/DTDWT on the second part of attacked watermarked audio signal.
Step2: Wavelet coefficients are segmented into frames.
Step3: Binary encrypted watermark vector is extracted from each frame by using following equation.

$$g_n^{'} = \begin{cases} 0, & if Q/4 \le mod(F_w^{''}(n), Q) < 3Q/4 \\ 1, & otherwise \end{cases} \quad (9)$$

Step4: The decryption process is same as encryption to determine the binary watermark sequence.
Step5: Finally, convert the one dimensional extracted and decrypted binary sequence into two dimensional watermark image of size M X M.

5. SIMULATION RESULTS

The experimental results give the comparative analysis of the three methods. The performance of the three methods iscompared in terms of robustness, imperceptibility and payload. The experiment is carried on 5 different types of 16-bit audio signals in the .WAV format with the sampling rate 44.1 kHz. Each audio is of 10sec duration.

Binary image of 64 X 64 size is used as a watermark. For increasing the security of the watermark, a Gaussian map chaotic encryption technique is used. Figure 5 illustrates Original and encrypted watermark images.

Figure 5. Original watermark and its encrypted watermark images.

5.1. Imperceptibility Test

The audio signal quality should not be degraded upon embedding. The two approaches to perform the perceptual audio quality evaluation [15]. i) Objective test by perceptual evaluation of audio signal ii) Subjective listening test based on HAS.

i) Objective evaluation test:

To evaluate the objective quality, SNR metric is used. International Federation of the Phonographic Industry (IFPI) quotes that watermarked audio should have SNR more than 20dB [8]. SNR Vs Quantization step for three methods are shown in Figure 6.

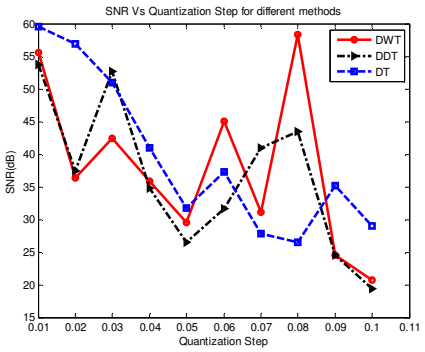

Figure 6. SNR Vs Quantization step

	DWT	DDDWT	DTDWT
Audio-1	31.1205	41.0349	27.7986
Audio-2	42.311	30.6061	27.2856
Audio-3	41.2256	27.0774	53.433
Audio-4	58.0209	41.3026	48.2897
Audio-5	29.8392	36.1878	36.0735
Average	40.5034	35.2417	38.5760

Table 1. SNR in dB for benchmark audio

Table 1 shows the SNR values and their average SNRs for different classes of benchmark audio signals at Q=0.07 are above 20dB and hence meets IFPI requirement.

ii) Subjective Listening Test:

The SNR measure is not sufficient to measure imperceptibilty [8]. Therefore, subjective listening test is also important to evaluate the imperceptibility. Subjective Difference Grade (SDG) is a popular method to evaluate the watermarked audio quality [11]. Table 2 shows the SDG ranges, which is from 5.0 to 1.0. This listening test is performed with ten listeners. Subjects are listened original and watermarked audio signals and they report if any variation is identified between two signals using SDG. The average SDG values are also called as Mean Opinion Score (MOS). The MOS values for DWT,DDDWT and DTDWT is 4.5, 4.8 and 4.7 respectively at Q=0.07.

Table 2. SDG Ranges

Report by subject	**Quality**	**Grade**
Imperceptible	Excellent	5
Perceptible, but not annoying	Good	4
Slightly annoying	Fair	3
Annoying	Poor	2
Very annoying	Bad	1

5.2. Robustness Test

Robustness of this scheme is evaluated with the below attacks on watermarked audio.

i) Resampling: The watermarked audio is resampled to 22.05 kHz, 11 kHz and 8 kHz and sampled back to 44.1 kHz.
ii) Re-quantization: Quantized down to 8-bit and re-quantized back to 16-bit.
iii) Noise: Added with random noise of 30dB signal.
iv) Low-pass Filtering: Cut-off frequency of 20 kHz is applied.
v) Echo addition: 10 ms and 1% decay of echo signal is added.
vi) MP3 Compression: 128 kbps and 256 kbps MPEG compression is applied to the watermarked audio signal and then decoded back to the .WAV format.

vii) Additive Noise: Additive Gaussian Noise with 50 dB and 60 dB.
viii) Cropping: 1000 samples of the watermarked audio signal are made zero at beginning, middle and ending parts.
ix) Signal Addition: Beginning samples are added with original audio samples.
x) Signal Subtraction: Watermarked audio signal beginning samples are subtracted with original audio samples.

For comparison of original watermark and extracted watermark, Bit Error Rate (BER) and Normalized Correlation (NC) are used.

$$\text{BER} = \frac{\text{Number of error bits}}{\text{Number of total bits}} \tag{10}$$

$$NC = \frac{\sum_m \sum_n (A_{mn} - \bar{A})(B_{mn} - \bar{B})}{\sqrt{\sum_m \sum_n (A_{mn} - \bar{A})^2 \sum_m \sum_n (B_{mn} - \bar{B})^2}} \tag{11}$$

Table 3 shows BER and NC for all mentioned signal processing attacks for three methods at Q=0.07.

Table 3. BER and NC values for signal processing attacks.

Method	**DWT**		**DDDWT**		**DTDWT**	
Signal Processing Attack	**BER**	**NC**	**BER**	**NC**	**BER**	**NC**
Without attack	0	1	0	1	0.0002	0.9994
Resampling(22.05kHz)	0.0007	0.9982	0	1	0.1182	0.7316
Resampling(11kHz)	0.1741	0.6096	0.1528	0.6508	0.3726	0.2303
Resampling(8kHz)	0	1	0	1	0.0012	0.9971
Re-quantization	0	1	0	1	0.0447	0.8954
Noise	0	1	0	1	0.0059	0.9861
Filtering	0	1	0.0002	0.9994	0.0269	0.9363
Echo addition	0	1	0.0002	0.9994	0.0203	0.952
MP3 Compression (256)	0	1	0	1	0.0063	0.9848
MP3 Compression (128)	0.0004	0.9988	0.0012	0.9971	0.0354	0.9167
Additive Noise (50dB)	0	1	0	1	0.0591	0.863
Additive Noise (60)	0	1	0	1	0.0146	0.9651
Cropping (middle)	0	1	0	1	0.0002	0.9994
Cropping (end)	0	1	0	1	0.0002	0.9994
Cropping (front)	0.0022	0.9948	0.0022	0.9948	0.0024	0.9942
Signal Addition	0.002	0.9953	0.0022	0.9948	0.0022	0.9948
Signal Subtraction	0.002	0.9953	0.0022	0.9948	0.0024	0.9942

6. CONCLUSIONS

The performance of DWT based audio watermarking schemes viz., DWT, DDDWT and DTDWT is analyzed. SNR is above 20 dB for all the three schemes. The watermarked signal is tested against various signal processing attacks for different classes of audio signals and the performance parameters BER and NC are obtained. The parameters shows that DDDWT

outperforms DTDWT for different values of quantization step. Also, DDDWT performance is almost nearer to DWT scheme.

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PERFORMANCE ANALYSIS OF CRT FOR IMAGE ENCRYPTION

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ABSTRACT

With the fast advancements of information technology, the security of image data transmitted or stored over internet is become very difficult. To hide the details, an effective method is encryption, so that only authorized persons can decrypt the image with the keys available. Since the default features of digital image such as high capacity data, large redundancy and large similarities among pixels, the conventional encryption algorithms such as AES, , DES, 3DES, and Blow Fish, are not applicable for real time image encryption. This paper presents the performance of CRT for image encryption to secure storage and transmission of image over internet.

KEYWORDS

Digital image, Chinese Remainder Theorem, encryption, confidentiality

1. INTRODUCTION

The role of Digital images is important, both in daily life applications as well as in areas of research and technology. An image is a 2-D representation of a three dimensional scene. Due to its large capacity data, huge redundancy and high similarities among pixels, there are several researchers [1-7] done lot of work for image compression for long period except for image encryption, From this, research papers we see that the compression performances are good**.**

Many number of image encryption schemes combined with compression are proposed. These methods divide the image encryption and image compression into two separate stages [8-13]. These, mainly separate the encryption without considering the compression process. Few propose overcome the drawbacks in Refs. [8–13] by making the image encryption and compression in a single process [14–17]. Refs [18] propose a new image encryption algorithm integrated with compression using 2D hyper-chaos discrete nonlinear dynamic system and Chinese remainder theorem. However these papers do not evaluate the performance of CRT. This paper presents the optimal performance and limitations of CRT for image compression.

2. CHINESE REMAINDER THEOREM

Chinese remainder theorem [19-23] is a theorem about congruence's in number theory. It can be stated as follows:

If m_1, m_2,…..m_k are pair-wise relatively prime positive integers , and if a_1, a_2, …., a_k are any integers , then the simultaneous congruence's

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$x \equiv a_1 \pmod{m_1}$, $x \equiv a_2 \pmod{m_2}$, …., $x \equiv a_k \pmod{m_k}$ have a solution, and the solution is unique modulo m, where $m = m_1 m_2 \ldots m_k$

From Chinese remainder theorem, using k gray values, $a_1, a_2, \ldots, a_k$, we get a gray value: $x \equiv m_1 m_1^{-1} a_1 + m_2 m_2^{-1} a_2 + \cdots + m_k m_k^{-1} a_k \pmod{m}$. Therefore. CRT can encrypt an image, at the same it also compress the image with a given compression ratio k, simultaneously. From the unique solution $x \equiv m_1 m_1^{-1} a_1 + m_2 m_2^{-1} a_2 + \cdots + m_k m_k^{-1} a_k \pmod{m}$. we can also get a_i by $a_i \equiv x \pmod{m_i}$, where i = 1,….,k. The above procedure is used for decryption and to uncompress the image.

.

The *Chinese Remainder Theorem* can be used for generating Godel numbering for sequences, for Good Thomas Fast Fourier transforms for re-indexing of data, for implementing the RSA encryption and decryption, for distributing the shared key among a group of people, and also used for range ambiguity resolution techniques with medium pulse repetition frequency radar Some of the important parameters image are PSNR value and Correlations are define as follows

3. PSNR value

Peak signal-to-noise ratio, often abbreviated **PSNR**, is the ratio between the maximum possible power of a signal and the power of corrupting noise that affects the fidelity of its representation. PSNR is usually expressed in terms of the logarithmic decibel scale.

$$\begin{aligned} PSNR &= 10 \cdot \log_{10}\left(\frac{MAX_I^2}{MSE}\right) \\ &= 20 \cdot \log_{10}\left(\frac{MAX_I}{\sqrt{MSE}}\right) \\ &= 20 \cdot \log_{10}(MAX_I) - 10 \cdot \log_{10}(MSE) \end{aligned}$$

4. CORRELATION

Correlation coefficient is a coefficient that illustrates a quantitative measure of some type of correlation and dependence, meaning statistical relationships between two or more random variables or observed data values.

5. IMAGE ENCRYPTION PROCEDURE USING CRT

Step1: To compress an image with size HxW in to an image with size (HxW)/K, we , set compression ratio k. This compression ration k is achieved by selecting randomly K integers:$a_1, a_2, \ldots\ldots ak, a_i$, where $a_i > 256$, $\gcd(a_i, a_j) = 1$, $1 <= i, j <= k$, where H and W are the height and width of the plain image

Step2: Divide the shuffled gray value sequence S' into

(H xW)/k blocks: $B_1 = \{S'_1, S'_2, \ldots\ldots, S'_k\}$, $B_2 = \{S'_{k+1}, S'_{k+2}, \ldots\ldots, S'_{2k}\}$, ……..,

$B_{(HxW)/k} = \{S'_{HxW-(k-1)}, S'_{HxW-(k-2)}, \ldots\ldots, S'_{HxW}\}$.

Step3: For each block Bi, i=1, 2, . . . ,(H x W)/k, by using CRT formula, encrypt each block into a value Vi, and get the encrypted and compressed sequence V ={V1,V2, . . . ,$V_{(HxW)/K}$}. Note that for each block Bi, $x_1,x_2, \ldots ,x_k$ can be different, which may enhance the security of the algorithm
Step4: To form the encrypted and compressed image, reshape V back to the 2D value matrix with size (H xW)/k

For experimental purpose, as example, I take k=4. This means that the cipher image is compressed into 1/4 of the plain image and further I chosen m_1 = 311, m_2 =313,m_3 =317, m_4 =293 randomly for encryption and decryption

The following procedure is used to uncompress and decrypt the image:

Step1: Arrange the encrypted-compressed image into a sequence

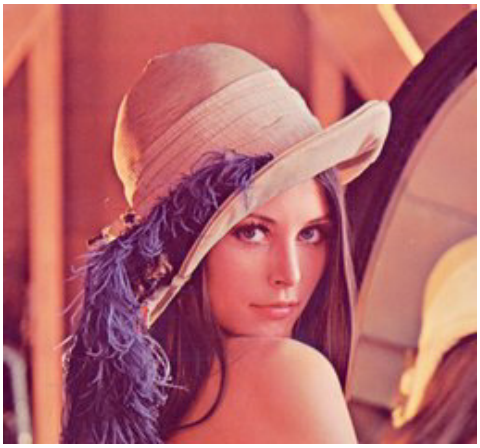
V ={ V1,V2, . . . ,$V_{(HXW)/K}$}.
Step2: Decrypt each Vi into k integers $x_1,x_2, \ldots ,x_k$ by $x_j = V_i \pmod{m_j}$, j = 1,2, . . . ,k,

where m_i is defined in the encryption procedure. Then, get a decrypted sequence
X={$x_1,x_2, \ldots ,x_{(HxW)}$}.

Step3: Reshape X ={$x_1,x_2, \ldots ,x_{(HxW)}$ } values with H rows and W columns to form the decrypted and decompressed image.

RESULT AND ANALYSIS

The following results shows the histograms of original, encrypted and decrypted image along with the correlation for different key values of the following standard image



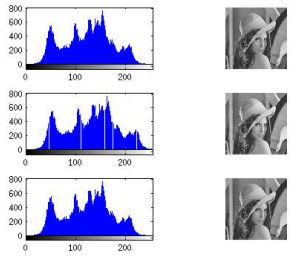
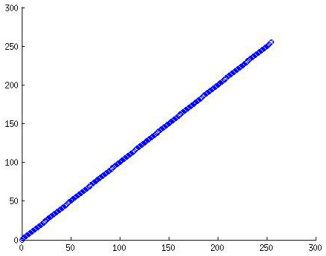
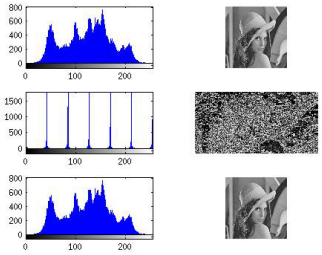
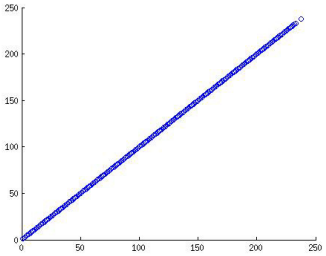
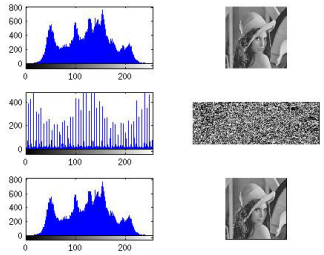
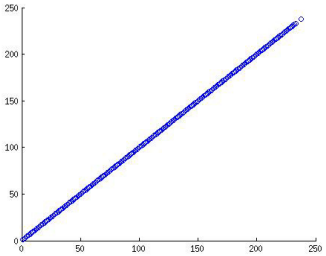
Standard .jpg

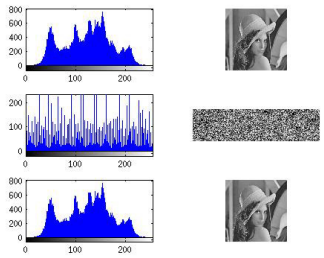
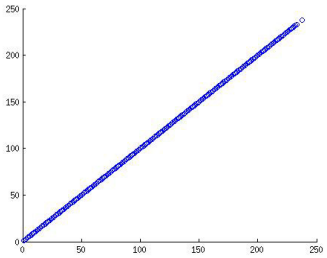
Key Values used are:

m = [467]; m for a=1
m = [971 977]; for a=2
m = [263 269 271]; for a=3

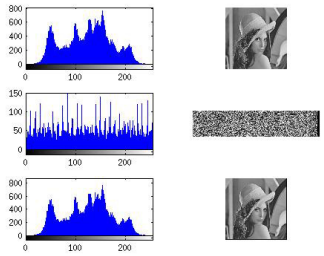
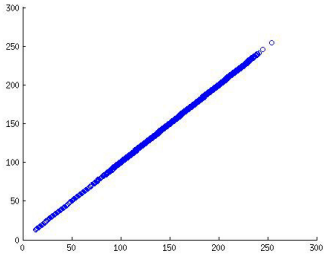
m = [977 983 991 997]; for a=4
m = [443 449 457 461 467]; for a=5
m = [263 269 271 277 281 283]; for a=6
m = [257 263 269 271 277 281 283]; for a=7
m = [307 311 313 317 331 337 347 349]; for a=8
m = [257 263 269 271 277 281 283 293 307]; for a=9
m = [257 263 269 271 277 281 283 293 307 311]; for a=10

Standard jpg

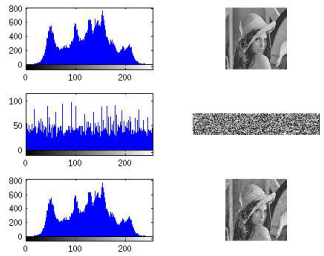
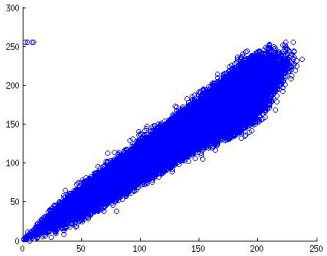
KEY VALUES	CORRELATION
(k=1) = [467]	
	
(k=2) = [971 977]	
	
(k=3) = [263 269 271]	
	
(k=4) = [977 983 991 997]	

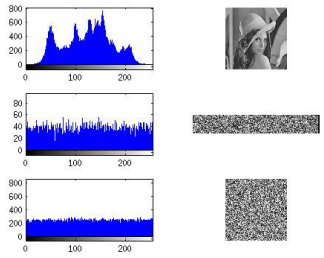
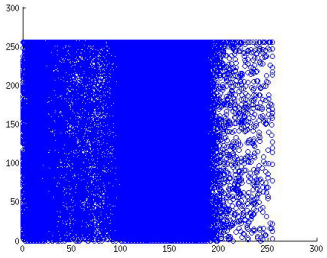
(k=5) = [443 449 457 461 467]

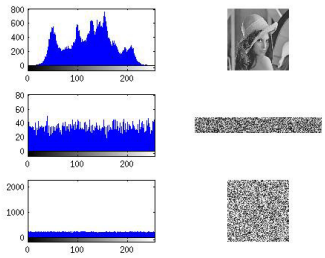
(k=6) = [263 269 271 277 281 283]

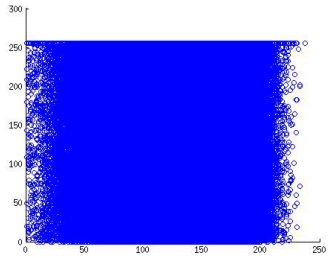



(k=7) = [257 263 269 271 277 281 283]

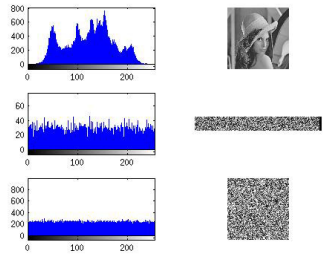



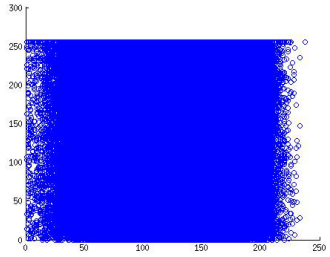
(k=8) = [307 311 313 317 331 337 347 349]



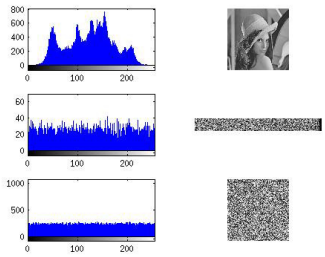


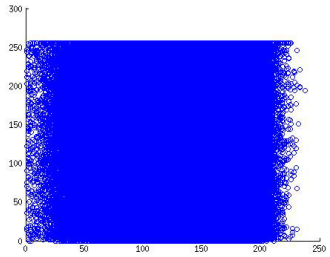
(k=9) = [257 263 269 271 277 281 283 293 307]





(k=10) = [257 263 269 271 277 281 283 293 307 311]





ANALYSIS

The following table values of correlation coefficient, PSNR and MSE for the sample image to the number of keys

SAMPLE NAME	Correlation coefficient	PSNR value	MSE value
Number of Keys =1 , m = [467]	1	infinity	0
Number of keys =2 ; m= [971 977]	1	infinity	0
Number of keys= 3, m = [263 269 271]	1	infinity	0
Number of keys= 4, m = [977 983 991 997]	1	infinity	0
Number of keys= 5, m =[443 449 457 461 467]	1	Infinity	0

Number of keys=6, m= [263 269 271 277 281 283]	0.9779	27.9575	104.07
Number of keys=7, m= [257 263 269 271 277 281 283]	-0.0067	8.0042	10296
Number of keys=8, m= [307 311 313 317 331 337 347 349]	-0.00085318	8.0243	10248
Number of keys=9, m= [257 263 269 271 277 281 283 293 307]	0.0013	8.7828	8606
Number of keys=10, m= [257 263 269 271 277 281 283 293 307 311]	0.0024	8.7352	8700.7

6. CONCLUSION

It is concluded from the result analysis of image encryption using CRT, that the encryption and decryption is optimal when the number of keys used are between 2 to 5 and the compression ratio is directly proportional to number keys used for encryption. Further it is observed that, if we increase the keys beyond the 5, the decryption process is unable to produce a valid decrypted image. Hence, this paper concludes, that, the CRT not only be used for image encryption and it also provide compression as well.

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BLIND IMAGE QUALITY ASSESSMENT WITH LOCAL CONTRAST FEATURES

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ABSTRACT

The aim of this research is to create a tool to evaluate distortion in images without the information about original image. Work is to extract the statistical information of the edges and boundaries in the image and to study the correlation between the extracted features. Change in the structural information like shape and amount of edges of the image derives quality prediction of the image. Local contrast features are effectively detected from the responses of Gradient Magnitude (G) and Laplacian of Gaussian (L) operations. Using the joint adaptive normalisation, G and L are normalised. Normalised values are quantized into M and N levels respectively. For these quantised M levels of G and N levels of L, Probability (P) and conditional probability(C) are calculated. Four sets of values namely marginal distributions of gradient magnitude Pg, marginal distributions of Laplacian of Gaussian Pl, conditional probability of gradient magnitude Cg and probability of Laplacian of Gaussian Cl are formed. These four segments or models are Pg, Pl, Cg and Cl. The assumption is that the dependencies between features of gradient magnitude and Laplacian of Gaussian can formulate the level of distortion in the image. To find out them, Spearman and Pearson correlations between Pg, Pl and Cg, Cl are calculated. Four different correlation values of each image are the area of interest. Results are also compared with classical tool Structural Similarity Index Measure (SSIM)

KEYWORDS

Gradient Magnitude, Laplacian of Gaussian, Joint Adaptive Normalisation, Normalised Bivariate Histograms, Spearman rank Correlation, Pearson Correlation Coefficient.

1. INTRODUCTION

Image quality assessment evaluates the quality of the distorted image. Factors which determine image quality are, noise, dynamic range tone reproduction, colour accuracy, distortion, contrast, exposure accuracy, lateral chromatic aberration, sharpness, colour moiré, vignette, artefacts. Distortion is defined as abnormality, irregularity or variation caused in an image. This is noticeable in low cost cameras. Distortions are caused during Acquisition, Compression, Transmission and Storage. Changes in image or quality of image are observed either by the human subjects called as subjective measure or calculated by mathematical operations called as

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objective measures. Image quality assessment can also be categorised as With Reference models and Without Reference models. First type of models finds out quality of the image by comparing with its original image. Second type of models also called as Blind image quality assessment finds out the quality of distorted image without comparing with its original image.

Local contrast features describe the structure of the image. The changes in the structure of the image like shape and amount of edges are detected easily. Two general local contrast features are Gradient magnitude and Laplacian of Gaussian. Joint adaptive normalisation (JAN) normalises G and L channels jointly. The benefit of JAN is to make the horizontal, vertical and diagonal features correlative in the image. It reduces the redundancies in image. Normalisation stabilizes the profiles of these features. The G and L distributions of images are very different from natural images. Quantising into levels and thereby giving joint probability function, statistics are derived. Marginal distributions and conditional probability dependency measures are recorded into four different correlations are drawn.

Over years there had been several performance measures for image quality assessment. DMOS/MOS difference mean opinion scores is a subjective measure which evaluates over human judgements [4]. Various databases established by IQA community are LIVE, CSIQ, TID2008. CSIQ, TID2008 and LIVE has 4 common types of distortions they are JP2K, JPEG, WN and Gaussian blur. These are used to identify the characteristics of the various distortions. To find out performance of a method, a machine which calculates the correlations of the subjective scores of the human judgements constructed. The correlations used are Spearman rank order correlation coefficient (SRC) and Pearson correlation coefficient (PCC). Proposed Blind image quality assessment model is compared with Structural Similarity Index Measure (SSIM).

Experimental results define that there is equivalent information in one of the four sets of statistics we derive. However joint statistics in of Pearson model give better results. Existing models involve in large procedures to find out the disturbances in the frequencies over different distortions. Few models even changes the features of the image. G and L operations are close to the results of the human visual system. G and L are independent over the distortions. The marginal and independency distributions can determine the quality of the image. Joint adaptive normalisation procedure normalises the G and L features. Proposed model uses independency distributions to measure joint statistics. Which leads to highly competitive results in terms of Quality prediction, Generalisation ability, and effectiveness. Existing models have computational complexity. To reduce regression methods, and get finer quality measure with no training or regression methods we derive a new method with probability statistics.

This paper is organised in four sections. Section II gives a brief study of all the existing models of without reference image quality assessment. Section III presents the features of the proposed model in detail and exclusive experimental results in each stage of the process. Section IV concludes the paper.

2. RELATED WORK

2.1.Literature Survey

There are several image quality assessment models. Mean Square Error (MSE) is the primitive measure [2]. When original image is the known reference image, a written explanation of the measure exits in the literature. Mean Square Error (MSE) found to be very important measure to

compare two signals. It provides a similarity index score that gives the degree of similarity. Similarity index map is amount of distortion between two signals. It is simple, parameter free and inexpensive. It is employed widely for optimizing and assessing signal processing applications. Yet it did not measure signal fidelity to certain required extinct. When altered by two different distortions at a same level, MSE only gave the value of distortion. MSE is very converse to the human perception. MSE led to development of Minimum Mean Square Error, Peak Signal to Noise Ratio.

Based on the luminance, contrast and structure of an image, the Structural Similarity Index Measure (SSIM) [3] is developed. It is an objective quality measure of image to quantify the visibility of errors. It is a similarity measure for comparing any two signals. Like MSE, it is a full reference model which depends on the structural similarity. It has SSIM index map which shows the comparison better than MSE. It is a complex measure for an image with large content. Though SSIM index could give better results compared to the traditional Mean square error, it lacked in defining what the type of distortion is present in the image. This novel work gave scope for the study on structure statistics of the image. Furthermore, it is used to simplify algorithms of image processing system. For image quality measure, SSIM proved its efficiency than mean square error. SSIM is computationally expensive than MSE.

Difference Mean Opinion Scoring (DMOS) is a performance evaluation study of existing methods of IQA along with subjective scores collected over a period of time with numerous human subjects [4]. There is no replacement to the Human Visual system (HVS) [5]. DMOS when compared objective measures like PSNR, MSE and SSIM, proved that Human Visual System had better evaluation. Subjective group verified and gave responses over LIVE database which consists of 779 distorted images from 29 original images with five distortions [14]. It gave importance to visual difference. Used of Spearman Rank Correlation and Root Mean Square Error for perfection. It has 95% confidence criterion of finding out whether distorted or not. This study gave a valuable resource of scores of distortion. It led to study of natural scene statistics. DMOS is used as benchmark for checking of constructed models.

The reference image is not always available. Hence, there is need of without reference image quality assessment measure also called as Blind Image Quality Assessment. It assesses the quality of an image completely blind i.e., without any knowledge of source distortion [5]. Distorted Image Statistics (DIS) which is used to classify images into distortion categories gave the ease to decide type of the distortion [5]. In this literature, wavelet transform is performed on the image indices. Shape parameter is defined using Gaussian distribution. Given a training set and testing setoff distorted images, a classifier Support Vector Machine is used to classify image into five distortions. This is the first without reference method. It could differentiate the type of distortion. Results of this model correlates with reference models. Its drawback is its computational complexity. This methodology can be replaced with any module which performs better i.e. either by increasing the number of distortions or by increasing training set for better results. This model can be used for video processing by adding measure of relevant perceptual features.

With the probability of usage of the indices as features, a new approach BLIINDS is proposed [5]. It is a model with the evolution of features derived from the Discrete Cosine Transform domain statistics. While the previous no reference is distorted specific approaches, this approach could explain the type of the distortion. It used Support Vector Machine (SVM) which correlates well with human visual perception. It is computationally convenient as it is based on a DCT-framework entirely, and beats the performance of Peak signal to noise ratio. The probabilistic prediction model was trained on a small sample of the data, and only required the computation of

the mean and the covariance of the training data. It computes blockiness measure. It estimates the particular type of distortion. Time taken for computation is high.

Final evolution is the reduction of complexity by combination with Natural scene statistics and addition of distorted image statistics. Work is to extract the statistical information of the edges and boundaries in the image and to study the correlation between the extracted features. Change in the structural information like shape and amount of edges of the image derives quality prediction of the image. Local contrast features are effectively detected from the responses of Gradient Magnitude (G) and Laplacian of Gaussian (L) operations. Adaptive procedures are used to normalize the values of G and L. Normalized values are quantized into certain levels respectively. Conditional probability and Marginal distribution of G and L are calculated which are stored into three segments. They proposed three models. These three segments or models are M1, M2, M3 which have only conditional probability values, only marginal distribution values and both conditional probability and marginal distribution values. Loading values in the support vector regression; over the set of images collected from LIVE database a probable score is determined for each distortion.

There is complexity in training these values into the support vector machine. This paper is a thorough study of the conditional probability and marginal probability values of the gradient magnitude and Laplacian of Gaussian. Marginal distributions and conditional probabilities and their dependencies which lead to highly competitive performance are employed in this work. This avoided the training and learning of the features. Therefore, the complexity is reduced in the modelling. This procedure is a direct extraction of the amount of edges and change in the image. Intensive measurement of the structural information is derived from the correlations between the amounts of the variation caused in the image. Four correlations namely Pearson correlation coefficient between Pg and Pl (PRCP), Pearson correlation coefficient between Cg and Cl (PRCQ), Spearman rank correlation between Pg and Pl (SRCP), Spearman rank correlation between Cg and Cl (SRCQ) are proposed in this paper.

3.PROPOSED WORK

As discussed in the above section, a methodology to find out the profiles of the structural features and to derive the correlations between the structural features is explained in stages with their relevant outcome in each stage is given below.

3.1.Local Features

Local contrast features give the information of the amount of change in the structure of an image. Two general local contrast features are Gradient magnitude (G) and Laplacian of Gaussian (L).

Discontinuities in the structural details like luminance of an image or the change in the intensities are important for quality assessment. These can be derived by performing gradient magnitude and Laplacian of Gaussian operations. We use CSIQ database which is commonly used international database for image quality assessment. Trolley image is considered from database and denoted by I. To standardize Convert image from RGB to grayscale. For size of the image, in the following stages gradient magnitude and Laplacian of Gaussian operators are applied.

3.2.Gradient Magnitude

Gradient magnitude is the first order derivative, often used to detect the edges in the image. Expression for gradient magnitude is given as:

$$G = \sqrt{[I * V]^2 + [I * H]^2}$$

The vertical prewitt filter kernel (V) is considered as [-1 -1 -1; 0 0 0; 1 1 1]. The horizontal prewitt filter kernel (H) is considered as [-1 0 1; -1 0 1; -1 0 1]. Appling these kernels on the image and substituting in G expression given above, we get gradient magnitude image. The original image, vertical prewitt filtered image, horizontal prewitt filtered image and the resultant gradient magnitude image are shown in figure 1.

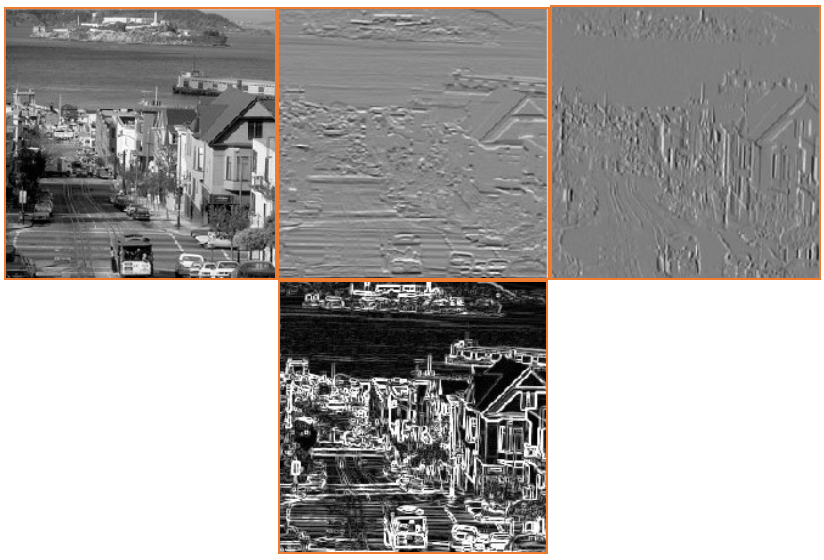

Figure.1. 1) Original image 2) Vertical Prewitt Filtered Image 3) Horizontal Prewitt Filtered Image 4) Resultant gradient magnitude image.

3.3.Laplacian of Gaussian

Laplacian of Gaussian is the second order derivative as shown in the equation. Expression of the Laplacian of Gaussian is given as,

$$L = I * h_{LOG}$$

Where,

$$h_{LOG} = \frac{\partial^2}{\partial x^2} g(x,y) + \frac{\partial^2}{\partial y^2} g(x,y)$$

G and L operations reduce the spatial redundancies in the image. The Laplacian of Gaussian applied image is shown in figure 2. Some consistencies between neighbouring structures still remain. So, to remove these we perform joint adaptive normalisation.

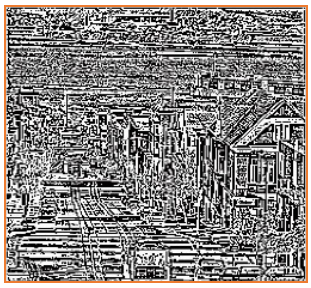

Figure 2. Laplacian of Gaussian performed image.

3.4.Joint Adaptive Normalisation

Joint adaptive normalization (JAN) is performed to remove the spatial redundancies remained in the image [1]. This decomposes the channel into different frequencies and orientations. According to the normalization factor G and L are reduced.

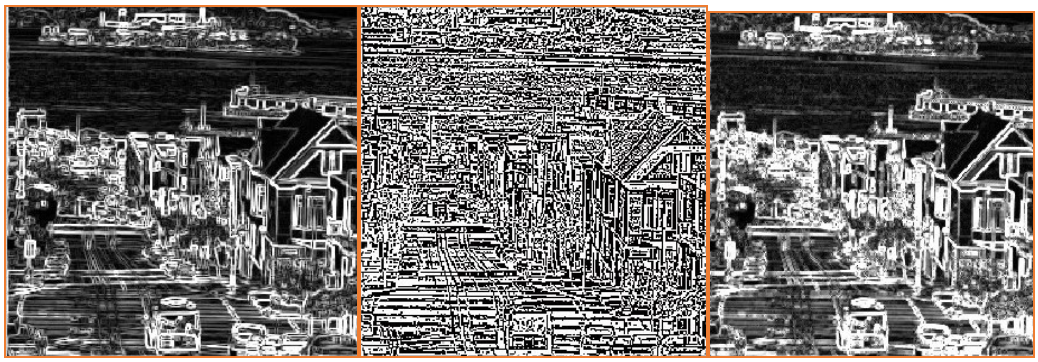

Figure 3. 1) Laplacian of Gaussian 2) Gradient Magnitude 3) Joint Factored Image

3.5.Locally Adaptive Normalization Factor

A 3*3 mask which has values which when summated equals to 1 is applied on the image. As the mask is run over square of joint factored image while finding out the square root of the same, gives normalization factor. Last step of this procedure is to find out new values of *G (i,j)* and L *(i,j)* as$G^{|}(i,j)$ and$L^{|}(i, j)$ by reducing the features by normalisation factor. Variation in Buildings image before and after joint adaptive normalisation are shown in figure 4.

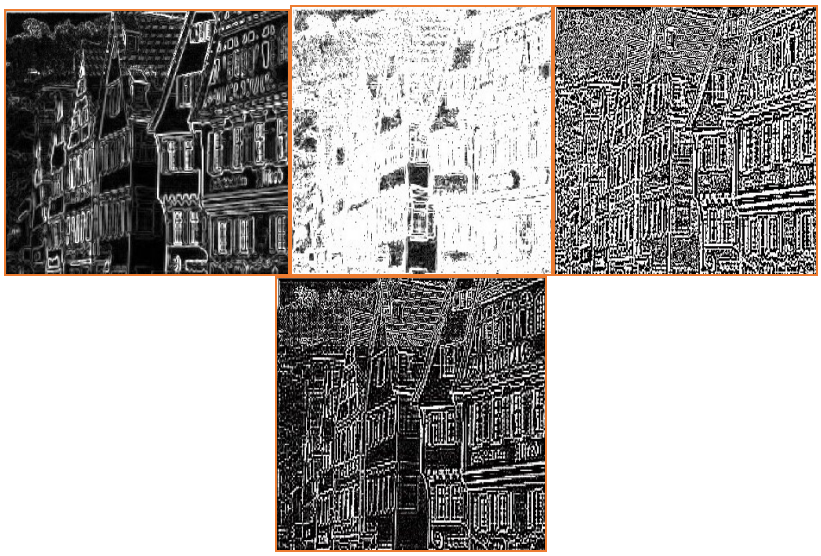

Figure 4. 1) Gradient Magnitude 2) GM after joint adaptive normalisation 3) Laplacian of Gaussian 4) Log after joint adaptive normalisation

3.6.Quantization

The features obtained on applying the techniques of gradient magnitude and Laplacian of Gaussian are quantised. This is performed to decrease the dynamic range and to bring the features into an optimum range. We quantized $G^{|}(i,j)$ into planes as $\{G_1, G_2, .. G_m\}$. Similarly $L^{|}(i,j)$into $\{L_1, L_2, .. L_n\}$. In this case we take 17 levels of which we assign 17 different levels of pixels values. This may be a lossy process but it is done to derive the respective density functions of gradient magnitude and laplacian of Gaussian features. Resultant Trolley image after quantization into 17 levels is shown in figure 5.

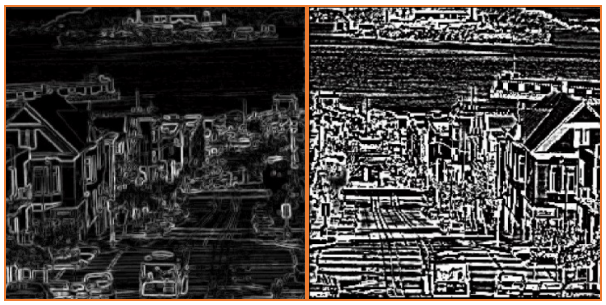

Figure 5. 1) GM quantised into 17 levels 2) LOG quantised into 17 levels

3.7.Marginal Distributions and Conditional Probability

Dependency measures like Marginal distributions and conditional probability closely relate the amount of distortion present in the image. This is more comprehensive evaluation of the extracted features. For the 17 levels of quantized images the marginal distributions and conditional

probabilities are derived. To find out the marginal dependencies of $G^{|}$and $L^{|}$, procedure starts with deriving the joint empirical functions for all levels.

$$JEF_{m,n} = (G^{|} = G_1, G_2, \ldots G_m,\ L^{|} = L_1, L_2, \ldots L_n)$$

Normalised histogram of $G^{|}$ and $L^{|}$is $JEF_{m,n}$. Marginal distributions of $G^{|}$ and $L^{|}$are given in the expression below. Marginal probabilities of $G^{|}$ and $L^{|}$ are shown in the figure 6.

$$\text{Pg } (G^{|}=G_m)=\sum_{n=1}^{N} JEF_{m,n}$$

$$\text{Pl } (L^{|} = L_n))=\sum_{m=1}^{M} JEF_{m,n}$$

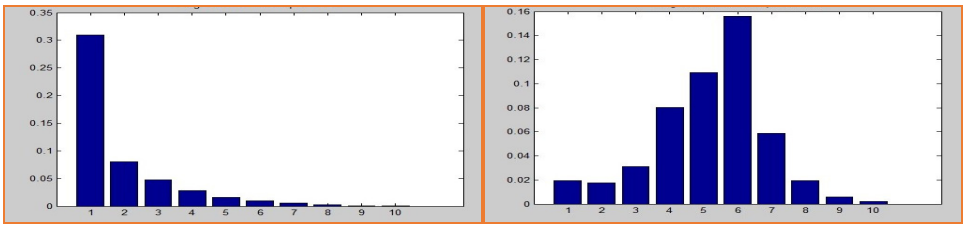

Figure 6. Marginal distributions of quantised$G^{|}$ and $L^{|}$.

Sometimes the marginal distribution does not show the dependencies between $G^{|}$ and $L^{|}$. The dependency between them are derived by dependency measure given in equation below.

$$DEP_{m,n}=\frac{JEF_{m,n}}{P(G^{|}) * P(L^{|})}$$

Using the marginal distributions as the weights the conditional probabilities are derived for $G^{|}$ and $L^{|}$ as Cg and Cl. These probability distributions are otherwise called as the independency distributions. Independency distributions of $G^{|}$ and $L^{|}$ are shown in figure 7.

$$\text{Cg } (G^{|}=G_m)=\text{Pg } (G^{|}) .\frac{1}{N}\sum_{n-1}^{N} DEP_{m,n}$$

$$\text{Cl } (L^{|}=L_N)=\text{Pl } (L^{|}) .\frac{1}{M}\sum_{m=1}^{M} DEP_{m,n}$$

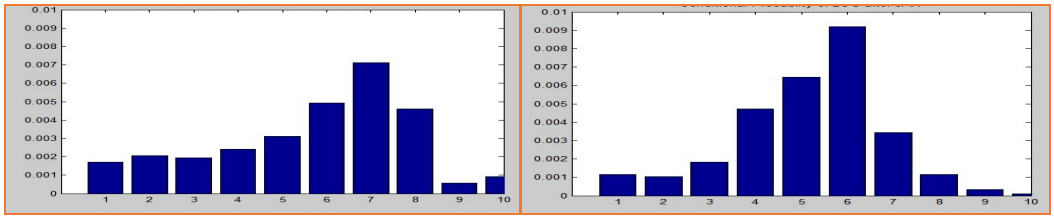

Figure 7. Independency distributions of $G^{|}$ and $L^{|}$.

While finding out the marginal densities of GM and LOG and their corresponding profiles, it is seen that changes in a distorted image and randomness of distortion is distinguishable through. Vertical, horizontal and diagonal profiles of $G^{|}$ and $L^{|}$ of a not distorted are shown in figure 8. A normal distortion less image has quite different distributions from that of a distorted version of it. Similarly their profiles are also plotted. The individual random process of G and L features after quantization are assumed as the random variables. The below figures fall under the assumption of binomial distribution of the data. Further there is need to identify the dependency between the distributions of G and L. Hence, calculating joint probability density function between them is the solution. In a general case they find to be independent and results are in product of their individual marginal density functions. For sample profiles over 20 bins are shown in plots in figure 8.

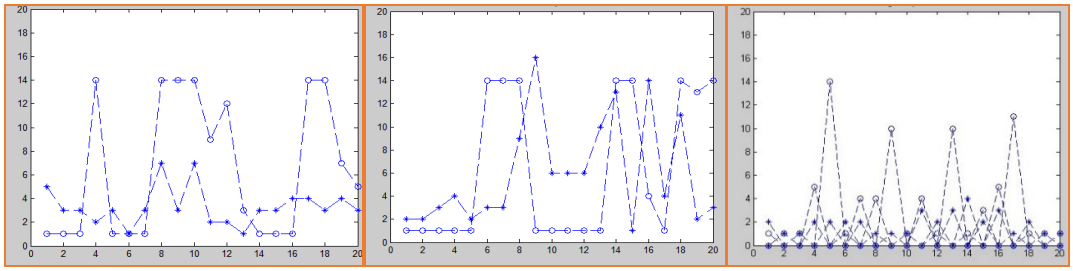

Figure 8. Horizontal, vertical and diagonal profiles of $G^{|}$ and $L^{|}$.

To present the image in the score accurately, two correlations that can measure scores that can measure the relation between structure features are used. They are Spearman rank order correlation coefficient (SRC) and Pearson correlation coefficient *(*PCC).

The dependencies between features of extracted horizontal, vertical and diagonal profiles can formulate the level of distortion in the image. To find out them, spearman and Pearson correlations between Pg, Pl and Cg, Cl are calculated. We propose four models Pearson correlation coefficient between Pg and Pl (PRCP), Pearson correlation coefficient between Cg and Cl (PRCQ), Spearman rank correlation between Pg and Pl (SRCP), Spearman rank correlation between Cg and Cl (SRCQ). The scores of four models and their comparison with Structural similarity value are tabulated in columns below. Highlighted values represent right ordered values in coincidence with level of distortion.

Scores of AWGN distorted images and their relevant SSIM values are recorded in table 1. For Blur, Pearson correlations of conditional probabilities give more equivalence. The scores of blur distorted images and their relevant SSIM values are given in table 2. For AWGN, Spearman correlations of marginal distributions give more equivalence. The scores of images distorted with flicker noise and their relevant SSIM values are recorded in table 3. For flicker noise affected images, Pearson correlations of marginal distributions and conditional probabilities give more equivalence. The scores of JPEG distorted images and their relevant SSIM value are recorded in table 4. For JPEG, Pearson correlations of marginal probabilities give more equivalence. The scores of JPEG2k distorted images and their relevant SSIM values are shown in table 5. For JPEG2k, Spearman correlations of conditional probabilities and Pearson correlations of marginal distributions give more equivalence. Overall, Pearson correlation coefficients of marginal distributions proves to be exemplary.

Table 1. Scores of AWGN distorted images and their relevant SSIM value.

Level of Distortion	PRCP	PRCQ	SRCP	SRCQ	SSIM
1	**0.2368**	**0.9244**	0.3333	**0.8182**	0.9869
2	**0.2688**	**0.9324**	0.2001	**0.8545**	0.9554
3	**0.2791**	0.9239	0.2256	**0.8788**	0.8853
4	**0.2881**	**0.9345**	0.2121	**0.9157**	0.7781
5	0.2881	0.9105	0.9761	**0.9258**	0.6319

Table 2. Scores of Blur distorted images and their relevant SSIM value.

Level of Distortion	PRCP	PRCQ	SRCP	SRCQ	SSIM
1	**0.2299**	0.9362	0.4061	**0.8182**	0.9953
2	**0.2149**	**0.9206**	0.4061	**0.8303**	0.9827
3	**0.2045**	**0.9302**	**0.4061**	0.7455	0.9437
4	**0.1775**	**0.9308**	**0.4499**	**0.8909**	0.8366
5	**0.0941**	0.8739	**0.6383**	**0.9031**	0.6263

Table 3. Scores of Fnoise distorted images and their relevant SSIM value.

Level of Distortion	PRCP	PRCQ	SRCP	SRCQ	SSIM
1	**0.2577**	**0.9464**	0.2485	**0.9031**	0.9908
2	**0.2689**	**0.9407**	**0.2001**	0.8667	0.9667
3	**0.2781**	**0.9321**	0.2485	**0.8909**	0.9162
4	**0.2808**	**0.9174**	**0.2485**	**0.8788**	0.8241
5	**0.3162**	**0.8703**	**0.3051**	**0.7939**	0.6978

Table 4. Scores of JPEG distorted images and their relevant SSIM value.

Level of Distortion	PRCP	PRCQ	SRCP	SRCQ	SSIM
1	**0.2412**	**0.9204**	0.3333	**0.8305**	0.9912
2	**0.2526**	0.8824	0.2485	0.8909	0.9686
3	**0.2371**	**0.9133**	0.3708	**0.8424**	0.9196
4	**0.1706**	**0.8965**	0.3212	**0.8545**	0.7931
5	**0.1498**	**0.8816**	0.3697	**0.9142**	0.6826

Table 5. Scores of JPEG2k distorted images and their relevant SSIM value.

Level of Distortion	PRCP	PRCQ	SRCP	SRCQ	SSIM
1	**0.2414**	0.9134	**0.2918**	0.9031	0.989
2	**0.2321**	0.9064	**0.3333**	0.8788	0.9637
3	**0.1854**	0.8377	**0.3617**	0.9031	0.9008
4	**0.1334**	0.9458	**0.3818**	0.8349	0.7839
5	**0.0741**	0.9203	**0.4394**	0.8788	0.6097

4. CONCLUSIONS

Existing BIQA models are complex and involve either in exquisite decompositions or model learning and support vector regression. Few explicit models unlike the proposed method change the features of the image. Keeping this in concern, an attempt is made to use the correlations between the statistics of the local contrast features. Since these are independent, data of the image is not disturbed. In this paper simple procedures to normalise are used to derive joint statistics with joint adaptive normalisation. Marginal distributions and conditional probabilities and their dependencies led to highly competitive performance. Avoiding the training and learning of the features derived, complexity is reduced. Amongst the four models, Pearson correlation coefficient between Pg and Pl (PRCP) proved to be consistent. However, all the four models have affinity with structural similarity.While Pearson correlation is a linear correlation, Spearman is a rank correlation. Hence results are different for different types of distortions in proposed four models with two correlations because of the variation in structural profiles. This proves that when variation in the image structure can define the type of distortion present in the image.This can lead to development of newer models which can determine the type of distortion.

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AN OPTIMIZED APPROACH FOR FAKE CURRENCY DETECTION USING DISCRETE WAVELET TRANSFORM

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ABSTRACT:

With the increase of modest technology, copy-move forgery detection has grown in a rapid rate that new era of forged images came true which has the same resemblance as the old ones i.e. difficult to find out with naked human perception. Fake currency detection is one in the effect that currency note is tampered in a way such it has the similar resemblance as the original one. So in order to find out the duplicate or forged portion of the image we go for different splicing algorithms using different techniques. Image forgery results to various security issues. Hence an efficient algorithm is required to detect the forgery in images. By using DCT algorithm blocks of the image are represented by DCT coefficients. Presence of blocking articrafts in DCT makes the method to be a drawback. Hence we propose DWT for segmentation of image. Lexicographical sorting is utilized to find out the cloned image blocks. Finally normalization is applied to find the distance in between similar vectors. In DWT provides better resolution and segmentation compared with DCT. In this paper, due to DWT, Image Forgery detection is done on low-level image representation. By using DWT better accuracy in finding out the forgery is achieved in a less time which gradually reduces complexity.

KEYWORDS:

Fake Currency detection, DCT, DWT.

1. INTRODUCTION:

Forgery is the process of making, adapting, or imitating objects, statistics, or documents with the intent to deceive for the sake of altering the public perception, or to earn profit by selling the forged item. [1.]

Forging money or currency is widely often termed as fake or imitation of the original currency. Detection of Image Forgery is done in two techniques:

1. Active Approach
2. Passive Approach

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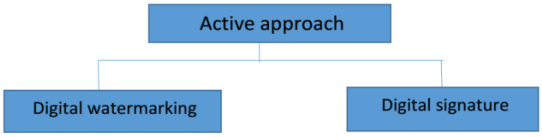
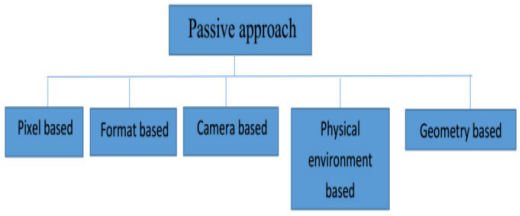
Active Approach:



In the Active approach, Digital images require some pre-processing like Watermarking, or Digital Signatures etc. Digital Watermarking technique is the process of inserting a digital watermark (a known authentication code) into the image at source side, and then this code is being used for verification of digital information at the time of detection.

Passive Approach:



Passive approach is also called Blind approach which requires no prior information about the image. Passive approach clarifies both the location and the amount of forgery is done in an image.

Passive approach has two methods:-

1. Image Source Identification and
2. Tampering Detection

2. IMAGE TAMPERING USING COPY-MOVE FORGERY DETECTION:

It is the widely used technique of copying and replacing the part of an image in context to change the meaning or to hide information of an image [1]. Hence a strong correlation exists between these that can be used as an evidence to detect image tampering or any Copy-move forgery.

If the copied parts are from the same image then it is very difficult to find the original one by extracting hue or any saturation points from the segments as they have the same gradient values and if the copied part of the image has any noise components or any distorted parameters then it is very difficult to find out the segment where it is copied and pasted. And because due to the dawn of new software's these type of image tampering will be very essential to find out.

There are three techniques used to manipulate digital images. They are:

1. **Copy-Move**: This method defines the exact measure of cut, copy and move of one segment of image to other.

2. **Tampering**: it defines the manoeuvring of an image to achieve a drastic change in the other image.
3. **Splicing**: photographic manipulation in which two or more images can be super imposed on a particular image.

Image Tampering Detection based on Frequency Method (Discrete wavelet Transform):

Our method on image tampering detection is completely based on the frequency. The quantization levels are used to calculate the DCT Coefficients by taking a value called as quantization factor Q. By choosing the certain level of Q-factor lexicographically sorting is done before matching. The algorithm used for the DCT may give false positives by matching even mutual errors. However the algorithm cannot differentiate large identical textures of the natural image. Hence we preferred to detect the forged image using DWT and pixel matching. In this method we convert the forged image into Gray-scale image and calculate the DWT to the whole image to obtain sub bands and calculate the offset between copied and pasted regions. As the spatial offsets of the copied and pasted regions of the image are same, we obtain the part where the image is tampered.

Example of a Tampered Image:

Fig1. The left part of the image is the original image taken in the pooling booth during local elections and the right part shows the tampered image.

Example 1. Shows the tampering of an image for the photo taken during elections. The person in the photograph (voter) has shifted from the left part of the image to the right. This image proves how the image tampering provides a disasterous effects during elections.

3. COMPARISON OF DIFFERENT FORGERY DETECTION TECHNIQUES

S.NO	Technique Name	Merits	Demerits
1.	Moment based 1. Blur	1. Lower Computational cost and time. 2. Fast Computation and effective blur identification 3. Less Complexity and need not necessary to know the original image information. 4. Segment of interest is able to identify effectively.	1. Not effective for complex image 2. helpful for small depth of field image 3. large database sampling is needed to prior of detection

			4.Only helpful to motion blur image
	2.HU	1.Robust and effective method detection 2. noise addition , blurring and compression etc., are done for post processing	1. Have many false Positives.
	3.Zernike	1.Flat regions of forgeries are detected	1. Calculating Zernike moment coefficient is complex.
2.	Dimensionality Reduction based 1.PCA	1.Efficient Method 2.Low false Positives	1. Low Efficient for low quality images 2.Low SNR and small blocks
	2.SVD	1. It can accurately measure	
	3.KPCA	1. Exact copy-move region is detected. 2. Works well in noisy compressed image	1. High noised and compressed image 1. block size should be much less than the duplicated image.
	4.PCA-EVD	1. The dimensions of the features are reduced. 2.The accuracy of the detection is good	1.Less Performance in detecting forgeries involving scaling, rotation etc.,
3	Intensity-Based 1.LUO	1.This method is efficient 2.It detects even JPEG compression and Gaussian noise	1. It fails when tampered region is rotated at some arbitrary angles
	2.BRAVO	1.It can accurately detect duplicated	1. Detect

		region	duplication in the region of uniform luminance
	3.CIRCLE	1.Working for post processing like noise addition, blurring , rotating etc	1.Scaling and geometric transformations cannot be detected.
4.	Frequency-Based 1.DCT	1.Copy move region is detected effectively	1.Less performance for any noisy image
	2.DWT	1.Exact copy move region will be detected	1.Works well in noisy and compressed region

In the above table of comparison for different Image Forgery Detection techniques or Real Segment identification of the forged image we are going to perform discrete wavelet Transform which gives better performance in noisy regions and also in the compressed regions. In our Paper, Fake currency note is identified by comparing the threshold values for each and every segment and whenever there is an error in the segmented portion of the image then it is so called tampered portion and it is identified and easily removed by using discrete wavelet transform.

4. PROPOSED METHOD FOR IMAGE TAMPERING IN FORGERY DETECTION USING DWT:

Detection of the tampered images (Forged images) can be easily identified using dwt algorithm. In our paper, we first convert the Original RGB image into a Gray scale image and then observe the quantization levels of the image by using pixel intensity. And if we found any change in quantization values or pixel intensity values then the tampered portion of the image is identified and is shown when the image is converted into its real form as displayed in the results.

Proposed Algorithm Using Discrete Wavelet Transform:

The study of different Seismic signals can be done using different tools of the wavelet known as wavelet transformations. To find out the discrete components of a signal or a part of an image then we go for discrete wavelet transformation by using any of the series of the wavelets i.e. Haar wavelet, Mexican Hat wavelet and Shannon wavelet (which has the poor time resolution).

The proposed algorithm in our project is done in two Phases:

Phase I:
Identification of Matched and Reference Blocks:

In the current Phase of the paper the tampered image is first converted into a gray scale image and then we apply wavelet transformation and convert the overlapping pixels into matrix format and

select the block which has the maximum contrast or max pixel intensity and sort the matrix. After sorting compare the phase correlation between the rows and sort the block into a new matrix which is the detected tampered segmented part of the image.

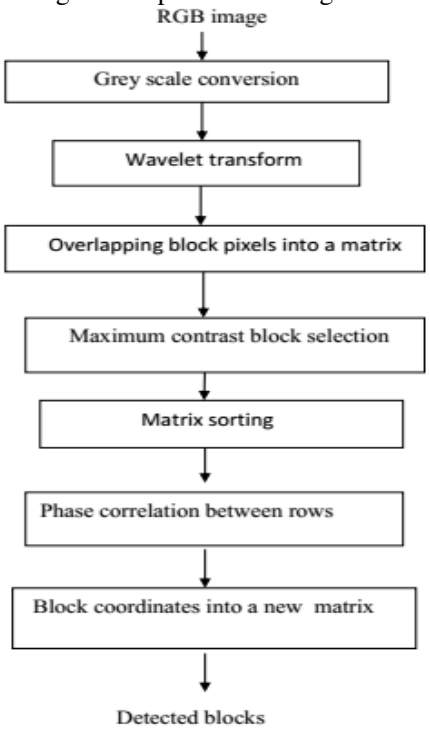


Fig2. Identification of Matched and Reference blocks

Phase II:
Verification on Resembling of Matched and Reference Blocks:

In this phase, a verification on resembling of matched and reference block is done in a robust method as shown in below figure 4.

At first we verify the candidate block of the LL-I image and compare with each and every block in the region of LL-I then compare the region directly with the image LL-II. So we can easily obtain the tampered portions or blocks of an image in a very ideal manner with less noise but the main point to be considered in this phase is the robustness of the algorithm or the process while verifying the identification of the matched and the original image.

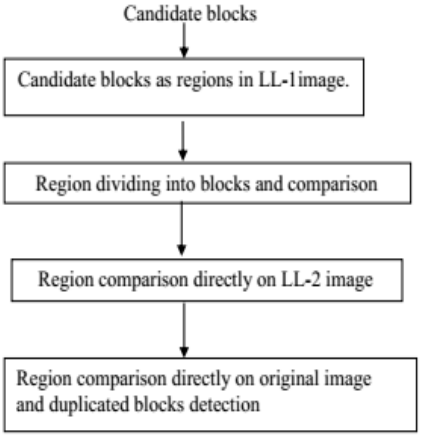


Fig3. Verification on resembling of matched and reference blocks

Proposed Algorithm:

The basic idea of using DWT is it reduces the size of the image at each level, e.g., a square image of size 2k ×2k pixels at level L reduces to size 2k/2 × 2k/2 pixels at level L+1. At each level, the image is spliced into four sub images labelled as LL, LH, HL and HH. LL corresponds to the coarse level coefficients or the approximation image.

In the First Phase the real image is converted into Gray scale image and segmented blocks of tampered image is identified and in the second phase, the discrete wavelet transform is applied for each and every wavelet of the segmented blocks and the tampered parts will be marked and displayed as a result.

Algorithm for Identification of Matched and Reference Blocks: [3]

1. User's image is taken as the input.
2. Convert the RGB image into a Gray scale image.
3. Apply discrete wavelet transform up to level L to the converted gray image.
4. For each overlapping m × m block in the LLL image
   - 4.1. Form a matrix X of dimension m2 columns and (Km+1) × (L-m+1) rows by extracting the resulting pixel values by rows into a row of X.
   - 4.2. Create another matrix Y same as X with two additional columns for storing top-left coordinates.
5. End
6. Highlight blocks where contrast is low.
7. Sort matrix X lexicographically.
8. for each row of X
   - 8.1. Compute the phase correlation for the block corresponding to the current row with the blocks corresponding to "x" rows above and below the current row.
   - 8.2. If the computed maximum phase correlation value exceeds a preset threshold value "T", then store the top left coordinates of the corresponding reference block and the matching block from Y matrix in a new row of a matrix.
9. End

Algorithm for Resembling Verification of Matched and Reference Blocks: [3]

1. For LLL-1 level in the image pyramid
1.1. For each row of the matrix
1.1.1. Form a reference region by padding "l" pixels on all the sides of the m × m reference block.
1.1.2. Form a matching region by padding "l" pixels on all the sides of the m × m matching block.
1.1.3. For each m × m overlapping of the reference region.
1.1.3.1. Find corresponding match in matching region based on Phase correlation but search process has to be opted for selected part of matching region.
1.1.3.2. If the computed maximum phase correlation value exceeds a preset threshold value, then the top left coordinates of the corresponding reference block and the matching block are stored in a new row of a matrix.
1.2. End
2. End
3. For LLL-2 level to original image in the image pyramid
3.1. For each row of the matrix
3.1.1. Form a reference region by padding "l" pixels on all the sides of the m × m reference block.
3.1.2. Form a matching region by padding "l" pixels on all the sides of the m × m matching block.
3.1.3. Compare them using Phase Correlation.
3.1.4. If the computed maximum phase correlation value exceeds a preset threshold value, then store the top left coordinates of the corresponding reference block and the matching block in a new row of a matrix.
3.2 End
4. End
5. Plot the blocks as tampered regions on the given input image.

5. FLOW CHART AND BLOCK DIAGRAM OF THE PROPOSED WORK:

Fig4. Flow Chart of the Proposed Work using DWT

Fig5. Block Diagram of Proposed work using DWT

Procedure for Tampered Image Identification and Marking:

P1: Select any particular image if it is assumed to be tampered and convert the Real image into Gray scale if the image at the input is not represented in Gray level.

P2: Apply Discrete Wavelet Transform

In this step, by applying the discrete wavelet transformation the original size of the image is reduced to half and transmitted to the next level.If the size of the image taken in a square matrix is 2j*2j, then the reduced image using DWT will be 2j/2*2j/2 and the level L is incremented to the next level L+1 which is as shown in the reference image below.

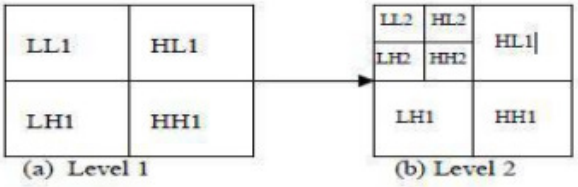


Fig6. (a.) Level 1 and (b.) Level 2

In the next level the image is decomposed into sub images with levels LL, LH, HL, HH as shown in the figure 7.

P3: Lexicographically Sorting:

In this method, the blocks in the matrix "X" is compared instead of Pixels and if it has the same values the algorithm stores the positions of the identical blocks in a separate other matrix "Y" and the counter is incremented with a value.

P4: Normalized shift vector Calculation:

Now the blocks having same segmented values will be compared with a shift vector "S", which increments the shift vector counter "C" to "C+1", after the shift has done and compares it with the normal positioning threshold of the image. The shift vector S can be written as

$$S = (s1, s2) = (p1 - q1, p2 - q2)$$

Where P1, P2 and Q1, Q2 are the positions of the matched blocks.

P5: Match Block Detection

The Blocks which has the same segmented values will be compared with the threshold value which has the smallest size of the segment and the image is re-coloured to show on which part of the image is tampered.

6. SIMULATION OUTPUTS:

Fig7. Original Note

The figure 8, Represents an original 500 rupee note. This note has been forged and we need to identify those tampered regions by using DWT algorithm. This can be done by first converting the RGB colour image into grey scale image this is shown below.

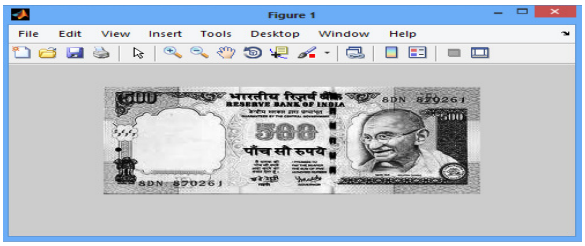


Fig8. Original RGB Converted into Gray scale

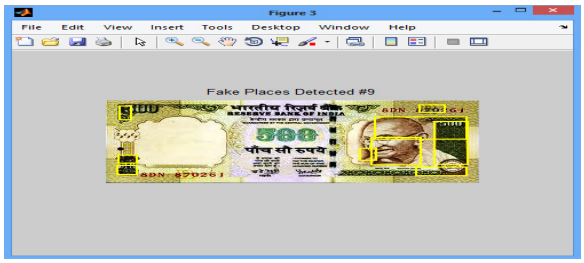


Fig9. Detection of Tampered Regions

The Resultant figure represents the regions in which tampering takes place. This is identified by applying DWT transform and calculating distance between the pixels. If the distance among the neighbouring pixels are same then that regions are said to be forged.

7. CONCLUSION:

Fake currency detection is one in the effect that currency note is tampered in such a way it has the similar resemblance as the original one. Hence an efficient algorithm is required to detect the forgery in images. By using DCT algorithm blocks of the image are represented by DCT coefficients. Presence of blocking articrafts in DCT makes the method to be a drawback. Hence we propose DWT for segmentation of image. Lexicographical sorting is utilized to find out the cloned image blocks. Finally normalization is applied to find the distance in between similar vectors.

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CONTENT BASED IMAGE RETRIEVAL USING GRAY LEVEL CO-OCCURRENCE MATRIX WITH SVD AND LOCAL BINARY PATTERN

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ABSTRACT

In this paper, gray level co-occurrence matrix, gray level co-occurrence matrix with singular value decomposition and local binary pattern are presented for content based image retrieval. Based upon the feature vector parameters of energy, contrast, entropy and distance metrics such as Euclidean distance, Canberra distance, Manhattan distance the retrieval efficiency, precision, and recall of the images are calculated. The retrieval results of the proposed method are tested on Corel-1k database. The results after being investigated shows a significant improvement in terms of average retrieval rate, average retrieval precision and recall of different algorithms such as GLCM, GLCM & SVD, LBP with radius one and LBP with radius two based on different distance metrics.

Keywords

CBIR, GLCM, SVD and LBP.

1. INTRODUCTION:

The image database is increasing fast recently. The capturing of useful images is difficult in the large image database and we obtain frequently useful images, which is widely extending through the Internet. It is not easy to change the situation by using existing methods, so it is a new way to find retrieve images accurately as urgent as possible. Thus image retrieval becomes an essential topic in pattern recognition domain and image processing. Images can be retrieved in three ways generally: content based, text based and semantic based[1–4]. Text based retrieval approach is widely used, such as Google and Baidu, and images can retrieved by using keywords that are annotated on images. However, with this method we have obtained that images are not related to our expected results. The two drawbacks of this approach are firstly, images in the database were manually annoted by annotators and secondly, the retrieval results are poor, because they are similar to the understanding of the query images. The ordinal approach, example, content based image retrieval (CBIR) had been proposed in the early 1990's [4–7]. This approach is based on retrieving the images by using low level features like colour, shape and texture that can represent

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an image. By using this method, we first extract the low level features on an example image, and then compute the similarity between the database images and the query image, finally images are sorted by similarity and the top images will be displayed. CBIR has been shown more subjectively and effectively compared to text based approach [8–9]. The final approach is semantic based method. CBIR has also failed to describe the semantic concepts, so some methods are proposed by researchers for image retrieval by using relevance feedback algorithms. The relevance feedback algorithms capture user's preferences and bridge the semantic gap [10], and the results are closer to human perception. In CBIR, color, shape and texture are the most significant features.

2. FEATURE EXTRACTION METHODS:

2.1 Gray Level Co-occurrence Matrix (GLCM):

The approach, which is the easiest, for texture description is to use statistical moments of the histogram based on intensity of region or image. Gray Level Co-occurrence Matrix is a one of the statistical approach, help to give important information about the relevant position of the neighboring pixels in an image. The gray level co-occurrence matrix P can be defined for an image I of size NxN as $P(i, j) = Nx=1\ Ny=1$, if $I(x, y) = i$ and $I(x + \Delta x, y + \Delta y) = j$, 0 otherwise. Here, the offset $(\Delta x, \Delta y)$, is representing the distance between the neighbor and its pixel of interest. Note that the offset $(\Delta x, \Delta y)$ parameterization makes the gray level co-occurrence matrix sensitive to rotation. Choosing an offset vector, such that the rotation of an image is not equal to 180 degrees, will result in a different gray level co-occurrence matrix for the same (rotated) image. This can be avoided by forming the gray co-occurrence matrix using statistical features of Co-occurrence matrix, of offsets sweeping through 180 degrees at the same distance parameter Δ to achieve a degree of invariant rotation (i.e., $[0\ \Delta]$ for 0°: P horizontal, $[-\Delta, \Delta]$ for 45°: P right diagonal, $[-\Delta\ 0]$ for 90°: P vertical, and $[-\Delta - \Delta]$ for 135°: P left diagonal). Figure 1 illustrates the details to generate the four co-occurrence matrices using Ng =5 levels for the offsets {[0 1], [-1 1], [-1 0], [-1 -1]} that are defined as one neighboring pixel in the possible four directions. We can observe that two neighboring pixels (2, 1) of the input image is reflected in PH concurrence matrix as 3, because there are 3 occurrences of the pixel intensity value 2 and pixel intensity value 1 adjacent to each other in the input image. The neighboring pixels (1, 2) will occur again 3 times in PH, which makes these matrices symmetric. In the same manner, the other three matrices PV, PLD, PRD are calculated.

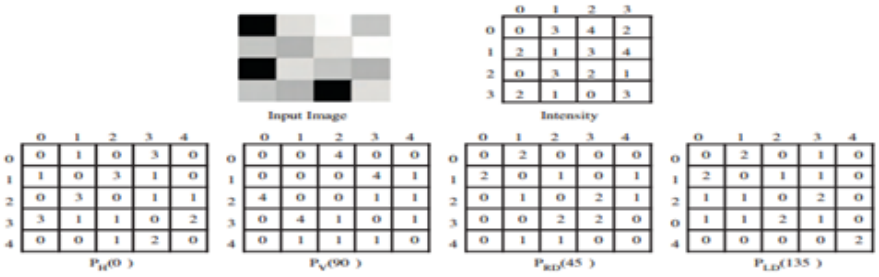

Figure1. Co-occurrence matrix generation for Ng =5 levels and four different offsets: PH (0◦), PV (90◦), PRD (45◦), and PLD (135◦).

2.2 Singular Value Decomposition:

Singular Value Decomposition (SVD) is one of the powerful mathematical tools in linear algebra used in many image processing applications such as image compression, object recognition [11], and image watermarking [12]. SVD is an optimal matrix decomposition technique in a least square sense that it packs the maximum signal energy into few coefficients. Singular value decomposition (SVD) of an image results in three matrices (U, D and V) of same size as that of the original image. U and V represents the left and right singular vectors of the image matrix and D is a diagonal matrix with singular values. Further, singular values extracted by SVD [11] have good performance for shape description. In the SVD of an image, each singular value in the SVD decomposed matrix (D) specifies the luminance of an image layer providing geometrical invariance, while the corresponding pair of singular vectors (U,V) specifies the geometry (structural details) of image layer. According to it, every real matrix *A* can be decomposed into a product of three matrices,

$$A=U\Sigma V^T \tag{1}$$

If A is represented in matrix format:

$$\begin{bmatrix} u_1 & u_2 & u_N \end{bmatrix} \times \begin{bmatrix} \lambda_1 & 0 & 0 & 0 \\ 0 & \lambda_2 & 0 & 0 \\ 0 & 0 & & 0 \\ 0 & 0 & 0 & \lambda_N \end{bmatrix} \times \begin{bmatrix} v_1 & v_2 & . & v_N \end{bmatrix}^T \tag{2}$$

The SVD of matrix A can be written as

$$A = \lambda_1 U_1 V_1 + \lambda_2 U_2 V_2 + ...\lambda_r U_r V_r \tag{3}$$

Where r is the rank of matrix A which is less than or equal to N. The singular values above rank r are zero. *U* and *V* are orthogonal matrices, satisfying the condition $U^TU= I$, $V^TV = I$, and Σ = diag (λ1, λ2, ...). The diagonal entries of Σ are called the singular values of *A*, the columns of *U* are

called the left singular vectors of *A*, and the columns of *V* are called the right singular vectors of *A*.

2.2.1 Properties of Singular Value Decomposition:

1. Existence and Uniqueness: Every matrix A, with real or complex values has singular valued decomposition. .If A is a square matrix and its singular values are distinct, than the left and right singular vectors are determined uniquely up to sign, i.e., a coordinate reflection of each set of singular values.

2. Energy: The largest singular values is related to spectral norm of the matrix A., i.e., $\sigma_1 = \|A\|_2$, while the square root of sum of its squared SVs is equal to Frobenius norm, i.e.

$$\|A\|_F = \left[\sum_{i=1}^{r} \sigma_i^2\right]^{\frac{1}{2}} \tag{4}$$

3. Stability: The SVs have a strong stability since the variation of both original and disturbed SVs cannot exceed 2-norm of the difference between the original and modified matrices.

4. Invariance to geometric distortions: The SVD exhibits the geometric invariance can be expressed in: Translational invariance: Both the matrix A and its translated counterpart has same singular values.

2.3 Local Binary Pattern:

The Local Binary Pattern initially appeared as a generic texture descriptor. The LBP operator gives a label for each pixel of an image by limiting a 3x3 neighborhood with the center pixel value and assuming the result as a binary number. In various publications, the circular 0 and 1 output values are read either clockwise or anti clockwise. In this research, the binary result will be computed by reading the values clockwise, starting from the top left neighbor, as shown below:

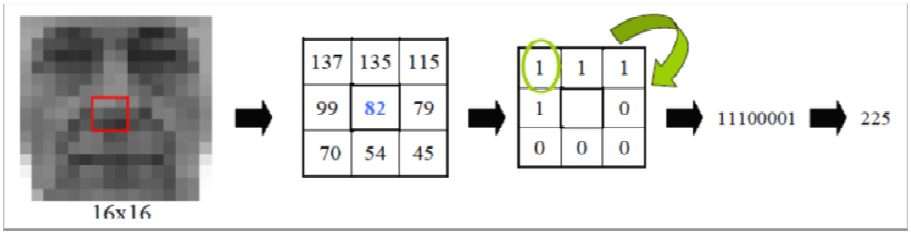

Figure2. LBP labeling: binary label is read clockwise starting from top left neighbor.

In other words, given a pixel position (xc, yc), LBP is defined as an ordered set of binary Comparisons of pixel intensities between the central pixel and its surrounding pixels. The resulting decimal label value of the 8-bit word can be expressed as follows:

$$LBP(x_c, y_c) = \sum_{n=0}^{7} s(l_n - l_c)2^n \tag{5}$$

Where lc corresponds to the grey value of the center pixel (xc, yc), ln to the grey values of the 8surrounding pixels, and function s (k) is defined as:

$$s(k) = \begin{cases} 1 & if \quad k \geq 0 \\ 0 & if \quad k < 0 \end{cases} \tag{6}$$

LBP can be extended as follows:

In order to treat textures at different scales, the Local Binary Pattern operator was extended to use neighborhoods of various sizes. By using the circular neighborhoods and bilinear interpolation of pixel values, any radius and number of samples in the neighborhood can be treated. Hence, the following notation is defined:

(P, R) which means **P** sampling points on a circle of radius **R**.

The following figure shows some examples of different sampling points and radius:

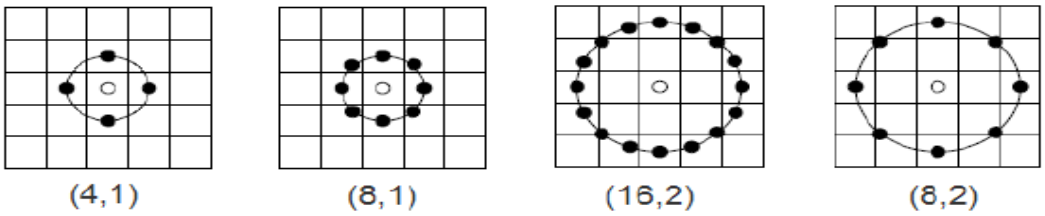

Figure3. LBP different sampling point and radius examples.

In (4,1) LBP case, the four points selected correspond to vertical and horizontal ones, because that faces contain more vertical and horizontal edges than diagonal ones. When computing pixel operations considering the NXN neighborhoods at an image boundary, a portion of the NXN mask is off the image edge. In these cases, various padding techniques are generally used such as repeating border elements, zero-padding or applying a mirror reflection to define an image border. Also, in LBP operator case, the critical boundary, defined by the radius R of the circular operation, cannot be solved padding technique, so the operation is started at an image pixel (R, R). The benefit of this is the final LBP labels histogram will be not influenced by the borders, as the resulting LBP labels image size will be reduced to Width-R X Height-R pixels.

3. FEATURE VECTOR PARAMETERS:

Texture features are a sort of internal visual features which do not based on brightness or color. These features comprise the both surface information and surrounding environment of the image. Texture features can also describe the spatial information of an image quantitatively. Haralick et al. defined 14 feature parameters of gray level co-occurrence matrix for analyzing texture , the study found that only 4 features are not related, namely angular second moment also called energy, moment of inertia also called contrast, entropy and correlation. In our work we use 3 feature parameters; they are energy, entropy and contrast.

3.1 Energy:

Energy is also known as uniformity or the angular second moment. It provides the sum of squared elements in the Gray Level Co-occurrence Matrix. Energy is 1 for a constant image. The energy is given by:

$$\text{Energy} = \sum_{i} \sum_{j} Pd^{2}(i, j) \tag{7}$$

3.2 Entropy:

The entropy of an image can be calculated as

$$\text{Entropy } H = -\sum_{i=0}^{L-1} P_i \ln Pi \tag{8}$$

3.3 Contrast:

Measures the local variations in the gray-level co-occurrence matrix. It reflects the depth of texture grooves and image clarity. Contrast is 0 for a constant image. The contrast is given by

$$\text{Contrast} = \sum_{i} \sum_{j} (i, j)_i^2 Pd(i, j) \tag{9}$$

4. DISTANCE MEASURES:

In image analysis, the distance transform measures the distance of each object point from the nearest boundary and is an important tool in image processing and pattern recognition. In the distance transform, binary image specifies the distance from each pixel to the nearest non-zero pixel. The distance transform provides a metric or measure of the separation of points in the image. The distance metrics used in this retrieving of images are Euclidean distance, Manhattan distance and Canberra distance.

4.1 Euclidean Distance:

The Euclidean distance of two images is given as:

$$d(x,y)=\sqrt{\sum_{i=1}^{n}(X_i-Y_i)^2} \tag{10}$$

4.2 Manhattan Distance:

The Manhattan distance of two images is given as:

$$d(x,y)=\sum_{i=1}^{n}(x_i-y_i)^2 \tag{11}$$

4.3 Canberra Distance:

The Canberra distance of two images is given as:

$$d(x,y)=\sum_{i=1}^{n}\frac{|x_i-y_i|}{|x_i|+|y_i|} \tag{12}$$

5. EXPERIMENTAL RESULTS:

The above mentioned three algorithms are validated through simulation experiments using MATLAB. The Corel image database is used for experimentation; choose 1000 images which are associated with busses, horses, elephants, buildings, mountains, flowers, African people, beaches, and food. Twenty images are randomly selected from each of the ten kinds of images regarded as query images. The above three methods are respectively used to retrieve images.

AVERAGE VALUES OF IMAGES USING 3 DISTANCE METRICS				
Category	**Distance Metric**	**Retrieved Images**	**Precision**	**Recall**
GLCM	Euclidean	23.410	0.234	0.023
	Manhattan	23.410	0.234	0.023
	Canberra	13.070	0.133	0.013
GLCM & SVD	Euclidean	22.900	0.229	0.022
	Manhattan	23.610	0.234	0.023
	Canberra	22.960	0.229	0.022
LBP RADIUS 1	Euclidean	14.130	0.141	0.014
	Manhattan	14.480	0.141	0.014
	Canberra	20.280	0.201	0.020
LBP RADIUS 2	Euclidean	13.321	0.133	0.013
	Manhattan	13.380	0.216	0.021
	Canberra	19.433	0.194	0.019

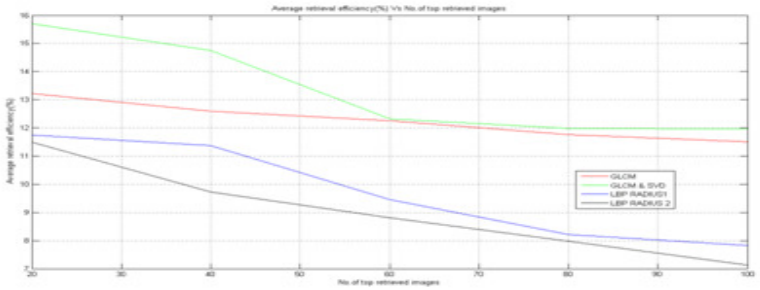

Figure 4. Percentage average retrieval efficiency on Corel 1K database using Euclidean Distance

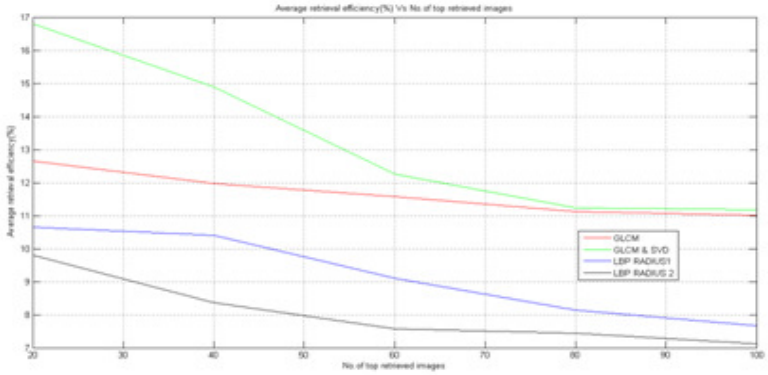

Figure 5. Percentage average retrieval efficiency on Corel 1K database using Manhattan Distance

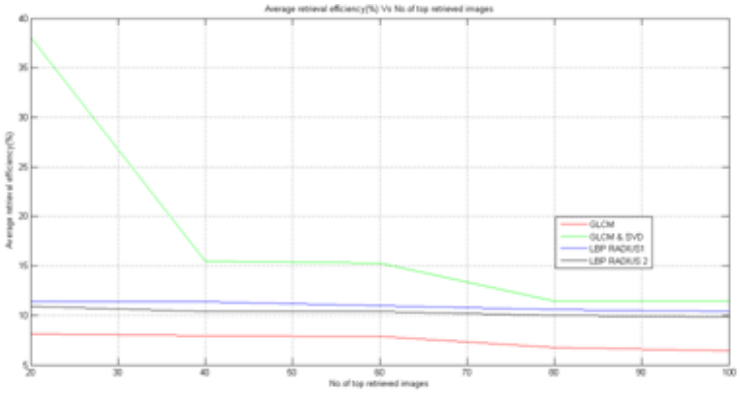

Figure 6. Percentage average retrieval efficiency on Corel 1K database using Canberra Distance

6. CONCULSION:

The CBIR technology can be used in several applications such as social networking sites, forensic labs and image search. CBIR system is a computationally an expensive task. Also it requires a lot of accuracy in the output. The accuracy in this paper has been increased by using various distance metrics such as Canberra distance, Manhattan distance and Euclidean distance on different algorithms such as GLCM, GLCM & SVD, LBP radius1 and LBP radius2 based on feature vector parameters such as energy, contrast, and entropy.

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COLOUR IMAGE SEGMENTATION USING SOFT ROUGH FUZZY-C-MEANS AND MULTI CLASS SVM

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ABSTRACT

Color image segmentation algorithms in the literature segment an image on the basis of color, texture, and also as a fusion of both color and texture. In this paper, a color image segmentation algorithm is proposed by extracting both texture and color features and applying them to the One-Against-All Multi Class Support Vector Machine classifier for segmentation. A novel Power Law Descriptor (PLD) is used for extracting the textural features and homogeneity model is used for obtaining the color features. The Multi Class SVM is trained using the samples obtained from Soft Rough Fuzzy-C-Means (SRFCM) clustering. Fuzzy set based membership functions capably handle the problem of overlapping clusters. The lower and upper approximation concepts of rough sets deal well with uncertainty, vagueness, and incompleteness in data. Parameterization tools are not a prerequisite in defining Soft set theory. The goodness aspects of soft sets, rough sets and fuzzy sets are incorporated in the proposed algorithm to achieve improved segmentation performance. The Power Law Descriptor used for texture feature extraction has the advantage of being dealt in the spatial domain thereby reducing computational complexity. The proposed algorithm is comparable and achieved better performance compared with the state of the art algorithms found in the literature.

KEYWORDS

Segmentation , Classification, Clustering, Fuzzy Sets, Homogeneity, Rough Sets, , Soft Sets, Multi Class SVM, Texture, Power Law Descriptor.

1. INTRODUCTION

Color image segmentation [2] is a pre-processing step of prime importance, used in numerous computer vision and image processing, connected applications such as robotic vision, face recognition, content based image retrieval and medical imaging [5]. Image segmentation algorithms can be categorized into four major groups, thresholding, clustering, edge based and region based segmentation.

Clustering techniques are explored in recent times for color image segmentation. Wang et al., in their work [19] applied the pixel wise homogeneity and texture features to SVM by training SVM, using the features obtained by preliminary clustering with Fuzzy C Means (FCM) algorithm. Lingras [9] et al., proposed rough k means algorithm for use in clustering of internet users, which was later applied for image segmentation applications. Pradipta Maji and Sankar Pal proposed RFCM, [12] in which they presented that, crisp lower bound and fuzzy boundary of a

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class, enables efficient selection of cluster prototypes.Freixenet et al., [8] proposed to integrate the information pertaining to region and boundary for colour texture based segmentation. They experimented and obtained the initial seeds from the regions, by considering perceptual colour and texture edges. The authors proposed "Colour Image Segmentation using Soft Rough Fuzzy C Means Clustering and SMO SVM",[14] in which they explored the parallel processing capability of Sequential Minimal Optimization Support Vector Machine. Deng et al., [6] proposed the well known J-SEGmentation (JSEG) algorithm, which combines both quantization process and clustering techniques for extraction of colour-texture cues in images. Mean Shift clustering in sync with edge information was employed by christoudias et al.,[4] in their work on edge detection and image segmentation (EDISION) system. Colour and texture cues play a predominant rule in segmenting the image. The segmentation algorithms based on clustering are unsupervised and so avoid human intervention.

In this paper, "*Color image segmentation using Soft Rough Fuzzy C Means and Multi Class SVM*" is presented. Initially the color and texture cues of the colour image, at pixel level are obtained through homogeneity and Power Law Descriptor. These features are then applied to Soft Rough Fuzzy C means (SRFCM) clustering algorithm. Later the Multi class SVM classifier is trained by using samples obtained from SRFCM clustering. The image segmentation step is completed with trained Multi Class SVM. The color image information at pixel stage, together with classification capacity of classifier is the major strong point of this technique. Simulated results show that the proposed method achieves better segmentation results. Performance measures compared with state of the art algorithms has been discussed in this paper.

The organization of the paper is as follows. The preliminaries of SRFCM clustering are discussed in Section 2. The basic concepts of Two Class SVM and Multi-Class SVM are discussed in section 3. The fundamentals of Power Law Descriptor are discussed in Section 4.In section 5 the proposed Color image segmentation using SRFCM clustering and Multi class SVM is discussed, followed by justification for using this algorithm. In Section 6 the performance measures used in evaluating the segmentation algorithm are presented. Section 7 shows the pictorial and objective evaluation results of the proposed algorithm. The concluding remarks are given in section 8.

2. SOFT ROUGH FUZZY C-MEANS ALGORITHM (SRFCM)

SRFCM has its roots in the k-means algorithm proposed by J Mc Queen. Fuzzy C-Means (FCM) Algorithm was proposed by Bezdek. In FCM, objects are not confined to belong to a single cluster. Each object belongs to all clusters with certain degree of belongingness. Rough k-means (RKM) was proposed by Lingras and West [9] by borrowing some of the concepts of rough set theory [13]. Rough Fuzzy c-means algorithm was proposed by Mitra et al., [11] . In this paper SRFCM is proposed by applying similarity concepts of soft sets to Rough Fuzzy Frame work.
Many authors were intrigued, and mined the issue of similarity measurement between sets. Majumdar and Samanta [10] presented the theory of similarity measurement of soft sets as follows.

Let $U = \{o_1, o_2, ... o_m\}$ be the set of objects and
$P = \{p_1, p_2, .. p_n\}$ be the set of parameters.
$\hat{Q} = \{F(o_i), i = 1,2,.... m\}$ and
$\hat{R} = \{G(p_i), i = 1,2,..... n\}$ be two groups of fuzzy soft sets.

The similarity between $\hat{Q}$ and $\hat{R}$ is denoted by S ($\hat{Q}$,$\hat{R}$) and is defined as follows $S(\hat{Q},\hat{R}) = \max S_i(\hat{Q},\hat{R})$ where

$$S_i(\hat{Q},\hat{R}) = 1 - \frac{\sum_{j=1}^{n} \left| \hat{Q}_{ij} - \hat{R}_{ij} \right|}{\sum_{j=1}^{n} \left| \hat{Q}_{ij} + \hat{R}_{ij} \right|} \tag{1}$$

The fuzzy soft set based similarity technique is applied to compute the similarity of objects in images. The soft set similarity proposed by Majumdar and Samanta is adapted to the Rough Fuzzy C-Means algorithm by considering that $\hat{Q}$ is the soft set representing the samples and $\hat{R}$ is the soft set representing cluster centroids.

The fundamental steps of SRFCM are as follows.

1. Assume m random initial cluster prototypes denoted by c_i.
2. Find membership u_{ik} between m cluster centers and k data points.
3. Allocate each data point o_k to the lower approximation ($\underline{A}U_i$) or upper approximation ($\overline{A}U_i$ and $\overline{A}U_j$) by calculating $u_{ik} - u_{jk}$, where u_{ik} be maximum and u_{jk} be second maximum membership of a data point o_k among all the clusters. A data point can belong to at most one lower approximation, and may belong to two or more than two upper approximations.
4. If the difference between the highest and next highest membership of a data point in all the clusters i.e ($u_{ik} - u_{jk}$) is below some pre-defined threshold value, then $o_k \in \overline{A}U_i$ and $0_k \in \overline{A}U_j$. It also implies that o_k cannot be a member of any lower approximation. On the other hand if ($u_{ik} - u_{jk}$) is above the threshold value then $o_k \in \underline{A}U_i$ which implies that membership value $u_{ik}$is highest among all the clusters.
5. Compute similarity of sample points soft set to the cluster centre soft set by using the given formula.

$$S_i(\hat{O},\hat{V}) = 1 - \frac{\sum_{j=1}^{n} \left| \hat{O}_{ij} - \hat{V}_{ij} \right|}{\sum_{j=1}^{n} \left| \hat{O}_{ij} + \hat{V}_{ij} \right|} \tag{2}$$

Calculate the maximum similarity and assign a pixel to a cluster to which it has maximum similarity after fuzzification.

6. Compute updated cluster prototype for each cluster U_i, as in (3).

$$v_i = \begin{cases} M_1, & \text{if } \underline{A}U_i \neq \Phi \ \wedge \overline{A}U_i - \underline{A}U_i \neq \Phi, \\ M_2, & \text{if } \underline{A}U_i = \Phi \ \wedge \overline{A}U_i - \underline{A}U_i \neq \Phi, \\ M_3 & otherwise \end{cases}$$

$$M_1 = w_{low} \times \frac{\sum_{o_k \in \underline{A}U_i} u_{ik}^m o_k}{\sum_{o_k \in \underline{B}U_i} u_{ik}^m} + w_{up} \times \frac{\sum_{o_k \in \overline{A}U_i - \underline{A}U_i} u_{ik}^m o_k}{\sum_{o_k \in \overline{A}U_i - \underline{A}U_i} u_{ik}^m}, \qquad M_2 = \frac{\sum_{o_k \in \overline{A}U_i - \underline{A}U_i} u_{ik}^m o_k}{\sum_{o_k \in \overline{A}U_i - \underline{A}U_i} u_{ik}^m} \qquad M_3 = \frac{\sum_{o_k \in \underline{A}U_i} u_{ik}^m o_k}{\sum_{o_k \in \underline{A}U_i} u_{ik}^m} \tag{3}$$

7.Iterate and run steps 2–6 until there are no further changes in cluster centroids. The weights (w_{up}, w_{low})are chosen to be values between 0 and 1.Further (w_{up}+w_{low}) = 1; (1/2 < w_{low}<1), 0 < T <0.5.

3. MULTI CLASS SUPPORT VECTOR MACHINE

3.1 Two Class SVM

Support vector machine (SVM) [5] in general is used to solve classification problems encountered in pattern recognition. Two class SVM is used to divide data into two sets of classes, by estimating the location of a slicing plane that optimizes (increases) the smallest distance between any two groups. Different hyper planes separate the data, but the hyper plane that optimizes the distance 2/w between the classes has to be found. SVM require training data which are manually annotated. The training data is used as reference for automatic classification of unclassified data. Let the training data be (x_i, y_i) and the corresponding output be $y_i \in$(-1,+1). SVM is modelled as

$$y = w^T x + b \tag{4}$$

where b is bias and w is weighted vector with dimensions akin to that of feature space.

SVM is formulated by assuming that given data can be linearly separated as given below.

$$\begin{aligned} w^T x_i + b &\geq +1 (y_i = +1) \\ w^T x_i + b &\geq -1 (y_i = -1) \end{aligned} \tag{5}$$

The margin m is thus

$$m = \frac{1}{\|\overline{w}\|^2} \tag{6}$$

Maximum margin implies minimum w, and the problem is solved as follows

$\min_{w,b} \frac{1}{2} \|w\|^2$ with the constraint

$$y_i \left(\overline{w} . \overline{x} - b \right) \geq 1 \qquad \forall i \tag{7}$$

where x_i is the i^{th} training data point and y_i is the expected response of the SVM for i^{th} training data point. The value of y_i is +1 for the excitations from group 1 and -1 for excitations from group 2.

3.2 Multi-Class Support Vector Machine Using One-Against-All Approach

This method is also called one-against-rest classification[5].To solve a classification problem in which a given set of data points is to be categorized into N classes, N SVM binary classifiers are created, where each individual classifier discriminates , each class from the remaining (N-1) classes. To elaborate, the first binary classifier is trained to distinguish class-1 data points and the

data points belonging to the other classes. Data points are classified by maximizing the location of the data point from the periphery of the linear slicing hyper plane. The final output class is the one that corresponds to the SVM with the largest peripheral distance. Nevertheless, if the responses of two or more classes are indistinguishable, those points are marked as unclassified, and are arbitrarily resolved. The multiclass method discussed is advantageous in the sense that the number of binary classifiers constructed is of the order of the number of classes. The hitch, however is that, in the training phase, the memory necessity is very high and is of the order of square of the selected training samples.

4. POWER LAW DESCRIPTOR:

The proposed texture descriptor is an extension to the Weber Local Descriptor proposed by Chen et al.,[3].

Ernst Weber observed that the ratio of incremental threshold to the background intensity is a constant [1]. This relation known since as weber's law can be expressed as:

$$\frac{\Delta I}{I} = k \tag{8}$$

0	0	0
0	1	0
0	0	0

1	1	1
1	-8	1
1	1	1

x_o	x_1	x_2
x_7	x_c	x_3
x_6	x_5	x_4

where ΔI represents the increment threshold (just noticeable difference for discrimination); I represents the initial stimulus intensity and k signifies that the proportion on left side of the equation remains constant despite variations in the I term. The fraction $\Delta I / I$ is known as the Weber fraction. Weber's law more simply stated says that the size of a just noticeable difference is a constant proportion of the original stimulus value. So, for example, in a noisy environment one must shout to be heard while a whisper works in a quiet room.

Chen et al., [3] proposed Weber Local Descriptor, as a texture descriptor, by considering the concepts of weber's law. But Guilford observed that empirical data such as an image does not always fit well into weber's law. He suggested a modification to weber's law as follows and hence called as Guilford power law[1].

$$\frac{\Delta I}{I^{\alpha}} = k \tag{9}$$

where α is an exponent slightly less than 1.The perceived brightness of the human eye is proportional to the logarithm of actual pixel value, rather than the pixel value itself. The power law is also scale invariant. Hence the proposed power law descriptor models the perception of human beings better than weber local descriptor

The Power law descriptor consists of two components differential excitation (ξ) and orientation (θ)

Differential excitation finds the salient variations within an image to simulate the pattern perception of human beings. It is defined as the ratio between two terms V_s^{00} and $[V_s^{01}]^{\alpha}$.

$$\xi(x_c) = \arctan\left[\frac{v_s^{00}}{[v_s^{01}]^{\alpha}}\right] \tag{10}$$

where V_s^{00} at any pixel is the sum of the differences between the neighbors and the current pixel, whereas V_s^{01} is the value of the current pixel to a power of α

$$V_s^{00} = \sum_{i=0}^{p-1}(\Delta x_i) = \sum_{i=0}^{p-1}(x_i - x_c) \tag{11}$$

These values are obtained by convolving the image with the following filters.

Filter used to realize V_s^{00} Filter used to realize V_s^{01} Template

The orientation component is the gradient orientation which is computed as

$$\theta(x_c) = \gamma_s^1 = \arctan\left[\frac{v_s^{11}}{v_s^{10}}\right] \tag{12}$$

$V_s^{10} = x_5 - x_1$ and $V_s^{11} = x_7 - x_3$

0	-1	0
0	0	0
0	1	0

0	0	0
1	0	-1
0	0	0

where V_s^{11} and V_s^{10} are obtained using the following filters

Filter used to realize V_s^{10} Filter used to realize V_s^{11}

Both the orientation and excitation values range in the interval
$[-\pi/2, \pi/2]$

Finally the two dimensional histogram of the differential excitation and orientation component is the texture descriptor used in the segmentation process.

The Texture feature is expressed as

$$TF_{ij}^{k} = 2D\ Histogram\ [\xi(x_c), \theta(x_c)]_{ij} \quad k = L, a, b \tag{13}$$

5. IMAGE SEGMENTATION USING SRFCM AND MULTI CLASS SVM (PROPOSED METHOD)

5.1 Algorithm Steps

1. Color, texture and spatial feature cues are extracted from the image. Homogeneity model is used to extract color features and Local Binary Pattern for texture features. Additionally the spatial information is embedded in the feature vector to nullify the effect of noise and outliers.
2. SRFCM based clustering is applied on the feature space for selecting the training samples which are to be applied to the Multi class SVM classifier in next stage of segmentation.
3. Multi Class SVM training
The One-Against-All Multi Class SVM classifier is trained using samples obtained from preceding step. For image pixels in j^{th} cluster some pixels are chosen as training samples remaining are used as test samples.
4. Multi SVM pixel classification
Apply the test set to SVM for classifying new data. Combine test set and training set to obtain the final segmentation result.

5.2 Colour Feature Calculation

All the pixels in the image are marked as homogenous region pertaining to an object. The image segmentation task is now a classification problem and the process of segmentation is aimed at assigning a label to each individual pixel or an entire region based on homogeneity. Color features are extracted from the Lab color model, because color difference can be measured conveniently in *LAB* color space.

Let $C_{ij} = (C_{ij}^{L}, C_{ij}^{a}, C_{ij}^{b})$ be the representation of color components in Lab colour model, corresponding to a pixel at the point (i,j) in an image. The colour feature CF_{ij}^{k} , k=L, a, b is derived from the color component C_{ij}^{k} , k=L, a, b as follows.

1.Prepare a window of size 3×3 for construction of pixel-level color feature.
2.Calculate pixel wise color feature CF_{ij}^{k} related to the color component C_{ij}^{k}, using pixel homogeneity, extracted from image, so that it reflects the uniformity of an image object. Pixel variance in terms of standard deviation and discontinuity in terms of edge detection, of color component C_{ij}^{k} are calculated. The product of normalized standard deviation and normalized edge discontinuity information is deducted from unity to obtain pixel homogeneity of the objects in the image.

Standard deviation and mean are defined as shown below. They are defined for each color feature C_{ij}^{k}(k=L,a,b) at location (i,j).

$$v_{ij}^{k} = \sqrt{\frac{1}{d^{2}} \sum_{m=i-\left(\frac{d-1}{2}\right)}^{i+\left(\frac{d-1}{2}\right)} \sum_{n=j-\left(\frac{d-1}{2}\right)}^{j+\left(\frac{d-1}{2}\right)} \left(c_{mn}^{k} - \mu_{ij}^{k}\right)^{2}} \tag{14}$$

and

$$\mu_{ij}^{k} = \frac{1}{d^2} \sum_{m=i-\left(\frac{d-1}{2}\right)}^{i+\left(\frac{d-1}{2}\right)} \sum_{n=j-\left(\frac{d-1}{2}\right)}^{j+\left(\frac{d-1}{2}\right)} c_{mn}^{k} \tag{15}$$

where μ_{ij}^{k} is mean of color component $c_{ij}^{k}(k = L,a,b)$

The edge variations are calculated in terms of the absolute value of first order derivative.

Let e_{ij}^{k}, k=L,a,b represent the gradient operator at a point (i,j) in the image. Gradient operator indicates the rate of change at any point in the image.

$$e_{ij}^{k} = \sqrt{(G_x^k)^2 + (G_y^k)^2} \tag{16}$$

(G_x^k) *and* (G_y^k) are composed of gradient components in x and y dimensions .

$$V_{ij}^{k} = \frac{v_{ij}^{k}}{v_{\max}^{k}}, E_{ij}^{k} = \frac{e_{ij}^{k}}{e_{\max}^{k}} \tag{17}$$

$$where \quad v_{\max}^{k} = \max\{ v_{ij}^{k} \},\ e_{\max}^{k} = \max\{ e_{ij}^{k} \},\ (0 \le i \le M-1, 0 \le j \le N-1), k = L,a,b$$

The colour feature is expressed as

$$CF_{ij}^{k} = H_{ij}^{k} = 1 - E_{ij}^{k} \times V_{ij}^{k},\ (0 \le i \le M-1, 0 \le j \le N-1),\ k = L,a,b \tag{18}$$

5.3 Texture Feature Extraction by Power Law Descriptor

The proposed power law Descriptor is a robust local texture descriptor which is resistant to illumination changes.

The procedural steps for texture feature extraction is as follows

1) Convert the given image into a gray scale image.
2) Calculate the Differential excitation values of the gray scale image and obtain the Differential excitation image.
3) Calculate the orientation values of the gray scale image and obtain the orientation component at each pixel location.
4) Find the 2-D histogram of Differential excitation and orientation values at each pixel location in a 3X3 neighbourhood.
5) The resulting histogram at pixel location (i,j) forms the texture feature $TF_{i,j}$for SRFCM clustering algorithm.

6. PERFORMANCE MEASURES

The Performance measures proposed by Unni Krishnan et al., [16] which are Rand Index (RI), Variation of Information (VOI), Global Consistency Error (GCE), and Boundary Displacement

Error (BDE) are used in evaluating and comparing our segmentation results with benchmark algorithms.

6.1 Rand Index

The Rand index indicates the proportion of pixels which are in agreement between the Computed Segmentation (CS) and the Ground Truth (GT). [16].

The rand index ranges between 0 and 1, where 0 confirms that CS and GT do not have common attributes and 1 confirms that CS and GT are indistinguishable.

6.2Variation of Information

The variation of information (VOI) is a measure that specifies the variation between computed segmentation and ground Truth .The lower is the value of VOI, the better is the segmentation result.

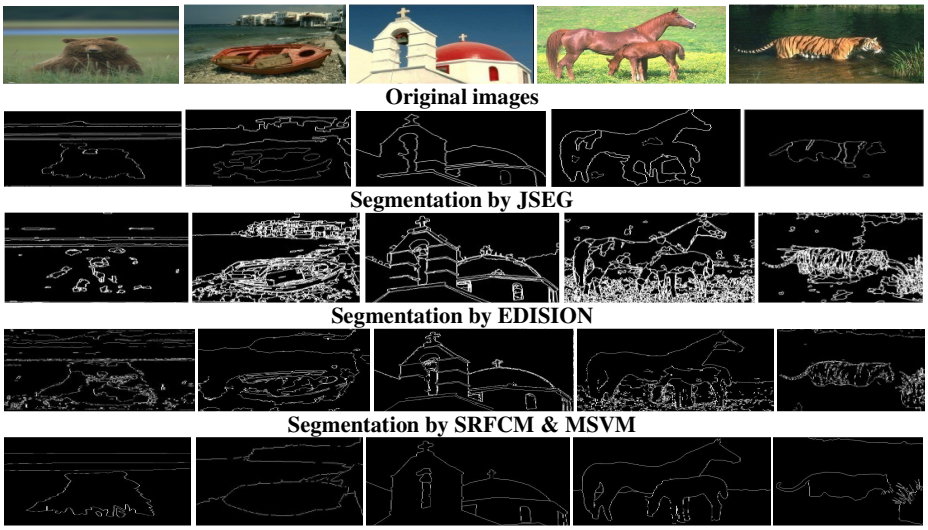
6.3 Global Consistency Error

Global consistency error is a measure of the limits to which the computed segmentation can be seen as transformation of Ground Truth towards Computed Segmentation. If one segment is proper subset of the other, then the pixel lies in an area of refinement, and the error should be zero. If there is no subset relationship, then the two regions overlap.GCE ranges between 0 and 1, where 0 signifies no error . Lower the value of GCE better is the segmentation result.

6.4 Boundary Displacement Error

The Boundary Displacement Error is a measure of the displacement error averaged between boundary pixels in computed segmentation and the nearest boundary pixels in the ground truth. BDE should be low for good segmentation.

7. RESULTS AND DISCUSSION



Human Labelled Segmentations (Ground Truths)

TABLE 1: RI& VOI

Image	RI			VOI		
	MSVM	JSEG	EDI	MSVM	JSEG	EDI
Bear	0.68	0.61	0.68	3.42	2.09	2.55
Boat	0.54	0.45	0.46	3.63	3.64	5.61
Church	0.72	0.45	0.67	2.70	3.03	3.06
Horse	0.60	0.45	0.46	3.30	3.34	5.33
Tiger	0.63	0.47	0.54	2.60	2.63	4.15

TABLE 2: GCE & BDE

Image	GCE			BDE		
	MSVM	JSEG	EDI	MSVM	JSEG	EDI
Bear	0.16	0.19	0.19	5.73	6.12	6.00
Boat	0.34	0.32	0.31	3.43	4.22	3.45
Church	0.18	0.21	0.19	6.87	10.24	8.74
Horse	0.24	0.25	0.24	5.32	7.29	5.86
Tiger	0.18	0.20	0.19	10.63	13.05	9.49

The experimental results show the performance comparison of the proposed algorithm, with state of the art JSEG algorithm [4] and EDISION [6] scheme. Five images with colour and texture variance from Berkeley Segmentation database are used for comparison. It can be observed that the JSEG algorithm could not identify the bush on the bottom right of the tiger image , and also the difference in colour between water and bush texture on the top portion of the image, where as the proposed algorithm could identify both, which claims the superiority of the proposed algorithm. The image segmentation by EDISION scheme for the same image is over segmented

as can be seen in the results, further displaying the superiority of the proposed algorithm. The algorithms have been implemented in Matlab 2014a using P-IV processor system with 4GB RAM. The observations in the table shows that SRFCM & MSVM out performs the algorithms in [4] and [6] in terms of rand index for the presented images. It can be observed that the proposed algorithm exhibits better performance results for most of the images in terms of RI, VOI, GCE and BDE.

8. CONCLUSION

The developed approach is a robust technique which integrates the strengths of three soft computing techniques which viz., rough sets, soft sets and fuzzy sets. The results obtained from this hybridization are later applied to the well-known machine learning tool, Multi Class Support Vector Machine for segmentation. Extensive Experimentation has been done on a lot of images from Berkeley segmentation database which consists of 500 natural color images along with their Ground Truths. The effectiveness of proposed algorithm is demonstrated along with the comparison with other state of the art algorithms. The results shows that in soft rough fuzzy c-means clustering with Multi Class Support Vector Machine, inter cluster distance has been maximized and intra clustering distance has been minimized. Various performance metrics have been compared and the proposed algorithm shows better results compared with other existing benchmark algorithms. The proposed algorithm can also be extended to evolutionary algorithms which increases the clustering accuracy. The proposed algorithm can also be used with noisy color images.

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TWO-DIMENSIONAL OBJECT DETECTION USING ACCUMULATED CELL AVERAGE CONSTANT FALSE ALARM RATE

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ABSTRACT

The extensive work in SONAR is oceanic Engineering which is one of the most developing researches in engineering. The SideScan Sonars (SSS) are one of the most utilized devices to obtain acoustic images of the seafloor. This paper proposes an approach for developing an efficient system for automatic object detection utilizing the technique of accumulated cell average-constant false alarm rate in 2D (ACA-CFAR-2D), where the optimization of the computational effort is achieved. This approach employs image segmentation as preprocessing step for object detection, which have provided similar results with other approaches like undecimated discrete wavelet transform (UDWT), watershed and active contour techniques. The SSS sea bottom images are segmented for the 2D object detection using these four techniques and the segmented images are compared along with the experimental results of the proportion of segmented image (P) and runtime in seconds (T) are presented.

KEYWORDS

Accumulated cell average- constant false alarm rate (ACA-CFAR), two-dimensional object detection, side scan sonar (SSS), Active contour, Watershed and undecimated discrete wavelet transform.

1. INTRODUCTION

SONAR is an acronym for Sound Navigation and Ranging is a procedurethat utilizes sound propagation usually underwater, as in submarine route to research, identify different vessels. Sonar framework gives a close-photographic high determination images of submerged territories, even in water with poor optical transparency. Most of the underwater tasks, such as the pipeline investigation and maintenance, resources, search, mine identification,or debris recognition, is mean to be delivered in anautomatic way by utilizing autonomous underwater vehicles(AUV). A group of objective detection methods widely used in the technology of radio detection and ranging(RADAR) is known asconstant false alarm rate. This group of techniques, keep up a CFAR, where interference energy must be approximated with the data. The probability of expected false alarm (p_{fa}) is preserved by setting up the detection threshold. If the interference energy and the threshold are evaluatedby the average of the estimate of thenearby cells, this approximation is denominated cell averaging-constant false alarm Rate (CA-CFAR). Since the

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technology of sonaris close to the radar technology, the proposal of this work is to migrate the mentioned radar detection techniquefor the object detection in the sea bottom, such as pipeline, from acoustic images.

2. RELATED WORK

The existing segmentation algorithms used for acoustical images change in accuracy, validity, speed, complexity and resources for computation.The algorithm employed for the seabed segmentation which reduces the issues such as the computationally expensive mathematical models used for the unsupervised segmentation of the seabed is the undecimated discrete wavelet transform (UDWT). The authors in [2] constructed a feature vector for each pixel utilizing the intra and inter resolution sampling data for the whole input image and has used the principle component analysis (PCA) for the reducing the dimensionality of this feature vector space. Finally, the segmentation is used to cluster by k-means such that the feature vectors are divided into disjoint classes.Constant false alarm rate is a technique used for target detection in the radar technology, which are described in detail in [9]. Then, another technique called as the cell-averaging constant false alarm rate (CA-CFAR) [9] which is an approximation technique was introduced such that the adaptive detection threshold is attuned for maintaining the probability of expected false alarm by maintaining the n adjacent cell average interference power values. The work done by the author in [A] has inspired the change of idea from radar to sonar by using the acoustic reverberation power as the interference power in radar.

The aim of this work is segmentation of the seabed intotwo sorts of regions: acoustic highlight and seabed reverberation areas. The proposed work uses a 2-D extension of accumulated cell averaging-constant false alarm rate (ACA-CFAR) for the object detection. Initially, the SSS images are denoised by employing undecimated discrete wavelet transform (UDWT) and then the resultant denoised image feature dimension is compressed by utilizing the singular value decomposition (SVD). The decreased feature space is segmented by the k-means clustering for obtaining the different disjoint classes used for segmentation purpose. This disjoint classes are further used for target detection by subjecting them to the 2D ACA-CFAR technique. This work aims to reduce the computational resources and complexity rather losing robustness.This work is further compared by with active contours, UDWT and watershed technique for image segmentation in order to detect an object. The remainder of this paper is organized as follows. Section 2 establishes the basic concepts and previous work done in the field of the object detection using CA–CFAR. Section 3 shows the method of ACA-CFAR - 2D. In Section 4 presents the experimental comparison and the results and the analysis made. Lastly, Section 5 presents the conclusions arrived.

3. METHODOLOGY

This following section presents the detailed procedure used in this proposed work and the figure 1 depicts the methodology employed.

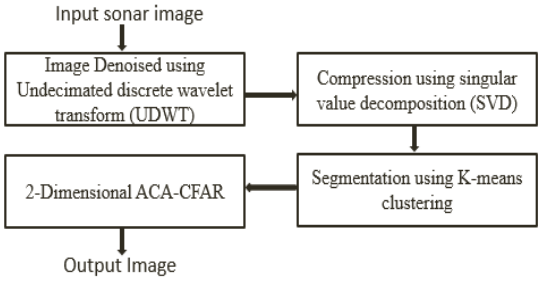

Fig. 1. Flow chart of proposed algorithm

3.1 Sidescan sonar image segmentation

Scan Sonar Image Segmentation is a process of image partitioning into significant parts that are relatively homogenous. Regions may correspond to a particular object, or different parts of an object.This is typically used to identify objects or other relevant information in digital images.

3.1.1. Image denoising using undecimated discrete wavelet transform (UDWT)

The undecimated discrete wavelet transform (UDWT) is a wavelet transform algorithm designed to overcome the defiency of translation-invariance of the discrete wavelet transform (DWT). By eliminating down samples in the DWT, translation-invariance can be achieved.

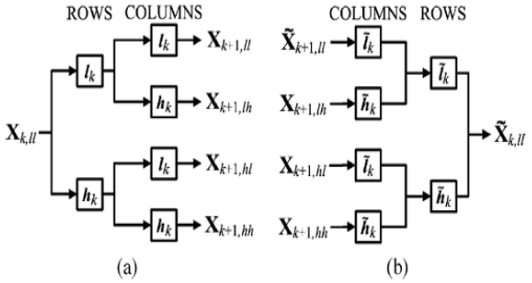

Fig. 2. One-level filter bank UDWT implementatio

(a) Forward transform. (b) Inverse transform

3.1.2. Compression using singular value decomposition

Image Compression deals with the representation of an image with minimal number of bits.Compression is achieved by minimizing the redundancies in an image. Compression is needed for saving bandwidth, memory, and cost. In this work, Singular value decomposition (SVD) approach is used for image compression. When an image is transformed using SVD, it is not constricted, but the data involves a phase in which the singular value has a great quantity of the image data. This means that few singular values can be applied to represent the image with a little different from the original image.

3.1.3. Segmentation using k-means clustering

Clustering is a classification of object into different groups which is achieved by using K-means clustering. It is an algorithm which partitions an image by assigning each and every point to a cluster with centroid/middle is nearest, where the middle constitutes the average of all phases in the cluster.

3.2 Cell average-constant false alarm rate for object detection

A false alarm is an erroneous radar target detection decision caused by noise or other interfering signals exceeding the detection threshold, this false alarm can be solved by implementing CFAR which maintains a false alarm probability as constant such that the threshold is updated in accordance with the estimated noise variance.

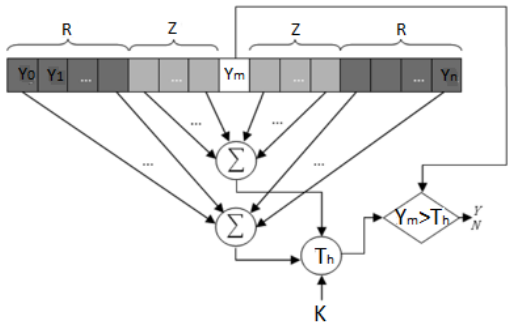

Fig. 3. General architecture of CA-CFAR process

Cell averaging is implemented on the set of range cells. The center cell of CFAR window is contained the object which called “Cell under Test”. These unused cells are then called guard cells and the remaining cells are reference. The two adjacent cells are added and multiplied by a constant to establish a threshold level for attaining the desired probability of false alarm.

$$\overline{P}_{fal} = (1+\frac{k}{R_c})^{-R_c} \tag{1}$$

Where

- $\overline{P}_{fal}$ is the false alarm probability.
- R_c is the total number of reference cells.
- K is a constant.
- CFAR is setting the threshold according to measured background.

$$\hat{T} = \frac{k}{R_c} \sum_{m=1}^{R_c} y_m \tag{2}$$

Where

- $\hat{T}$ is the calculated threshold
- y_m is the cell under test

3.2.1. Two dimensional Accumulated CA-CFAR

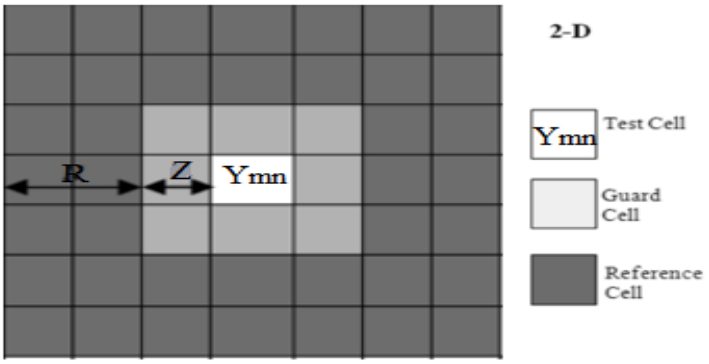

Fig. 4. Generic CA-CFAR window for 2-D.

	0	1	2	3	4	5
0	Acu_{11}	Acu_{12}	Acu_{13}	Acu_{14}	Acu_{15}	Acu_{16}
1	Acu_{21}	Acu_{22}	Acu_{23}	Acu_{24}	Acu_{25}	Acu_{26}
2	Acu_{31}	Acu_{32}	Acu_{33}	Acu_{34}	Acu_{35}	Acu_{36}
3	Acu_{41}	Acu_{42}	Acu_{43}	Acu_{44}	Acu_{45}	Acu_{46}
4	Acu_{51}	Acu_{52}	Acu_{53}	Acu_{54}	Acu_{55}	Acu_{56}
5	Acu_{61}	Acu_{62}	Acu_{63}	Acu_{64}	Acu_{65}	Acu_{66}

Fig. 5. Sample accumulated matrix using (5) for ACA-CFAR - 2D.

The Figure. 5 presents an example of the sample matrix y_{mn} (with m=1 . . . r and n=1 . . .c where r and c are the row and column sizes, respectively). The guard distance is the distance between the test and far cell in the guard window, which is given as d_z = G. In the same way, the reference distancegiven by d_{re} = N + G is the distance from the test to farthest cell in the reference window. The entire number of Reference cells can be measured with

$$R_c = (2.d_{re} + 1)^2 \tag{3}$$

The entire number of Reference cells can be measured with

$$Z_c = (2.d_g + 1)^2 \quad (4)$$

The ACA-CFAR - 2D method calculates an accumulated absolute sample or Acu_{rc}, for eachcell, using

$$Acu_{rc} = \sum_{m=1}^{r} \sum_{n=1}^{c} y_{mn} \quad (5)$$

Reference cell computations

$$\sum_{rc} = Acu_{dre + r,dre + c} - Acu_{r - dre - 1,dre + c} - Acu_{dre + r,c - dre - 1} + Acu_{r - dre - 1, c - dre - 1} \quad (6)$$

Guard cell computations

$$\sum_{rc} = Acu_{dz + r,dz + c} - Acu_{r - dz - 1,dz + c} - Acu_{dz + r,c - dz - 1} + Acu_{r - dz - 1, c - dz - 1} \quad (7)$$

4. OBJECT ANALYSIS AND RECOGNITION

Our object recognition approach was used in order to speed up the object recognition process bySimplifying these objects to the nearest geometrical shape.Acquired sonar images, which was employed for recognizing the object by applying proposed approach.The suggested approach can be summed up the next steps:

4.1 Denoising sonar image using undecimated wavelet transform

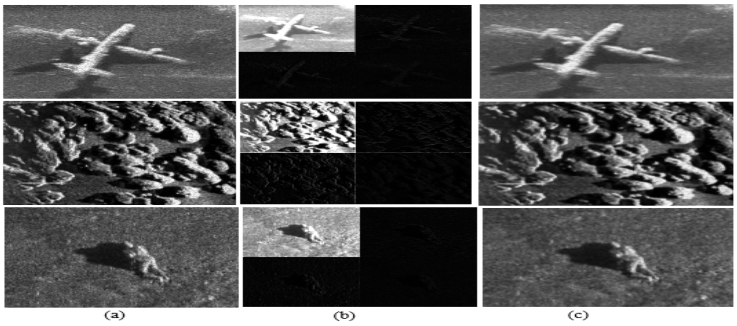

Fig. 6. Sea bottom denoised image using UDWT (a) input sidescan sonar image (b) single level decomposition (c) denoised image.

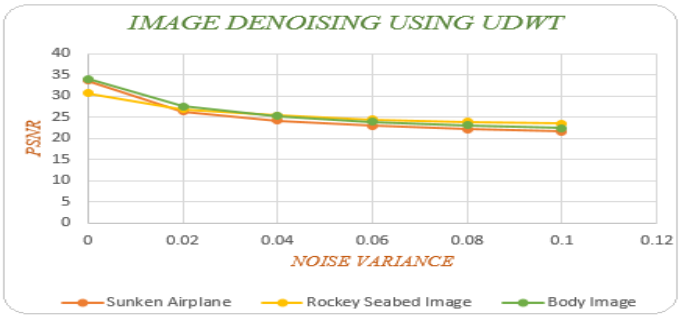

Fig. 7. Graphical representation of denoised image using UDWT.

4.2 Compression using singular value decomposition (SVD)

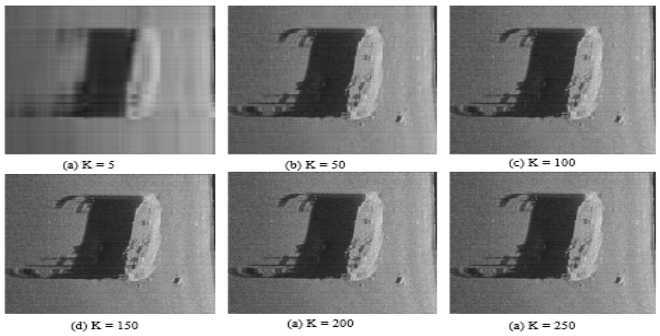

Fig. 8. SVD compression for different singular values ‘k’

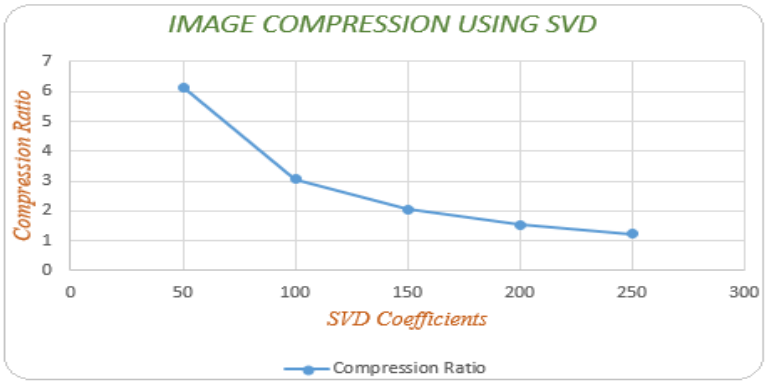

Fig. 9. Graphical representation of compression ratio using singular value decomposition

4.3 K-means clustering for Sea bottom Segmentation

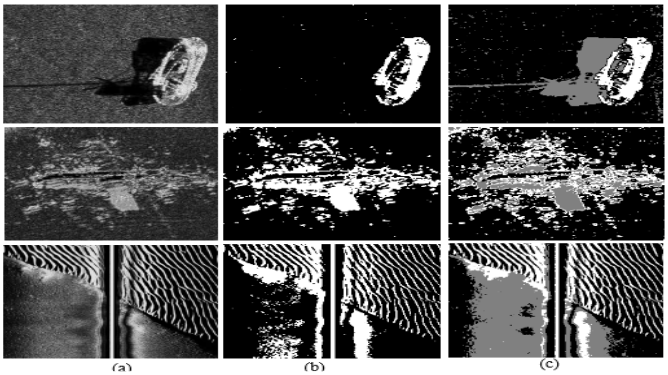

Fig. 10. Sea bottom segmentation using k-means clustering (a) input SSS images (b) partition an image into 2 clusters (c) partition an image into 3 clusters.

4.4 Two dimensional Object Detection Using ACA-CFAR

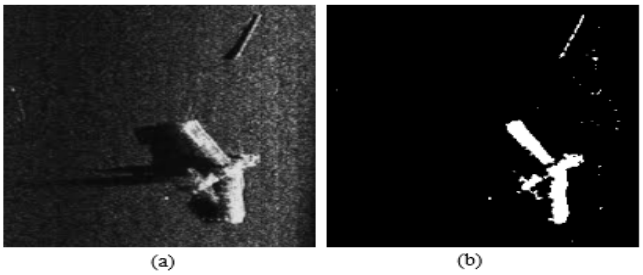

Fig.11. wreckage of a Seabee RC3 aircraft lost 1958 in lac Simon, Quebec Canada (a) input sidescan sonar image (b) segmented image using ACA-CFAR - 2D

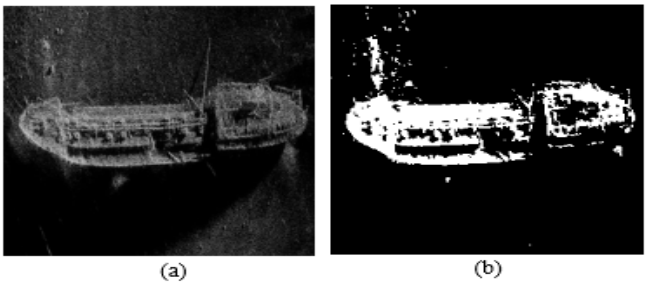

Fig. 12. Synthetic aperture SSS image of shipwreck (a) input SSS image (b) ACA-CFAR - 2D segmented image.

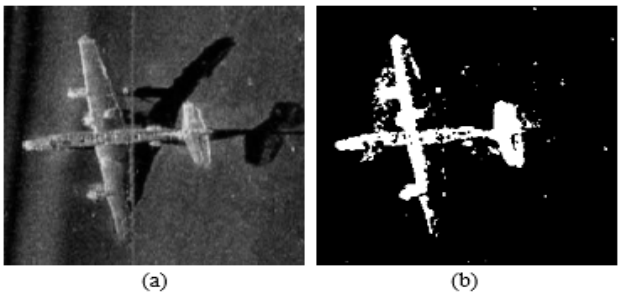

Fig. 13. SSS image (600 kHz with a range of 50m) of a sunken airplane (a) input sidescan sonar image (b) ACA-CFAR - 2D segmented image.

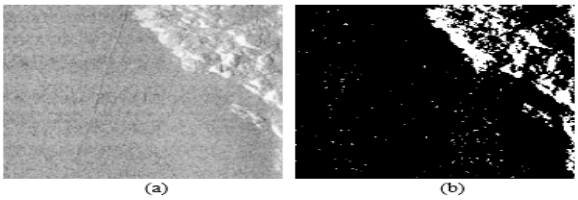

Fig. 14. SSS images of rocks of the seafloor: (a) input SSS image (b) ACA-CFAR - 2D segmented image.

4.4.1. Quantitative metrics of segmentation

In [2] the two quantitative figures of merit used for the comparison purpose are: (i) the proportion (P)of segmentedimages; and (ii) runtime (T) in seconds. The value 'P' is the measure of the percent of segmentation performance used for differentiating the segmentation maps of the ground-truth (SMgt) and the other techniques map (SMi), and is generally computed using

$$P = 1 - \frac{\sum_{m=1}^{h}\sum_{n=1}^{w}\phi(SMgt(m,n), SMi(m,n))}{h.w} \tag{8}$$

Where $\phi(x, y) = 1$ when x = y, and $\phi(x, y) = 0$ when x ≠ y. When SMgt and SMi arethe same,then Pis 1, and P approaches 0, when the dissimilaritybetweenthem increases.

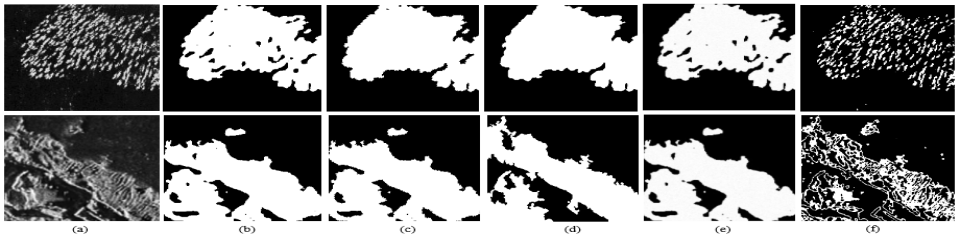

Fig. 15. Sea bottom segmentation using different algorithms: (a) input SSS images, (b) ground truth segmentation maps and segmentation results using (c) active contours, (d) watershed (e) UDWT (f) the proposed algorithm (ACA-CFAR - 2D).

4.4.2. Quantitative Assessment and comparisons

In general, segmentation is an application dependent method, such that in this work the sea bottom objects are detected using the ACA-CFAR - 2D algorithm based on pattern recognition. The Figure 15 depicts the segmented image results for different algorithms such as active contours, watershed, UDWT and the ACA-CFAR - 2D which is the proposed algorithm and are compared with their respective ground-truth maps.The algorithm suggested in this workhas significantly improved thecomputation time for all the sea bottom images which have similar segmentation results. This method can be further proved to be useful segmentation technique, if the parameters such as false alarm probability, the reference and guard cell numbers are set according to requirement and without resorting to any complex models, thus, making this approach more robust. The quantitative metrics like proportion and runtime used in this work are tabulated in the Table 1, where the ground-truth segmentation maps are generally compared with segmentation results obtained from the algorithms are purely subjective measures. For this reason, even when the results for ACA–CFAR - 2D represented by the performance metrics in Table 1 seem worse than the UDWT results. The applications such as the determination of free-span or rock-dump grounds generally prefer the proposed ACA–CFAR - 2D algorithm for segmentation than the UDWT technique.

Input image from fig. 15 (a)	Active contours		Watershed		UDWT		ACA-CFAR 2-D	
Row #	P	T	P	T	P	T	P	T
1	85.91	1.13	79.03	1.45	93.61	1.95	82.68	1.00
2	84.34	1.327	78.48	1.65	90.13	1.89	86.23	1.07

Table. 1. Performance metric results for different approaches.

5. CONCLUSION

In this paper, a 2-D object detection method utilizing ACA-CFAR for sidescan sonar images is implemented. This is an efficient approach for performing segmentation of the seabottom image into two regions: acoustical highlight and seafloor reverberation areas.The implemented ACA–CFAR - 2D algorithm represents a variation of a method broadly utilized as a part of radar innovationfor moving object detection in real time, where its efficiency is measured by an algorithmic complexity and through quantitative metrics measure. The work also presents a comparison of the segmentation results obtained from active contours, watershed and UDWT techniques with the proposed ACA–CFAR - 2D algorithm.

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GAIT BASED PERSON RECOGNITION USING PARTIAL LEAST SQUARES SELECTION SCHEME

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ABSTRACT

The variations of viewing angle and intra-class of human beings have great impact on gait recognition systems. This work represents an Arbitrary View Transformation Model (AVTM) for recognizing the gait. Gait energy image (GEI) based gait authentication is effective approach to address the above problem, the method establishes an AVTM based on principle component analysis (PCA). Feature selection (FS) is performed using Partial least squares (PLS) method. The comparison of the AVTM PLS method with the existing methods shows significant advantages in terms of observing angle variation, carrying and attire changes. Experiments evaluated over CASIA gait database, shows that the proposed method improves the accuracy of recognition compared to the other existing methods.

KEYWORDS

Gait Analysis, GEI, PCA, PLS, Feature Selection, AVTM.

1. INTRODUCTION

Human gait is the most important biometric trait for person authentication. The biometric system mainly used to prevent the unauthorized access. Biometric resources such as face recognition, voice recognition, iris, fingerprints, palm prints, shoe prints and hand writing, are a subject of extensive research work, studied and employed in many applications. The advantage of gait as the biometric is that the gait of a human can be captured even from a great distance [1].

There is a need for automation in applications such as security systems, crime investigation department and surveillance. Today, biometric is an effective tool for reliable person authentication. The motion vision's main purpose is to use surveillance when unexpected occurrences befall us.

The classification of gait recognition is done in various ways. Human motion and vision is one of a kind, recognition based on a wearable sensor, through sensor information from floor of the motion are the other types. Wearable sensor systems require carrying the sensors and floor sensors system around that necessitates setting the sensors on the floor [2, 3]. First kind is further divided, based on appearance and model parameters and appearance method is divided into two categories: they are spatio-temporal and state-space methods. Most researchers used appearance-based method compared to model-based method [4].

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The gait recognition system is capable of identifying humans from a distance beyond human interactions. This characteristic of gait recognition system is suitable for applications in large and controlled environments such as banks, military installations and even airports that are enabled to quickly detect threats.

2. PROBLEM STATEMENT AND CONCEPTS

2.1. OBJECTIVE

The primary objective of this paper is to evaluate the performance of different gait recognition methods selected for person identification.

2.2. OPTIMUM GAIT ANALYSIS

This section uses a PLS type of feature selection to find optimum gait analysis. In general human gait occurs in a periodic manner. Detection period helps in preserving the temporal information which reduces computational complexity and cost. Using the methods illustrated in [7, 9] estimate the bounding box changes and the aspect ratio, which depends on the periodic changes in human walk. These methods use GEI as the important gait parameter. PLS method is applied to extract components of gait feature descriptor.

By the periodic estimation of the GEI features gives the gait information in temporal and spatial domain. Silhouettes are obtained through background subtraction and the GEI is obtained. $B_{l,t}(p,q)$ is a binary silhouette in which the pixels are located at position (p, q).Each binary silhouette has $l\ (l = 1,2, \dots \dots \dots L)$ gait cycles. Each gait cycle has t (t=1, 2 …T) frames. Silhouette normalization is performed along both vertical and horizontal directions for a fixed range. GEI of height M and width N represents is given by

$$f(p,q) = {}^{1}/_{T} \sum_{l=1}^{L} \sum_{t=1}^{T} B_{l,t}\,(p,q) \quad \dots (1)$$

Here T represents total frames in one gait cycle. B represents the silhouette at t, p and q are the coordinates of the image.

The 1-D feature vector is obtained by concatenating the value of each position in $B_{l,t}(p,q)$ along all consecutive rows and columns which is represented by f_k^m, where k represents the k^{th} observing angle and m represents the m^{th} subject. PLS regression is used as the FS scheme to learn about optimal feature representation and also used to reduce the dimension. The major advantage is reduction in dimension of target will not limit the class number considered in database of training set. Furthermore, on applying PLS and factorization process [7], it is found that optimized GEI is better than original GEI.

Consider the case of two different persons m and n with the same k^{th} observing angle .Then f_k^m and f_k^n are the two sets of gait feature vectors are obtained. The objective function of maximum covariance between two variables is obtained by using PLS, which gives the optimal projection. The objective function is given by

$$\max_{w_k}[COV(f_k^m w_k, f_k^n)] \quad \dots (2)$$

For k^{th} observing angle w_k is the learned matrix of projection. The covariance of original GEI features with different observing angles is calculated using covariance operation. Therefore, from

a given GEI feature vector f_k^m we get the optimal feature vector A_k^m for corresponding the k^{th} angle [11].

$$A_k^m = f_k^m w_k \quad \ldots (3)$$

2.3. AVTM PLS TECHNIQUE

The following representation is regarding procedural steps for the AVTM PLS method for Gait authentication. Figure1. represents the block diagram of AVTM PLS method.

Step1 consider the gait sequence from the CASIA database.

Step2 Extract the frames from the Gait video sequence.

Step3 Perform the Background subtraction to extract the silhouette images [10].

Step4 Feature extraction is performed on silhouette images and gait features are found.

Step5 Estimate the gait period, by using this GEI is computed which is averaging of silhouettes over one gait period.

Step6 Dimensionality Reduction Techniques are used to reduce the higher dimensional feature to a lower dimensional feature .Which results in reduction in time, space and cost.

Step7 The reduced lower dimensional feature vectors are extracted by using singular value decomposition and then apply view transformation model with PLS.

Step8 The Extracted feature vectors are used for matching purpose. L1 norm distance is computed to find similarity of considered simplified gait.

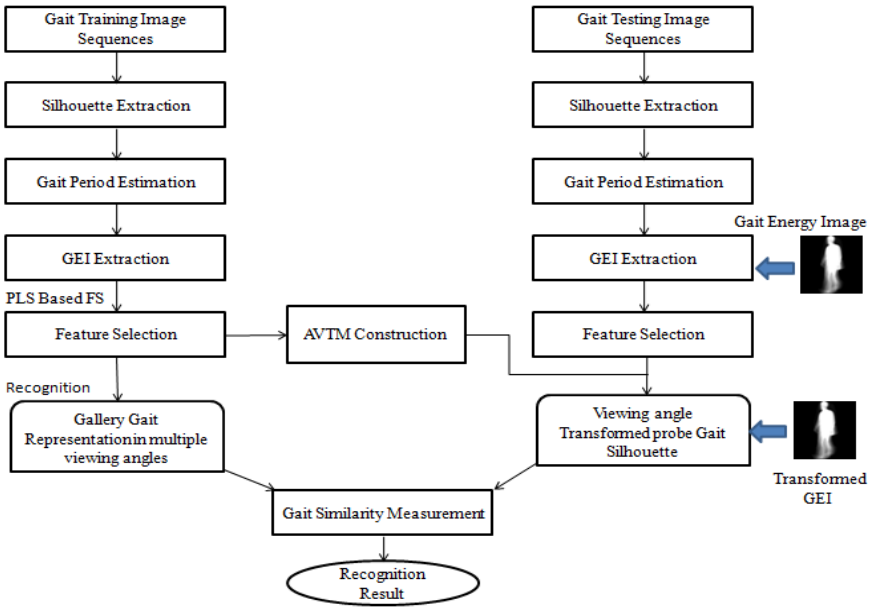

Figure1. Block diagram of Gait Recognition.

3. MODELLING OF THE PROBLEM

This section deals with modelling of Gait Recognition Method. It shows the analysis of the proposed method.

3.1. ARBITRARY VIEW TRANSFROMATION MODEL

The left hand side matrix of equation (4) is called optimized gait representation matrix represented as A_K^M . Every row indicates the gait data under same observing angle from different subjects whereas column represents same subject with different observing angles. Consider a total of M subjects and K observing angles and constructs a View Transformation Model. Singular Value Decomposition is used for factorization [7] as defined below:

$$A_K^M = \begin{bmatrix} a_1^1 & . & . & . & a_1^M \\ . & . & . & . & . \\ . & . & . & . & . \\ . & . & . & . & . \\ a_k^1 & . & . & . & a_K^M \end{bmatrix} = R[z^1 \ldots\ldots\ldots\ldots z^M] = XYZ^T \quad \ldots (4)$$

Here X and Z are orthogonal matrices with dimensions of $KN_f \times M$, $M \times M$ respectively. a_k^m has the dimension $N_f \times 1$. S is a diagonal matrix with dimension $M \times M$ has the singular values. $R = [R_1, \ldots\ldots\ldots\ldots\ldots, R_K]^T$=XY, here R_K is sub-matrix of XY and z^m is column vector.

The vector z^m represents the gait feature vector of m^{th} subject for any observing angle. Under a specific observing angle R_k represents transforming matrix which is independent of subject. It helps in projecting shared gait feature vector z to gait feature vector under specific angle k. From equation (4), for an optimized gait vector a_j^m from the m^{th} subject with j^{th} observing angle, the learned gait transformation of feature vectors from j^{th} to i^{th} observing angle is obtained as

$$t_{a_i^m} = R_i R_j^+ a_j^m \quad \ldots (5)$$

Here, R_j^+ represents pseudo inverse matrix.

4. RESULTS

4.1. OBJECTIVE MEASURES AND SIMULATION PLATFORM

The AVTM PLS method is compared with various View Transformation Models for same circumstance. Gait Energy Image features are extracted. Different methods have the variations among the VTM and FS algorithm. Consider the probe feature vector for various observing angles, the methods of AVTM and FS scheme are applied to obtain the shared subspace. Matching is performed using L1-norm distance.

Performance analysis is made by comparing recognition rate of different VTMs and its associate FS algorithm. Recognition rate gives the correctness in matching procedure.

4.2. GAIT SIMILARITY IN GAIT RECOGNITION

A PLS based VTM along with factorization process is presented. The gait similarity measurement is simplified using L1- norm distance and is given by equation (8)

$$d(a_k^i, a_k^j) = \left\| a_k^i - a_k^j \right\| \quad \text{... (8)}$$

Here d represents the distance of separation between gait signatures of the two different persons under the same observing angle. The gait feature dimension is represented by N. If the distance of separation is more then the similarity between the gait signatures a_k^i and a_k^j .

4.3. EXPERIMENTS

Simulations are performed on CASIA gait database [3]. The dataset contains the data is obtained for all 11 degree observation angles from 124 subjects. From each observation angle six sequences are considered with normal walk [12]. Furthermore, this dataset comprises of two sequences indicating respective overcoat attire and bag carrying situation for all 11 observing angles.

4.4. IDENTIFICATION RATE

For a range of varying observing angle from 0° to 180° recognition rates of popular gait recognition methods are compared for various probe angles. From the figures 1, 2 and 3 represents the simulation results of the person with overcoat, with a bag and normal walk respectively.

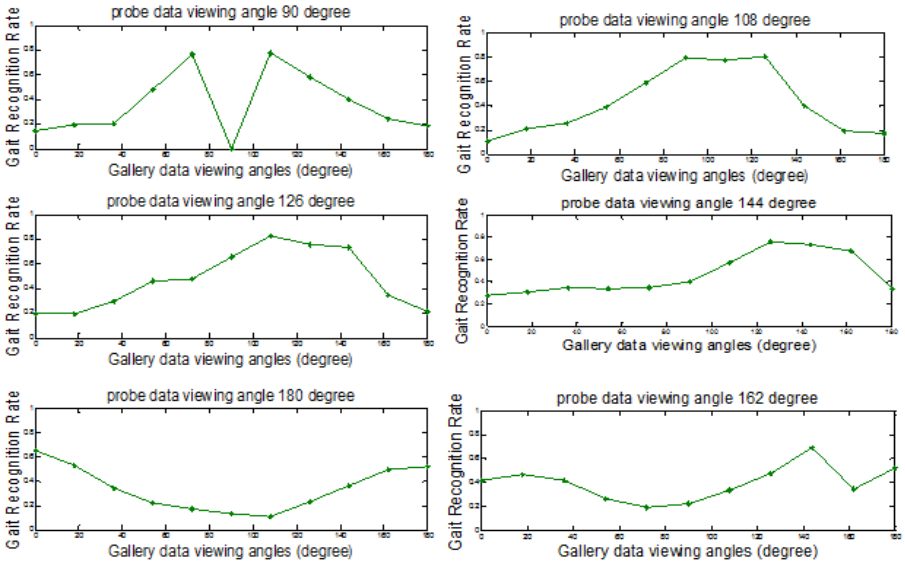

Figure2. Simulation results of the person with overcoat.

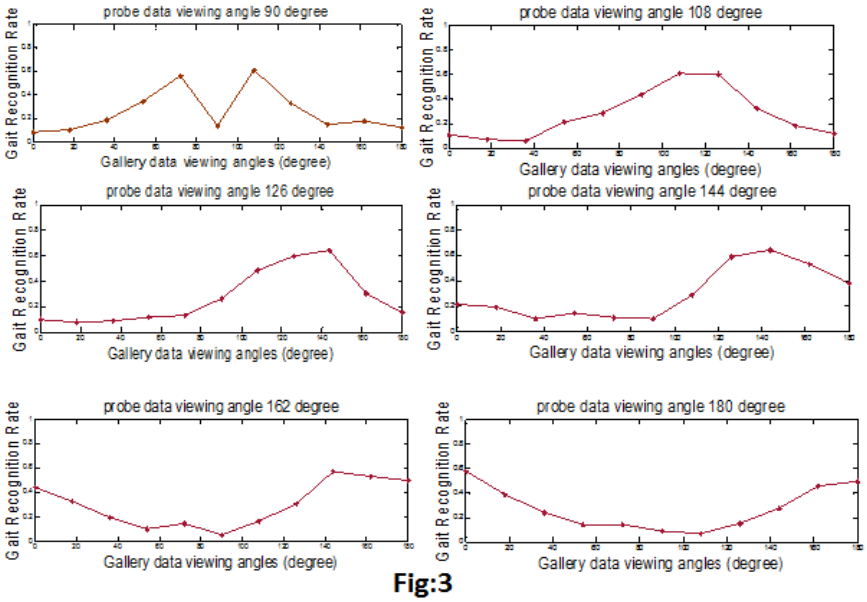

Figure 3. Simulation results of the person walk with a bag.

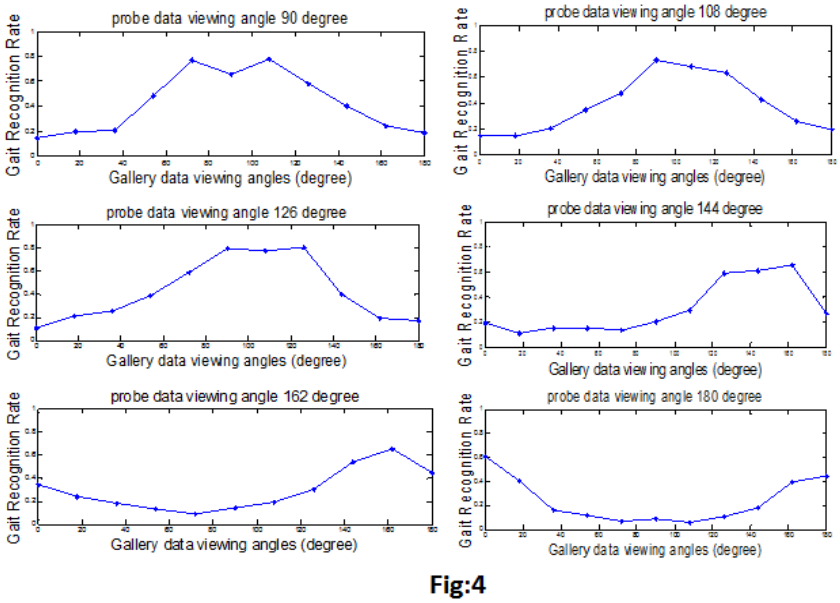

Figure 4. Simulation results of the person with normal walk.

From the Table number 1, 2, 3 and 4, the proposed technique is dominant in performance over [6], [7], [8] methods. Table1 represents the recognition rate of various algorithms for a given condition of a gallery data with observation angles varying from 72° to 162° where the probe gait data observation angle is given as 126° (With overcoat).Table2 represents the recognition rate of various algorithms for a given condition of a gallery data with observation angles varying from 54° to 144° where the probe gait data observation angle is given as 90° (With a bag). Table3 represents the recognition rate of various algorithms for a given condition of a gallery data with

observation angles varying from 54° to 144° where the probe gait data observation angle is given as 90°. Table4 represents the recognition rate of various algorithms for a given condition of a gallery data with observation angles varying from 54° to 144° where the probe gait data observation angle is given as 144°.

Table 1. Various gait recognition algorithms and its accuracy of Recognition.

Gallery observing angle	72°	90°	108°	144°	162°
GEI+LDA+TSVD[7]	0.09	0.10	0.20	0.30	0.13
Yu's method[8]	0.14	0.09	0.06	0.18	0.02
AVTM_PLS	**0.48**	**0.65**	**0.85**	**0.78**	**0.28**

Table 2. Various gait recognition algorithms and its accuracy of Recognition.

Gallery observing angle	54°	72°	108°	126°	144°
GEI+LDA+TSVD[7]	0.10	0.31	0.23	0.13	0.10
Yu's method[8]	0.13	0.31	0.44	0.15	0.02
AVTM_PLS	**0.35**	**0.60**	**0.65**	**0.42**	**0.18**

Table 3. Various gait recognition algorithms and its accuracy of Recognition.

Gallery observing angle	54°	72°	108°	126°	144°
FG+SVD[6]	0.29	0.40	0.45	0.30	0.20
GEI+LDA+TSVD[7]	0.50	0.70	0.72	0.40	0.20
Rectified method[5]	**0.72**	0.70	0.68	0.66	-
Yu's method[8]	0.16	0.81	0.77	0.22	0.03
AVTM_PLS	0.43	**0.82**	**0.85**	**0.68**	**0.42**

Table 4. Various gait recognition algorithms and its accuracy of Recognition.

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Gallery observing angle	54°	72°	90°	108°	144°
FG+SVD[6]	0.20	0.29	0.48	0.60	0.40
GEI+LDA+TSVD[7]	0.30	0.43	0.72	0.72	0.40
Rectified method[5]	**0.71**	0.59	0.60	0.70	-
Yu's method[8]	0.21	0.60	0.81	0.48	0.03
AVTM_PLS	0.42	**0.64**	**0.83**	**0.80**	**0.45**

5. CONCLUSIONS

All the VTMs using factorization are compared with proposed method. The accuracy of AVTM can be proved by considering the (GEI+TSVD) approach. The variation among Gait features with frequency- domain representation (FG) is used rather than GEI in [6]. PLS based AVTM feature selection algorithm is implemented for several view gait identification under various object positional angles like position of the bag and new objects like wearing of coat. For different observing angles the shared gait features are assumed with low significant performance on these multiple view gait databases with variations in carrying or wearing conditions.

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COMPARATIVE PERFORMANCE ANALYSIS OF LOW POWER FULL ADDER DESIGN IN DIFFERENT LOGICS IN 22nm SCALING TECHNOLOGY

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ABSTRACT

This paper gives the comparison of performance of full adder design in terms of area, power and delay in different logic styles. Full adder design achieves low power using the Transmission Gate logic compared to all other topologies such as Basic CMOS, Pass Transistor and GDI techniques but it make use of more number of transistors compared to GDI. GDI occupies less area compared to all other logic design styles. This paper presents the simulated outcome using Tanner tools and also H-Spice tool which shows power and speed comparison of different full adder designs. All simulations have been performed in 90nm, 45nm and 22nm scaling parameters using Predictive Technology Models in H-Spice tool.

KEYWORDS

CMOS, SGMOSFET, DGMOSFET, Transmission Gate, GDI, Predictive Technology.

1. INTRODUCTION

To reduce the size of chip, the complexity in the circuits has increased drastically, because of that the power dissipation and performance of the circuit are being affected. So, there is concern towards circuits design in low power VLSI design to reduce the chip area and power dissipation [1]. There are two types of power dissipations in MOSFET, namely static power dissipation and dynamic power dissipation. In Static power dissipation, there are few parameters which show effect on operation of device, among them mainly sub-threshold leakage, gate direct tunneling leakage, reverse-biased junction leakage and gate induced drain leakage shows the major effect in various scaling parameters. In Dynamic power dissipation switching and short circuit power will have the effect. The static and dynamic power dissipations are calculated theoretically from the equations shown in 1 and 2 respectively.

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$$P_S = I_{CC} * V_{DD} \quad \text{..... (1)}$$

$$P_D = \frac{1}{2} C_L (\Delta V_0)^2 f \quad \text{..... (2)}$$

Where, I_{cc} = Sum of leakage current

V_{DD}= Supply voltage

C_L= Load capacitance

ΔV_0 = Logic voltage swing

f= Frequency of switching

Power delay product (PDP=P_{AVG}*T) is a parameter we used for comparison between various circuits to estimate the optimised results which can be operated at different frequency regions. A full adder is the base in digital circuits employed for performing arithmetical and logical operations, compressors, comparators and parity checkers. In present world of VLSI system applications such as specific DSP architecture, Systolic array design, microprocessors, FIR Filters, perform fundamental operations. Full adder is a core element that determines the overall performance of arithmetic circuit. In this paper, we designed improved full adder which operates in 22nm scaling technology using transmission gate (TG) logic.

This paper summarizes as follows, Section 2 Power Consumption in VLSI Circuits, Section 3 describes the topologies of the implemented low power full adders. Section 4 represents the proposed circuit designs. The simulation results are shown and discussed from the observations in waveforms and power delay product values of different circuits presented in section 5 the conclusions in section 6 followed references in Section 7.

2. POWER CONSUMPTION IN VLSI CIRCUITS

2.1 Need for Low Power design:

Especially for portable devices the Battery lifetime plays very important role. Any customer while purchasing any portable device will definitely enquire about its battery life and reacts accordingly. A portable device must also be reliable for user friendly behavior.

The following are the Low Power Strategies that a designer must follow while designing any device.

Initially, the OS level which shows about the partitioning and power down. Next in Software level the Regularity, Locality and Concurrency (i.e., Compiler technology for low power, instruction scheduling) will be done. Next, the Architecture level part where Pipelining, Redundancy and Data Encoding (ISA, architectural design, memory hierarchy, HW extensions,

etc) are done, after that Circuit/logic level where the Logic styles, Transistor sizing and Energy recovery (Logic families, conditional clocking, adiabatic circuits, asynchronous design) will be done and finally in Technology level the Threshold reductions are done.

2.3 Main components of power consumption in digital VLSI circuits.

The main components of power consumption in digital VLSI circuits are Switching component; Short-circuit component, and Static power component. The Switching component is the power which is consumed while charging and discharging of the circuit capacitances during transistor switching. Short-circuit component occurs because of short-circuit current flowing from supply voltage to ground during transistor switching. And Static power component exists because of static and leakage currents in stable state of circuit cause this component of power consumption.

The average power dissipation for a CMOS circuit is the sum of dynamic power, static power and short circuit power as given in the Equation 3 and final form is given in Equation 4.

The average power dissipation for a CMOS circuit is given by:

$$P_{avg} = P_{dynamic} + P_{static} + P_{shortcircuit} \quad \text{..... (3)}$$

$$P_{avg} = V_{dd} * f_{clk} \sum (V_{iswing} * C_{iload} * \alpha i) + V_{dd} \sum I_{isc} + V_{dd} \quad \text{..... (4)}$$

The challenge that has been faced by VLSI designers is to find effective techniques and their efficient applications to get minimum power dissipation without any compromise on their performance evaluation parameters. Thus, the design of low power circuits with improved performance is a major concern of modern VLSI designs. The combination of certain logic styles and low power modules with low leakage circuit topologies may greatly reduce the limitations of deep-sub-micro-meter technologies. At the system level, in synchronous implementation of microprocessors, adder cells are the basic modules in a variety of arithmetic units such as arithmetic logical units, ripple carry adders , multipliers etc.

These days, as number of applications is increasing, the speed and portability are the major requirements of any smart device. The device size must be small, and it must have low-power high throughput circuitry. Sub circuits of any VLSI chip needs high speed of operation along with low-power consumption. Pass transistor circuits reduces the number of MOS transistors that are to be used in circuit, but it has drawback that the output voltage levels will no longer be same as the input voltage level. Each transistor in series has a lower voltage at its output than at its input.

From the Figure (1), the power consumption of the lead Intel microprocessors has been increasing significantly for almost every generation over the past 30 years. The frequency changes during this era from several MHz to 3 GHz. Figure (1) shows, at higher frequencies, the power dissipation is more.

Low power is required not only for portable applications but also for the reduction of power of high performance systems. Due to the requirement of large integration density and speed of

operation, systems with high clock frequencies are playing prominent role. These systems are using high speed processors and associated circuits which increase the power consumption. The cost associated with cooling, packaging and fans required by these systems to remove the heat generated because of power consumption is increasing significantly.

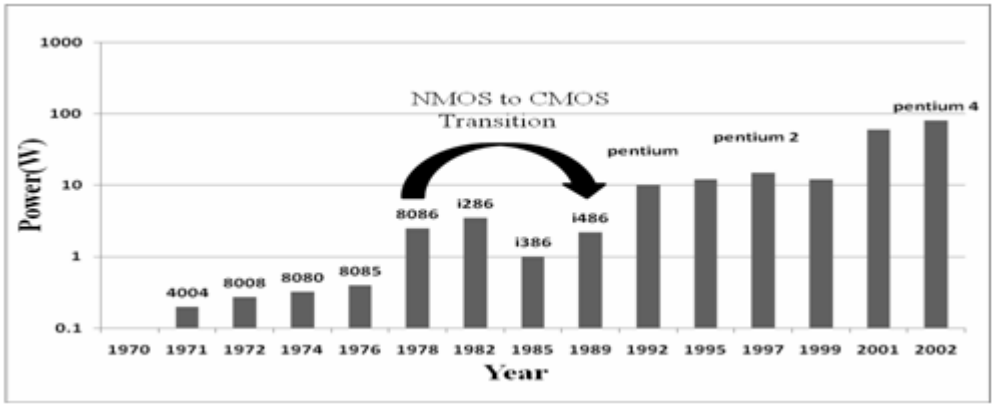

Figure 1. Maximum power consumption of Intel Microprocessor

3. PREVIOUS WORK ON ADDERS

3.1. CMOS Full Adder

Starting with basic CMOS full adder circuit, it consists of 28 transistors as shown in figure 2,[3] with less delay and high speed it also has good voltage swing, so the circuit's performance will be good but its power dissipation is more because the transistor's count is high so the area occupancy of the circuit is more. This CMOS logic is the basic logic operation of any circuit. It has PMOS in the pull up mode and NMOS in the pull down mode, so reducing the transistors count in the logic circuit is very difficult.

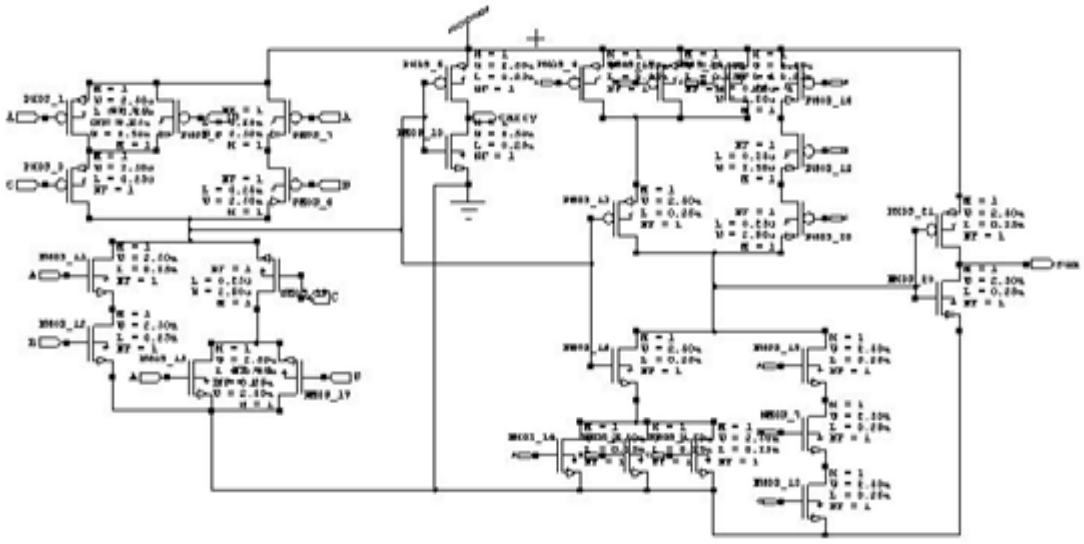

Figure 2. Basic CMOS full adder circuit using 28 transistors

3.2. Single gate MOSFET Full Adder

In order to reduce the transistors count in full adder, a circuit is designed by using single gate MOSFET consists of 10 transistors as shown in figure (3). Here in this logic VDD supply voltage is not required as the outputs sum and carry will be produced from the three applied inputs [4]. The main drawback in it is that its voltage swing is poor. It requires high input voltages to obtain the outputs, because of which the power dissipation of the circuit will be more and also XNOR/XOR sub-circuit doesn't provide stable output for applied zero inputs, because of which the logic of the circuit may differ for low transitions.

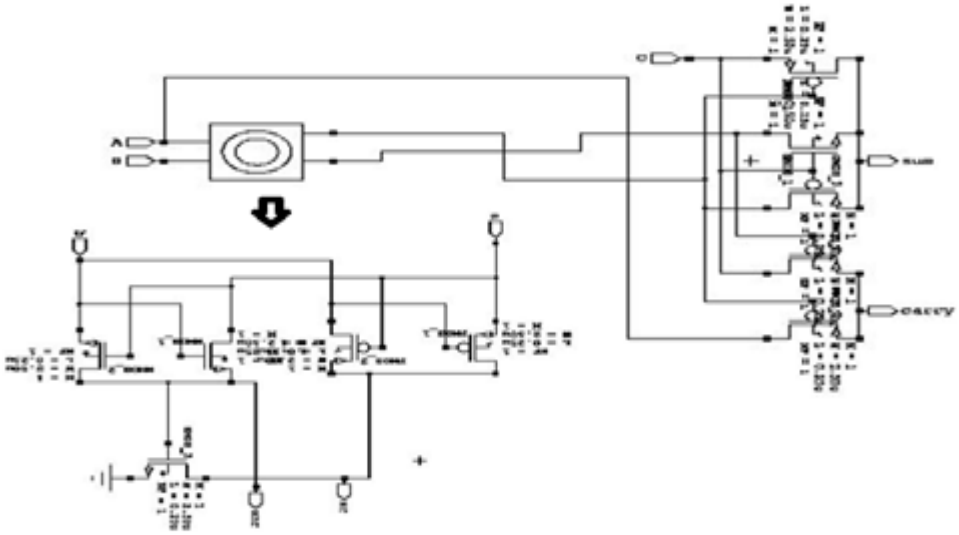

Figure 3. Single gate MOSFET full adder circuit

3.3. Double gate MOSFET Full Adder

To overcome the drawbacks in Single gate MOSFET i.e., to increase the output voltage swing in Single gate MOSFET a double gate MOSFET is designed by connecting two single gate transistors back to back in such a way that sources and drains of two single gate MOSFET transistors are connected respectively as shown in figure (4).This circuit has 4 pairs of NMOS and 6 pairs of PMOS. The logic and analysis is similar to Single gate MOSFET except voltage swing. But the draw back in this case is that it consumes more power when compared to single gate MOSFET. Generally size of PMOS is doubled than size of NMOS but in Double gate MOSFET W/L ratio is maintained as 1:1 for all transistors, because of which there is leakage in PMOS transistors [4]. The W/L ratio is maintained so as to attain sufficient output voltage swing.

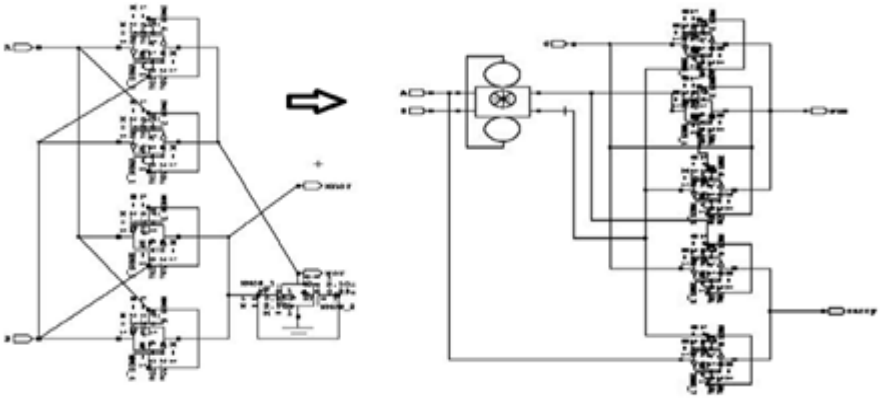

Figure 4. Double gate MOSFET full adder circuit

4. PROPOSED FULL ADDER CIRCUITS USING 22nm TECHNOLOGY

4.1. Transmission Gate full adder

A transmission gate has three inputs, called *source*, *n-gate*, and *p-gate*; and it has one output, called *drain*. The values at *n-gate* and *p-gate* are expected to be opposite to each other. If *p-gate* is 0 while *n-gate* is 1, then the value found at *source* is transmitted to *drain*. If *p-gate* is 1 while *p-gate* is 0, then the connection is broken, so the value at *drain* is left floating. In all other cases, *drain* receives an error output — unless *source* is floating, in which case *drain* is floating as well. as shown in figure (5). In this logic, one PMOS transistor and one NMOS transistor is connected back to back. This circuit has 4 pairs of Transmission Gates as shown in figure (5)[5]. The Transmission gates are used to increase the output voltage level of MOSFET's which drives their output as input to a particular MOSFET for increase in output voltage swing. It overcomes the drawbacks in pass transistor logic and above mentioned logics in section II. As transistor count is reduced without effect in performance, this circuit is preferred. It can be operated at different loads and at different frequency of operations

Table 1: Transmission gate full adder logic

p-gate	*n-gate*	*drain*
0	0	X*
0	1	*source*
1	0	Z
1	1	X*
X/Z	*any*	X*
Any	X/Z	X*

* *If source is Z, drain is Z; otherwise drain is X.*

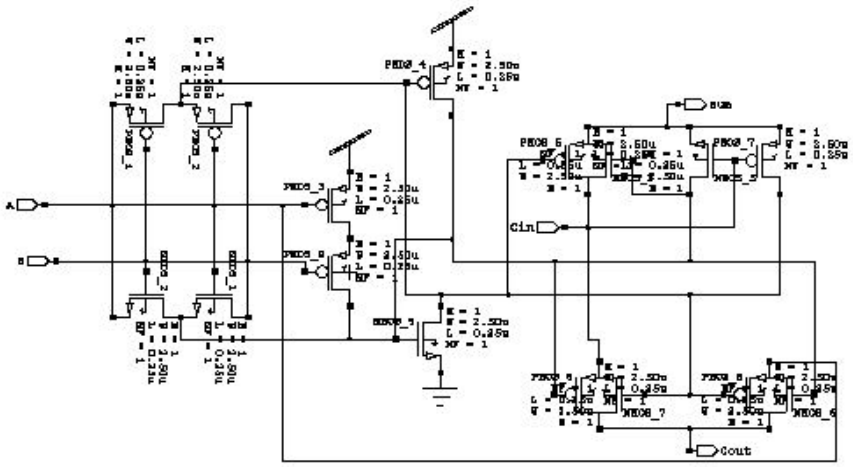

Figure 5. Transmission Gate full adder circuit

4.2. GDI

The architecture of the 2:1 MUX using GDI method is shown in fig 6.[6] In this we have connected NMOS and PMOS gate along with a SEL line ‘A’, as in MUX. As we know that PMOS works on LOW and NMOS works on HIGH. So, when the SEL input is low, then the PMOS get activated, and show the input ‘B’ in the output and due to low input the NMOS idle, as it is activated in high input. For the same case, while the G input is high then the NMOS get activated, and show the input ‘C’ at the output. Thus this circuitry behaves as a 2-input MUX using ‘A’ as SEL line, and shows the favourable output as 2:1MUX. Now it's implemented the low power full adder circuit with the help of 2T MUX, done by GDI technique. It require total 6 numbers of 2T MUX having same characteristics to design a 12T full adder [7].

4.2.1. Gate Diffusion Input Technique:

GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit. This scheme gives for fast and low power circuit designs, which is reduce

the number of MOS transistors as compared to CMOS design and also other existing low power techniques, while the logic level swing and static power dissipation improves.

GDI technique based full adders have advantages over the full adder using pass transistor and is categorized by tremendous speed and low power. This technique has been described below:

1. The GDI cell consists of one nMOS and one pMOS. The structure looks CMOS inverter. Though in case of GDI both the sources and corresponding substrate terminals are not connected with supply and it can be randomly biased.

2. It has three input terminals: G (nMOS and pMOS gate input shorted), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS drain terminal shorted).

The digital circuit can be analyzed logically with the help of simple Boolean algebra. The output of each MUX can be analyzed to get sum & carry.

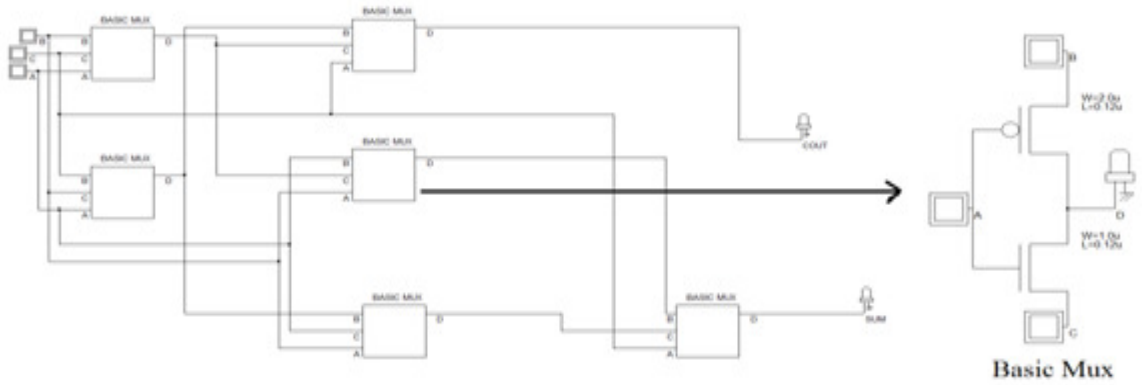

Figure 6. GDI Full Adder

4.2.2. Logic Analysis:

The digital circuit shown in figure (6), can be analyzed logically with the help of simple Boolean algebra [8]. The outputs of each MUX can be analyzed to get the sum and carry.

MUX 1= (BA^1+CA)
MUX 2 = (CA^1+BA)
MUX 3= $[(CA^1+BA)C^1+(BA^1+CA)C]$
= ABC^1+A^1BC+AC
= $ABC^1+A^1BC+AC(B+B^1)$
= $ABC^1+A^1BC+ABC+AB^1C$
= $ABC^1+ABC+A^1BC+ ABC+ AB^1C+ABC$
= $AB(C+C^1)+BC(A+A^1)+AC(B+B^1)$
= AB+BC+AC=Cout
MUX 4=$A^1B+(A^1B+AC)B$
MUX 5=$(CA^1+BA)B^1+AB$

MUX 6= $[A^1B+(A^1B+AC)B]C^1+[(CA^1+BA)B^1+AB]C$
= $AB^1C^1+A^1BC^1+ABC$=SUM

5. SIMULATION RESULTS AND ANALYSIS

For the implementation of basic CMOS circuit the scaling parameters of 22nm technology is used, W/L ratio as 2:1 and Supply voltage of 0.9V is applied for better voltage swing as shown in figure (7). For single gate full adder the output logic cannot be obtained when V_{DD}=0.9V as shown in the figure (8). So that input voltage is raised up to 1.5V to obtain the output voltage which is shown in figure (9). Double gate MOSFET output logic is similar to the single gate MOSFET output logic and their output waveforms are shown in figure (10) and figure (11).

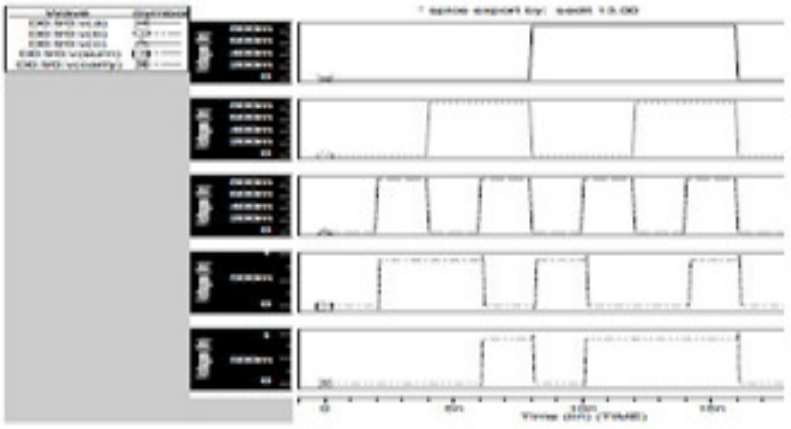

Figure 7. Basic CMOS full adder simulation results in 22nm

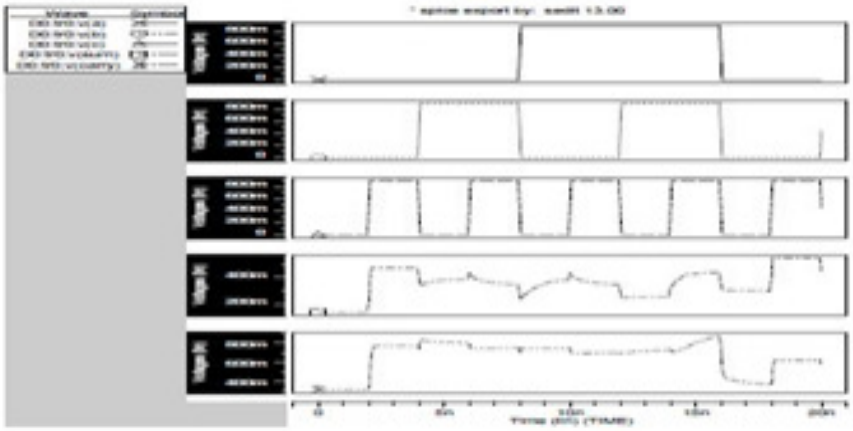

Figure 8. Single gate MOSFET simulation result in 22nm when V_{DD}=0.9V

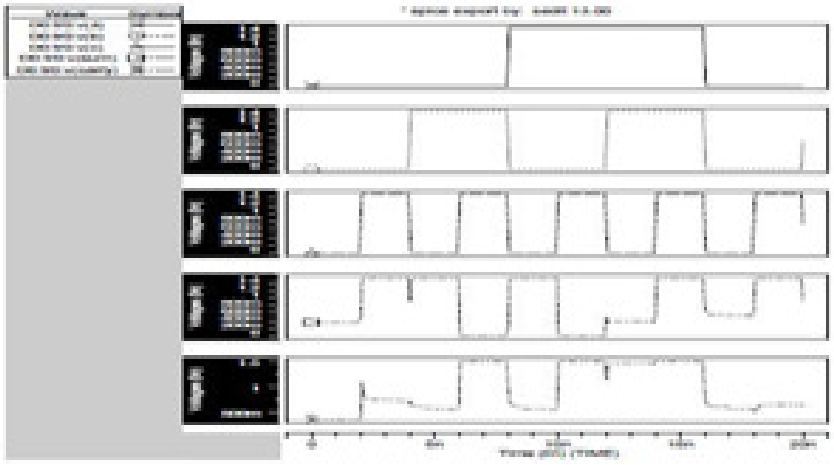

Figure 9. Single gate MOSFET simulation results in 22nm when V_{DD}=1.5V

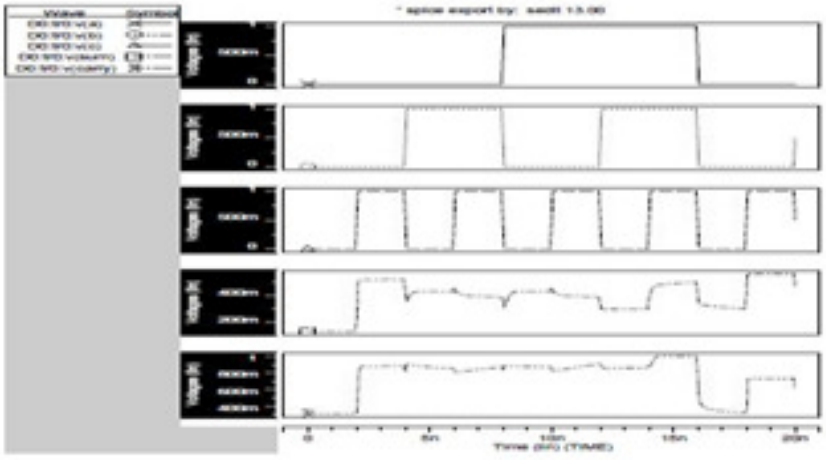

Figure 10. Double gate MOSFET simulation result in 22nm when V_{DD}=0.9V

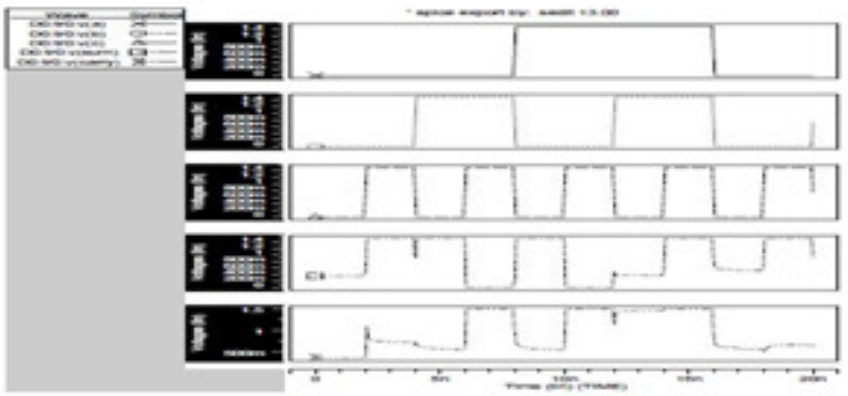

Figure 11. Double gate MOSFET simulation results in 22nm when V_{DD}=1.5V

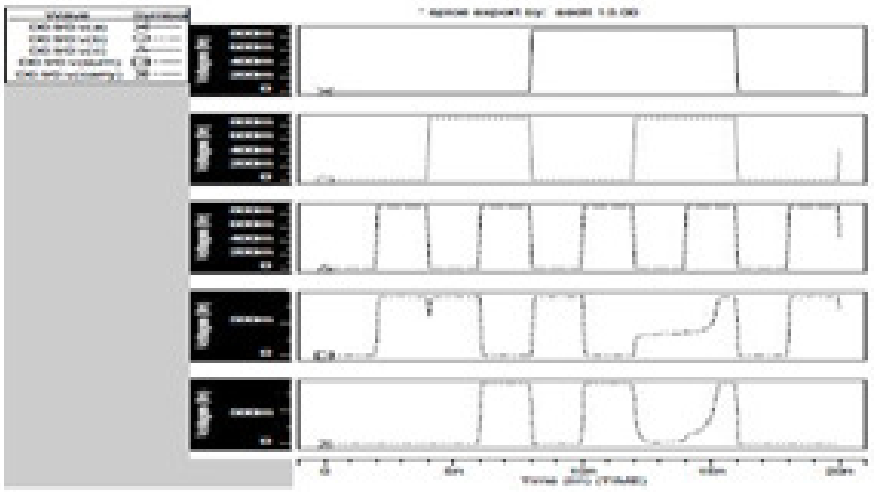

Figure 12. Transmission gate simulation result in 22nm

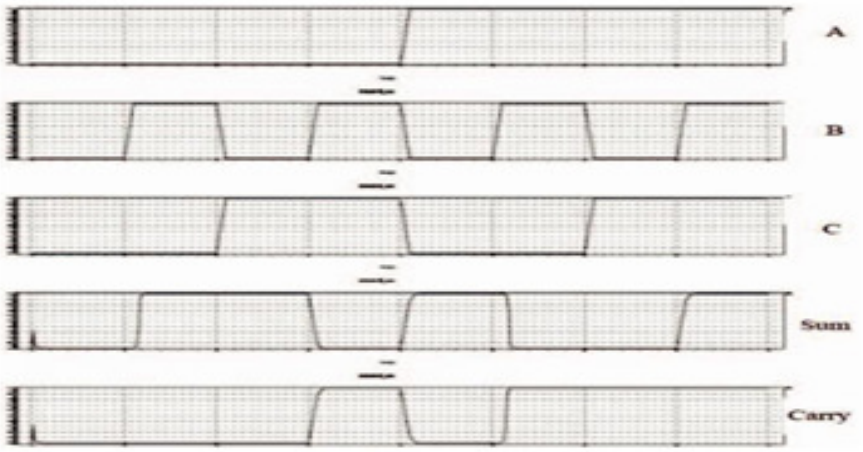

Figure 13. GDI

The average power dissipation in different nano meter scales of full adder circuits is shown in table 1. From the table, in 90nm and 22nm technology the modified full adder consumes less power. Coming to 45nm single gate MOSFET consumes less power but as mentioned in section II, “it doesn’t give strong zero at carry at transition zero”, as shown in figure (12). So, the proposed full adder has less power dissipation with good performance compared to remaining circuits. Similarly, the power delay product analysis is done in table 2, the results shows that the proposed circuit had the best optimized results. In table 3, the results are taken by operating the full adder circuits with different frequencies and the minimum required supply voltages for operating with good voltage swings are tabulated. In figure (14) and figure (15) the power dissipation and power delay product of the circuits are shown respectively. Figure (13) shows the comparison of required voltage to run the circuit with good voltage swing with respect to frequency. Figure (16) shows the area comparison with different technologies. Figure (17) show the Layouts of GDI.

Table 2: Power dissipation in different scaling parameters

S.No	FULL ADDER	90 nm	45 nm	22 nm
1	Basic CMOS	1.132	5.16	0.0362
2	Single gate MOSFET	0.1854	0.787	0.0362
3	Double gate MOSFET	1.1124	0.63	1.19
4	Transmission Gate	0.1549	0.408	0.0254
5	GDI	1.457	1.18	0.2846

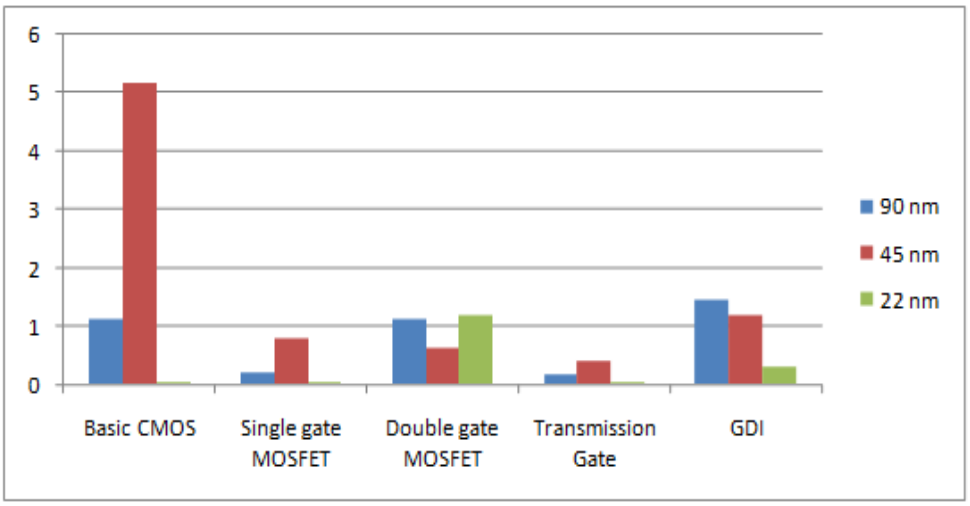

Figure 14. Comparative analysis of Power Dissipation in different circuit modes

Table 3: Power delay product in different scaling parameters

S.No	FULL ADDER	90nm	45nm	22nm
1	Basic CMOS	1.132	5.16	0.0362
2	Single gate MOSFET	0.1854	0.787	0.0362
3	Double gate MOSFET	1.1124	0.63	1.19
4	Transmission Gate	0.1549	0.408	0.02544
5	GDI	0.33	0.115	0.02393

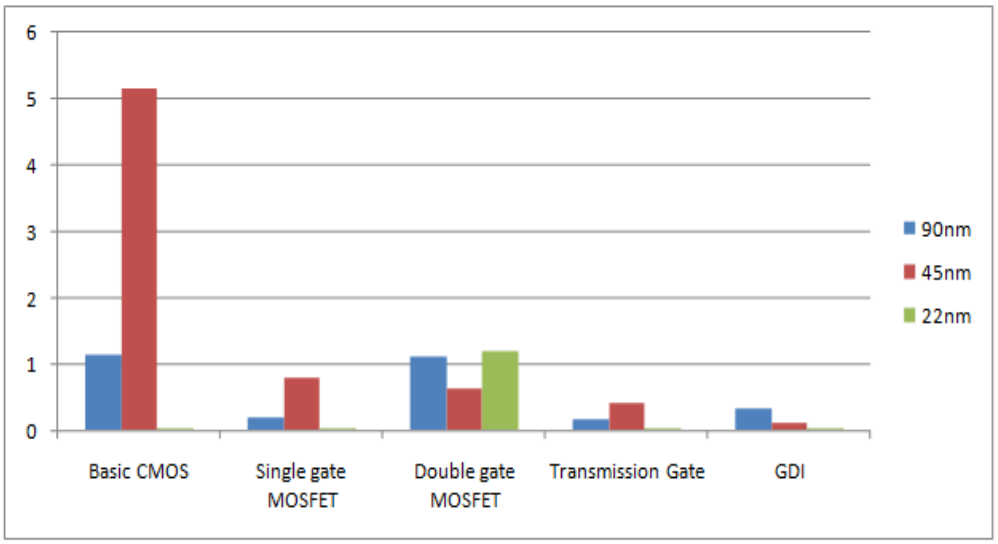

Figure 15. Power delay product analysis

Table 1. Area in 22nm scaling technology with lambda=0.1um

Model	CMOS	SGFA	DGFA	TGFA	GDIFA
22nm	1740	726	1512	1173	858
XxY	87x20	33x22	63x24	51x23	39x22

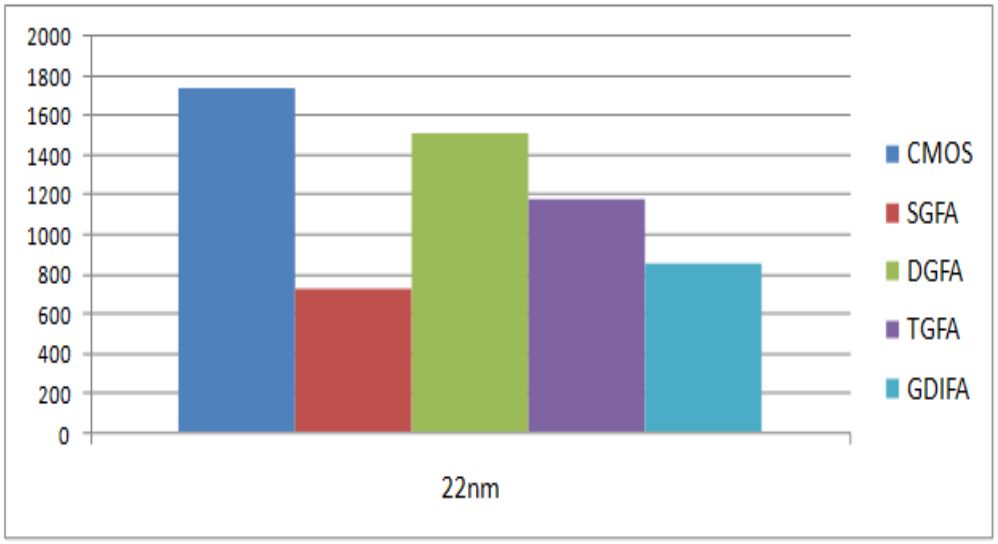

Figure 16. Area Comparison of different models in 22nm technology

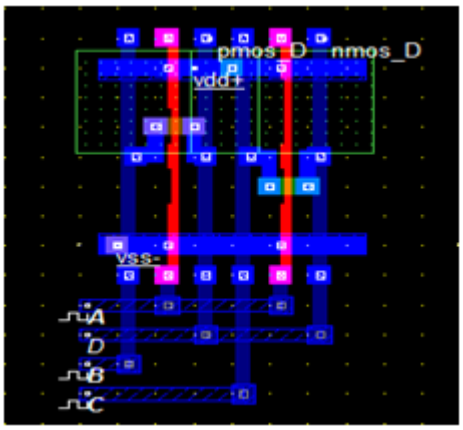

Figure 17. Full Adder Layout using GDI

6. CONCLUSION

The performance parameters such as power, area and speed are evaluated for full adder using various nano-scale technologies. The simulation results shows that as we go on scaling there is drastic decrease in power consumption of full adder. It is not only achieves the low power but also operate at high speed. Post-Layout simulations shows the full design occupies the less area in 22nm technology compared to other nano scale technologies. The full adder designs are best suitable designs for the low power high-speed applications.

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NOISE IMMUNE CONVOLUTIONAL ENCODER DESIGN AND ITS IMPLEMENTATIONIN TANNER

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ABSTRACT

With the rapid advances in integrated circuit(IC) technologies, number of functions on a chip was increasing at a very fast rate, with which interconnect density is increasing especially in functional logic chips. The on-chip noise affects are increasing and needs to be addressed. In this paper we have implemented a convolution encoder using a technique that provides higher noise immunity. The encoder circuit is simulated in Tanner 15.0 with data rate of 25Mbps and a clock frequency of 250MHz

KEY WORDS

Noise immune design, Convolutional encoder design.

1. INTRODUCTION

Due to the rapid advances in integrated circuit technologies,with the advent of VLSI,The electronics industry has achieved a phenomenal growth over the last few decades,The number of applications of been rising steadily, and at a very fast pace. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field.

The design complexity of logic chips increases almost exponentially with the number of transistors to be integrated. As the technology aggressively scales down, the density on the chip have increased and hence the interconnection density, leading to increased interaction among the connections and thereby increasing crosstalk and system failures.

On the other hand with the decrease in supply, the gate threshold is decreased to preserve system throughput and so leakage currents have increased. And therefore the noise margins have greatly reduced. The noise immunity is of more concern in high fan-in circuits as they have larger leakage due to more parallel evaluation paths. As the number of parallel paths(fan-in) increase in the design, the noise immunity of the design decreases. The circuits with wide fan-in include coding and decoding circuits in communications, address decoding and encoding, data sequencing and timing control in computational applications.

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PROBLEM STATEMENT

The basic digital communication system employs various encoding and decoding circuits as shown in Fig. 1. Forward error correction schemes are generally used in transmitter to encode the data or information and in receiver to detect and correct errors.

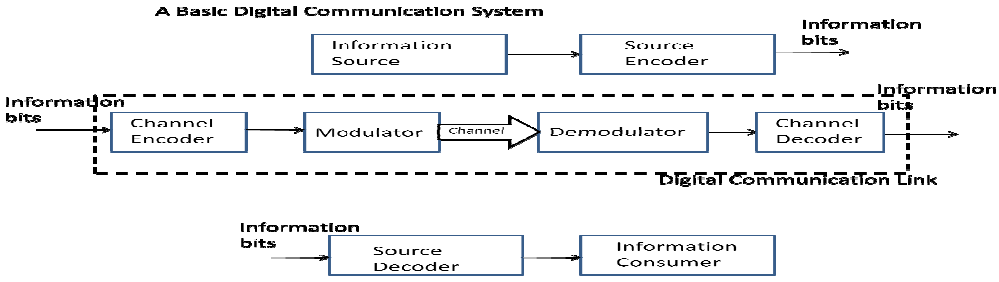


Fig.1 Basic Digital Communication System

Forward Error Correction (FEC) in digital communication system improves the error detection as well as error correction capability of the system at the cost of increased bandwidth and system complexity. Using FEC the need for retransmission of data can be avoided hence it is applied in situations where retransmissions are relatively costly or impossible. FEC codes can be classified in two categories namely block codes and convolution codes. Block codes operate on fixed size data blockswhere as convolution codes operate on arbitrary length data blocks. A convolution coder is often used in digital communication systems where the signal to noise ratio is very low. Error detection and correction or error control arethe techniques that enable reliable delivery of digital data over an unreliable (noisy) communication channel. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, where aserror correction techniques allow for the reconstruction of the original data.

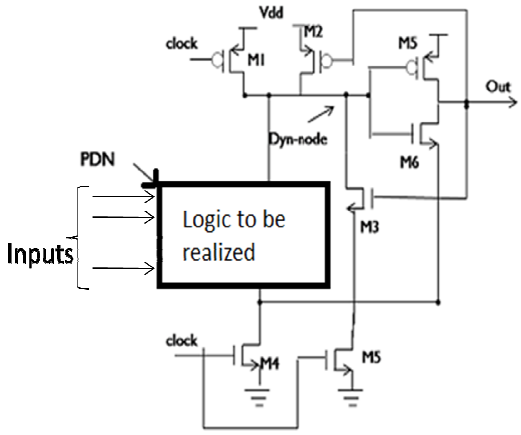
As the encoder circuits comprise of high fan-in gates, when implemented in nano-metric technologies, are prone to noise effects. In the chips which realize logic, most of the chip area is used in providing interconnections and because of their high density; interaction among them would be more. This large inter coupling among the wires introduces noise in the nearby wires which in turn may result in errors in function realization, especially when the encoder input gets corrupted, it results in unrecoverable error at the output of the encoder. Thus we have designed a convolution encoder with a technique which is more noise immune and simulated the design.
In section II we discussed the noise immune technique, Section III deals with Convolution encoder design ,in section IV, simulation results and in section V conclusion were presented.

2. NOISE IMMUNE GATE DESIGN

Dynamic logiccircuits find their wide application in high speed, low power areas such as microprocessors, digital signal processing, dynamic memories etc., because of their low device count, high speed, short circuit power free and glitch free operation [2]. On the other hand it is also possible to design a dynamic logic unit that is smaller than its static counterpart. Dynamic logic consists of pull down network realizing the logic.

From the basic theory of dynamic logic, large amount of noise gets induced and power consumption increases. Dynamic logic suffers from charge sharing and cascading. To overcome these problems domino logic was proposed. When a dynamic gate is cascaded by a static inverter, it is called Domino logic. For the same output current and a lower switching threshold, aDomino gate runs faster thanits static counterpart as they present much lower input capacitance.

The proposed domino circuit is shown in the Fig.2 [3]. Transistor M3 and M5 are connected between the dynamic- node and ground, gate ofM3 transistor is connected to the OUT terminal and M3 is stacked with M5. During evaluation phase when PDN is on with one or more inputs connected to logic one, the transistor M4 discharges the dynamic-node and the Out terminal goes to logic '1' and M3 becomes on which aids in faster discharge of any accumulated charge on dyn_node along with PDN and M4. The rate of discharge can be controlled by varying the W/L ratio of M4. When all the inputs are at logic '0', output stay at logic '0' and M3 remains off and thus dyn_node retains its charge. If any input changes from logic '0' to logic '1' , PDN becomes conducting and during evaluation phase when clock is high, dyn_node discharges below V_t of the inverter turning its output to logic '1'. When output becomes logic '1', M3 turns on providing a path to discharge dyn_node quickly as M5 is also ON during evaluation phase. At the same time as the source node of M6 being connected to N-foot, effect of noise in the circuit can also be reduced. An Ex-or gate of the proposed technique is implemented and simulated.



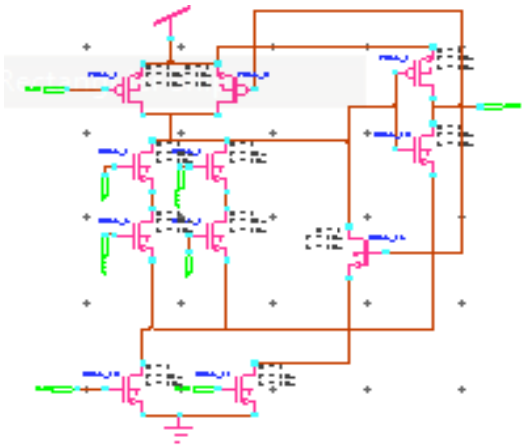


Fig.2 Proposed noise immune technique. Fig.3 Two inputs Ex-OR gate of the proposed technique.

3. CONVOLUTIONAL ENCODER DESIGN:

Convolution codes operate on arbitrary length data blocks. The convolution coder is often used in digital communication systems where the signal to noise ratio is very low. In this, the encoding operation may be viewed as discrete time convolution of input sequence with the impulse response of the encoder.

Convolutional codes are commonly specified by three parameters, (n,k,and m),Where n represents the number of output bits,krepresents number of input bits andm, the number of registers. [4] Code rate k/n is measure of efficiency of the code. Generally k and n range from 1 to 8, m from 2 to 10 and code rate from 1/8 to 7/8 except for deep space applications where code rates as low as 1/100 or even longer will be used[4]. Convolutional code chip manufacturers often specify the code by parameters (n,k,L), where L is constraint length, defined by L = k(m-1), and

represents the number of bits in the encoder memory that effect the generation of the n output bits[4].

As a bit is shifted along the register it becomes part of other output symbols sent. Thus the present output bit that is observed has information about previous input bits. A convolution encoder used shown in Fig.4. It is assumed here that the shift register shifts in one bit at a time and outputs three bits, though other combinations of input to output bits are also possible.

Input[S1]	[S2 S3]	[O1 O2 O3]
0	0 0	0 0 0
1	0 0	1 1 0
0	1 0	1 1 0
1	1 0	0 1 1
0	1 1	0 1 1
1	1 1	1 1 0
0	0 1	1 0 1
1	0 1	0 0 0

Table 1. Encoder Transition table

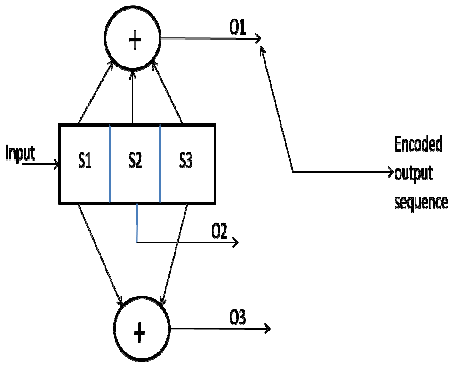


Fig.4. Convolutional Encoder

Here the present input bit is shifted intoS1,S2 and S3 holds the previous bits thus defining the state of the encoder. For every input bit there are three output bits (O1, O2,O3), thus code rate is 1/3. The transition tabledefines the output of the encoder for given state and input (Table.1).
It is the code generation polynomial which gives a unique error detection quality for a generator.For example a list of Generator polynomials found by Busgang for good rate 1 /2 codes is shown in Table.2, as can be seen from the table that fan-in of summing circuit (here EX-OR) is increasing with constraint length. Thus as the fan-in increases the effect of on chip noise at will be more and thus can cause errors in the coded output, and cannot be recovered at the receiver as the encoder output itself is erroneous. Thus to eliminate such type of error, Ex-or gate should have high noise immunity.

Constraint Length	G1	G2
3	110	111
4	1101	1110
5	11010	11101
6	110101	111011
7	110101	110101
8	110111	1110011
9	110111	111001101
10	110111001	1110011001

Table.2 Generator Polynomials found by Busgang for good rate ½ codes

The encoder circuit is thus implemented with a gate having high noise immunity as reported in [4]. Two input and three input ex-or gates were implemented and simulated with the proposed technique.

4. SIMULATION AND RESULTS

Simulations were done on Tanner T-spice 15.0 with 16nm technology PTM files with 1V supply. The encoder circuit is implemented in three design techniques namely footless domino gate with keeper (FLDG Keeper), Scheme [8] technique and Noise immune proposed technique. All the circuits were simulated with 250MHz clock and data rate of 25Mbps.

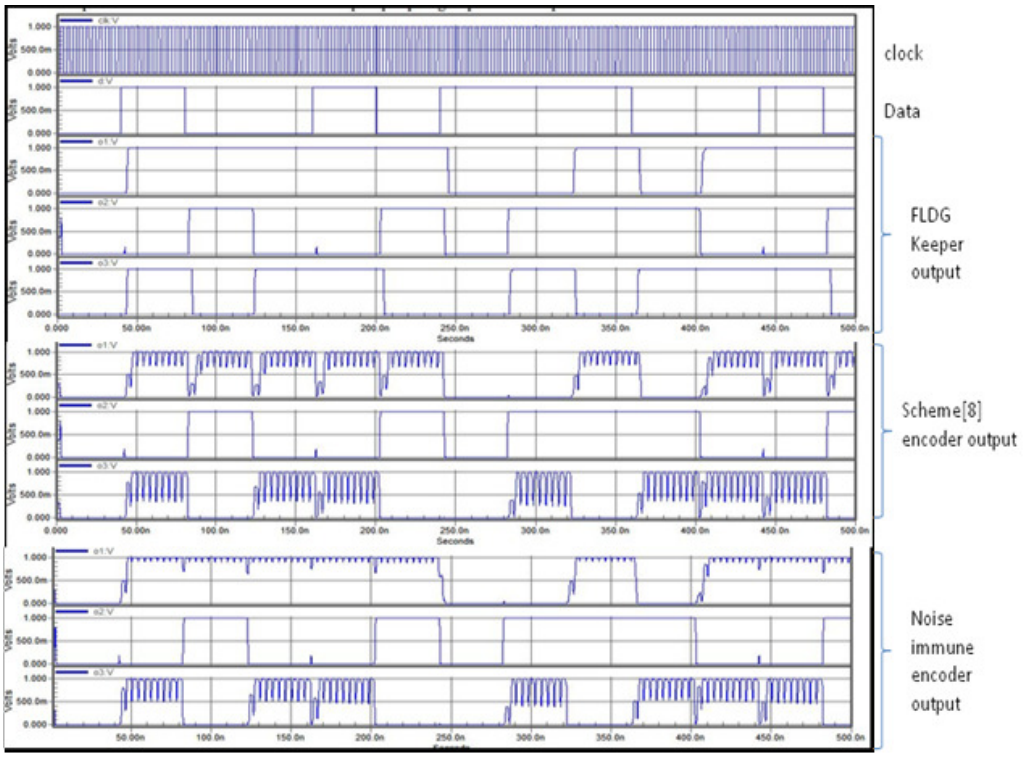


Fig.5. Simulation results of convolutional encoder using three different techniques

From the simulation result we have observed that the proposed technique has less- ripple in the output and more noise immune as EX-OR gates are implemented with noise immune design technique.

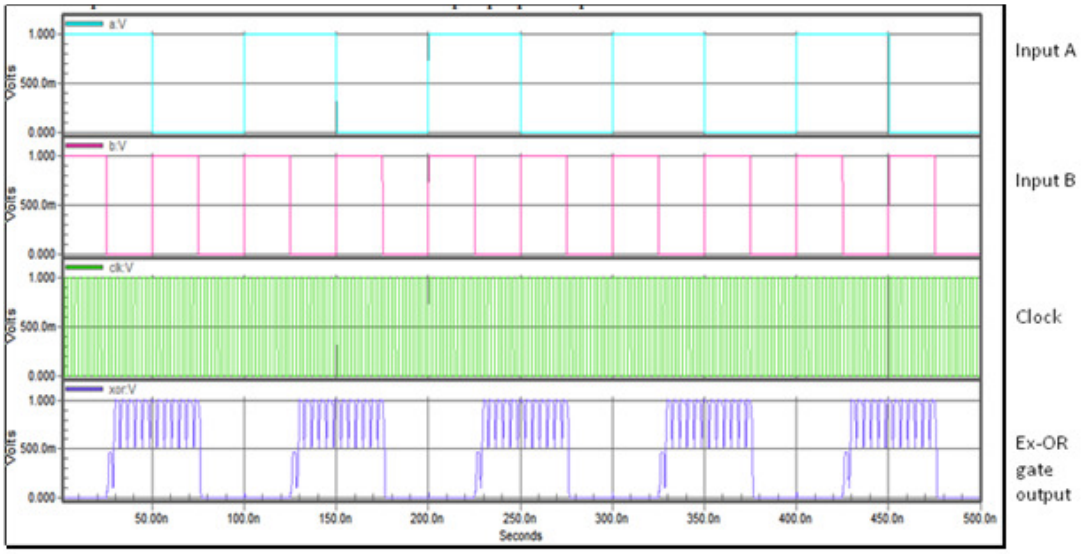


Fig.6. Simulation result of two input Ex-OR gate.

Fig. 6 shows the simulation output of two inputs Ex-OR gate with noise immune technique.

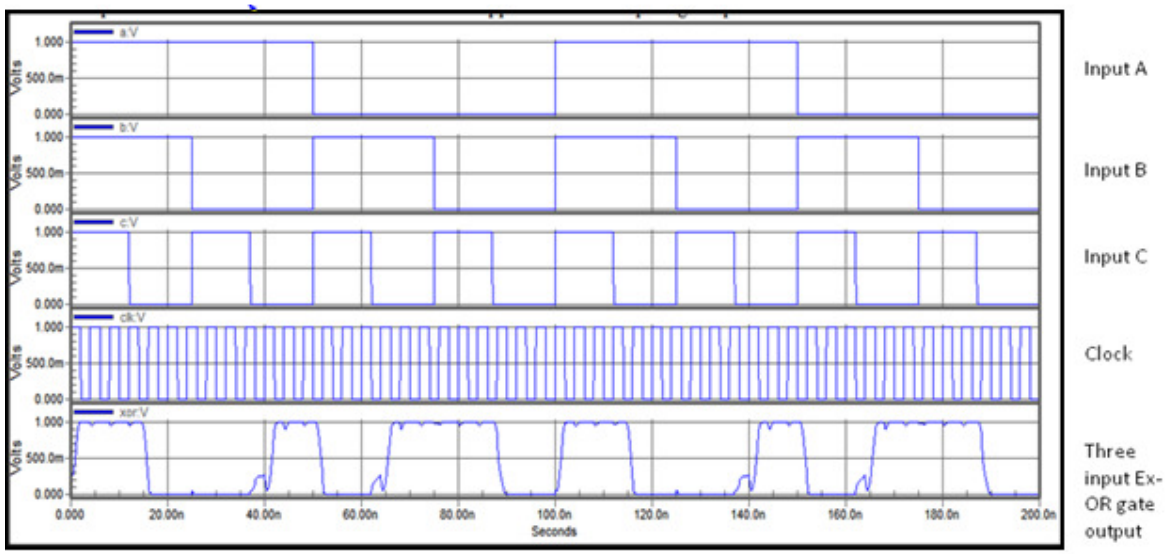


Fig.7 Simulation result of three input Ex-OR gate.

Fig. 7 shows the simulation output of a three input Ex-OR gate with noise immune technique.

CONCLUSION

In this paper we have presented theimplementation results of a rate 1/3 convolutional encoder with input data rate of 25Mbps and Clock rate of 250MHz. The circuit is implemented in three different techniques and their simulation results were presented, and found that the proposed technique has fewer ripples in the output and is more noise immune.

ACKNOWLEDGEMENTS:

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DESIGN ANDIMPLEMENTATION OF EFFICIENT TERNARY CONTENT ADDRESSABLE MEMORY

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ABSTRACT

A CAM is used for store and search data and using comparison logic circuitry implements the table lookupfunction in a single clock cycle. CAMs are main application of packet forwarding and packet classification in Network routers. A Ternary content addressable memory(TCAM) has three type of states '0','1' and 'X'(don't care) and which is like as binary CAM and has extra feature of searching and storing. The 'X' option may be used as '0' and '1'. TCAM performs high-speed search operation in a deterministic time. In this work a TCAM circuit is designed by using current race sensing scheme and butterfly matchline (ML) scheme. The speed and power measures of both the TCAM designs are analysed separately. A Novel technique is developed which is obtained by combining these two techniques which results in significant power and speed efficiencies.

KEYWORDS

Content Addressable Memory (CAM) Circuit, XOR-based conditional keeper, Ternary Content Addressable Memory (TCAM)Circuit,Pseudo-Footless Clock Data Pre-charge Dynamic Match line (PF-CDPD)Architecture.

1. INTRODUCTION

Ternary Content Addressable Memory (TCAM) is the useful for search and store ternary values and used for partial data matching. TCAMs are composition of conventionaltype semiconductor memory with addition of comparison circuitry. The most common application of TCAMs arepacket forwarding and packet classification.

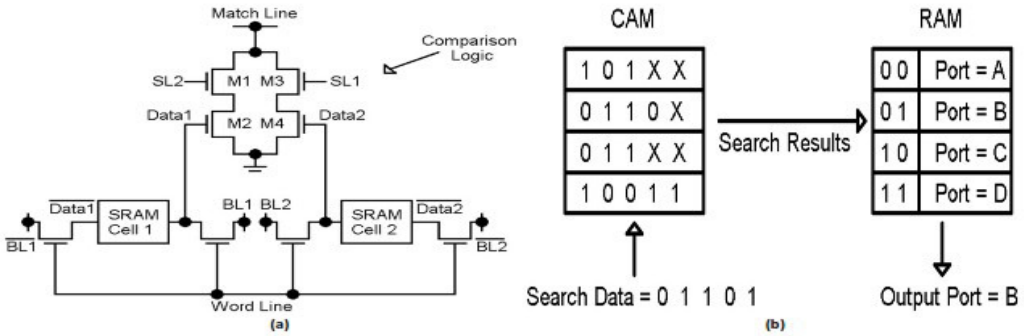

Fig 1(a) Conventional TCAM (b) Address lookup with TCAM/RAM

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A TCAM contains two parts.Static RAM cells and a comparison logic circuit. These are shown in Fig.1.Both NOR and NAND versions are used to design TCAMs. But NOR type is used to design TCAM because higher speed. The stored data (D1, D2) is referred as three type of states such as '1', '0' and don't care(X).Search data (SL1, SL2) is present and it is provided through search line pair. In case of a mismatch the ML is connected to ground through one of the paths M1,M2 or M3,M4.In the case of a match (D1D2=SL1SL2) there is no connection to ground. So, reduction ofpower consumption is reduced to design TCAM.

Fig1 (b) shows TCAM system as a complete implementation of an address lookup function. The match address output of the CAM is in fact a pointer used to retrieve associated data from RAM. In this case the associated data is the output. The TCAM search can be viewed as a dictionary lookup where the search data is word to be queried.

2. MATCH LINE TECHNIQUES

2.1.1 Current Race Scheme

The Current Race Scheme is the one of the matchline techniques. The scheme achieves the 50% of power saving. The scheme starts with the precharges the matchline (ML) low and evaluatesmatchline (ML) state is the chargewith the current I_{ML} is placed by a current source. The precharge signal of the matchline low when it starts the prechrging search cycle. thematchline is precharging low, then scheme charges the search lines/match lines to their search data values, eliminating the need for a separate SL precharge phase required by the precharge-high scheme. After the Search Line/Match Line precharge phase completes, current source to matchline is connected to enable signal. In match state the matchline (ML) is in high voltage, while in the miss state it is in low voltage. thevoltage of only I_{ML} x R_{ML}/M. The ML is connected to nMOS transistor, M_{sense}. The output of nMOS transistor M_{sense} is stored by half latch. The main reason of the ML is precharged low because of the scheme allow changing the CAM cell configuration. Hence there is no charge sharing problem when precharge low in the CAM cell configuration.

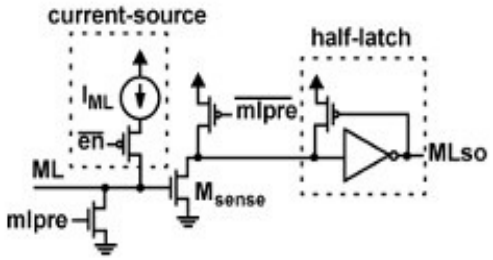

Fig 2(a) current race scheme

2.2.1 Butterfly ML TCAM

The butterfly match-line (ML) TCAM scheme is proposed using pseudo-footless clock data pre-charge dynamic (PF-CDPD) structure. It is associatedthe each pipelined stage is in the butterfly associationstructure which is utilized for diminish thepower consumption and search time. The powerutilization on the search line is reduced without any search time overhead. A noise-tolerant match-line (ML) scheme with XOR-based conditional keeper is introduced to diminish the power

consumption and search time. With the specific end of the goal to reduce the search time overhead caused by butterfly connection style the XOR-based conditional keeper system can decrease delay of critical path of the match-line. Figure 2(b) shows the butterfly connection structure. Thetwo CAM segments are associated in the butterfly connection structure. The two CAM segments are connected using two input NOR-gate, and controlled signal of next stage is generated by the two input NOR-gate output. The proposed four segment butterfly match-line scheme with XOR-based conditional keeper gives the power saving and high performance.

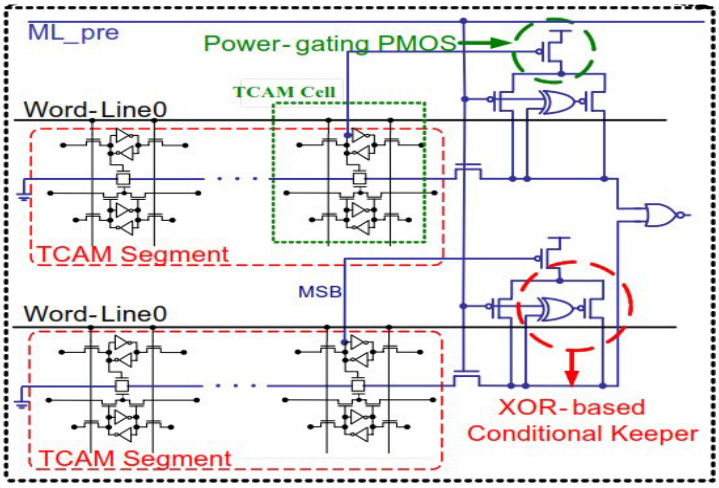

Fig 2(b) butterfly ML TCAM

2.3.1 Novel Technique

The novel technique is designed by using combining the current race scheme and butterfly match-line (ML) scheme. In the current race scheme the Match Lines are pre-discharged to ground.Match Line (ML) enable signal initiates the search operation. During the search operation MLs are charged towards high. Search Lines are need not to be precharged to ground in the technique. This reduced search line switching activity compared to the conventional scheme saves around 50% power. And Current Race scheme reduces the search time also.

In the butterfly match-line (ML) in order to reduce search time overhead caused by butterfly connection, a XOR-based conditional keeper technique is applied. The XOR-based conditional keeper is the turned off and it is used for to reduce the search time and power consumption.

Due to this butterfly connection style, this circuit has got high-degree of parallelism since it can do search operation of all TCAM cells at a time. Hence, because of this power of this circuit has been reduced considerably when compared to that of conventional TCAM cell.

2.3.2 Advantages of Novel Technique

The butterfly ML scheme could reduce about 82.2% of match-line power. And current race scheme reduce the delay of 41.2% of match-line power. So, we design a novel technique by combine these two techniques reduce the both power as well as delay of the circuit.

3. SIMULATION RESULTS

The Design and the implementation of the power reduction techniques have been carried out in Tanner tool 13.0 version software tool of 0.18µm CMOS technology. The specifications that are followed in the simulation results are shown in the table 3.1. The most power consuming task is the search operation in the TCAM access. The different techniques have been used to reduce power reduction and how far power and delay savings compare to traditional TCAM.

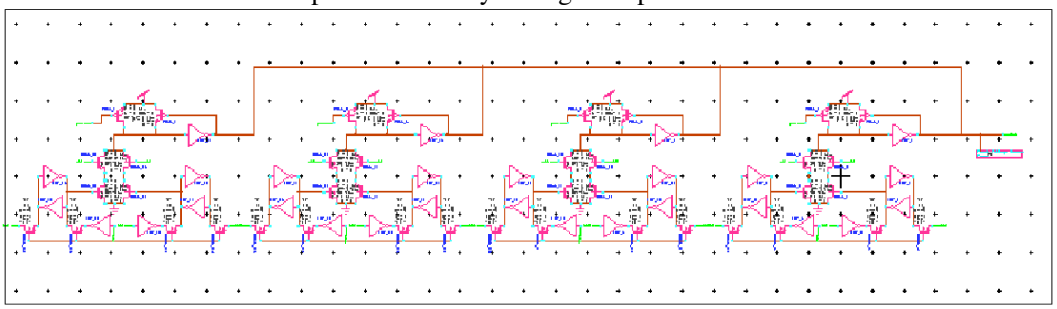

Fig 3.1(a) Circuit schematic conventional 4-bit TCAM cell with comparison and storage parts

Figure 3.1(a) shows the Schematic conventional 4-bit TCAM cell. Here four TCAM cells are connected in series. Each TCAM cell has comparison logic and storage parts.

Fig 3.1(b) Speed analysis of Conventional TCAM

Figure 3.1(b) shows the Conventional TCAM Speed analysis. The speed obtained is 2.47 Seconds.

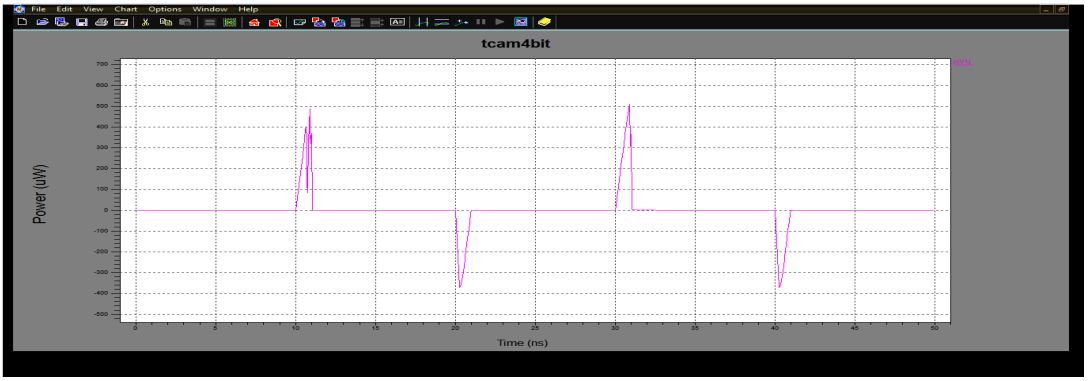

Fig 3.1(c) power analysis of Conventional TCAM

The figure 3.1(c) shows the power analysis conventional TCAM cell, which is used to compare the power reduced value to that of various implemented power reduction techniques. Here the power consumption obtained is 508µW.

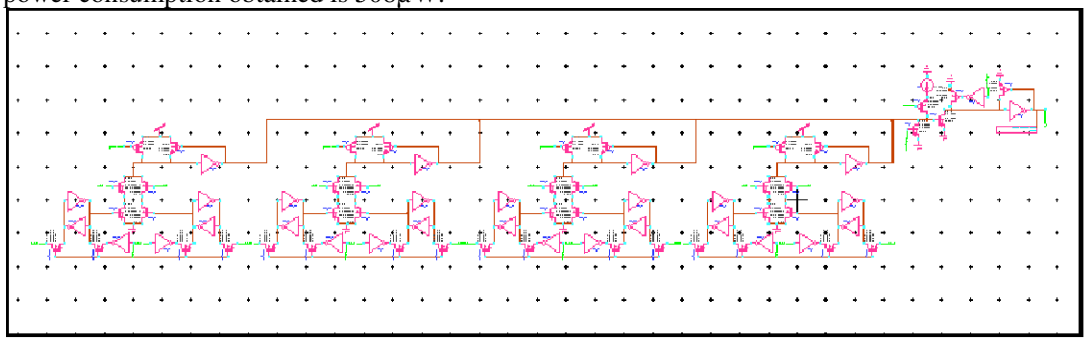

Fig 3.2(a) Circuit schematic of the proposed current race technique

Figure 3.2(a) shows the 4-bit TCAM with proposed current race scheme. The current race scheme is designed by connecting the conventional TCAM with current race scheme part. This is designed in Tanner tools software.

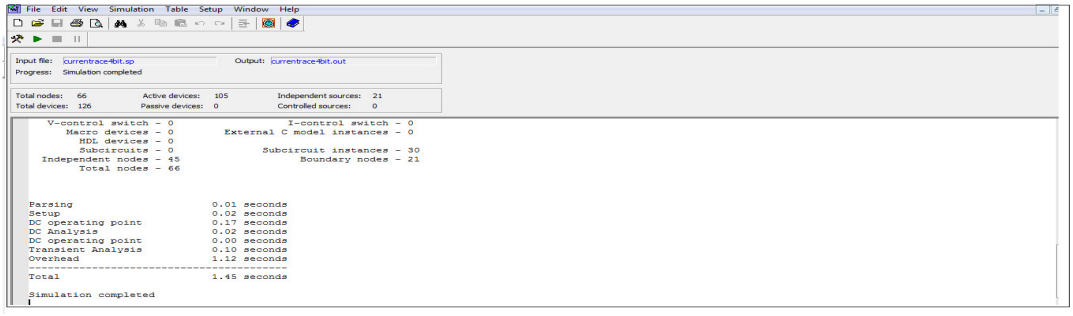

Fig 3.2(b) Speed analysis of the proposed current race technique

A figure 3.2(b) show the proposed current race scheme speed analysis and obtained the speed is 1.45 Seconds. The speed is better compared to conventional TCAM.

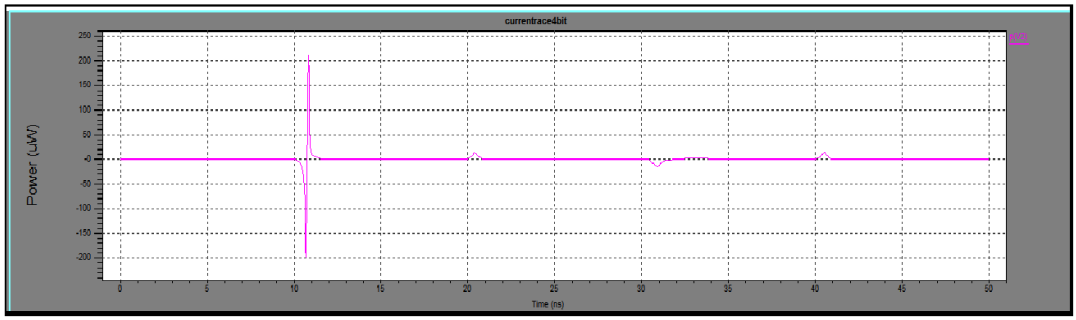

Fig 3.2(c) power analysis of the proposed current race technique

Figure 3.2(c) shows power analysis of the proposed 4-bit TCAM with the current race technique. During the ML charging phase Current race scheme passes similar currents to both matched and mismatched MLs. So, here in large number of mismatched MLs large amount of energy wasted. Hence the CR scheme is reduce the currents to the mismatched MLs. The obtained power consumption is 212µW.The current race scheme is reduce power is 58% and delay is 41% compared to Conventional TCAM.

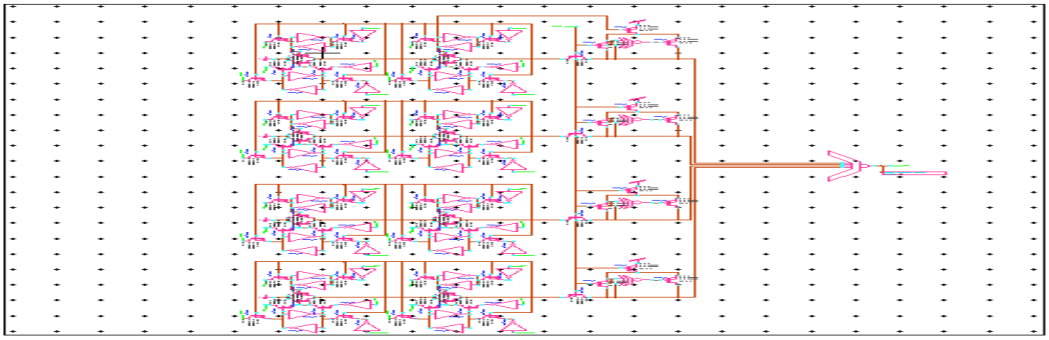

Fig 3.3(a) Circuit schematic of the 4-segment butterfly ML scheme

Figure 3.3(a) shows the 4-segment butterfly match line scheme which is connected the TCAM segments are in pipelined architecture. Four TCAM segments are connected with NOR gate.

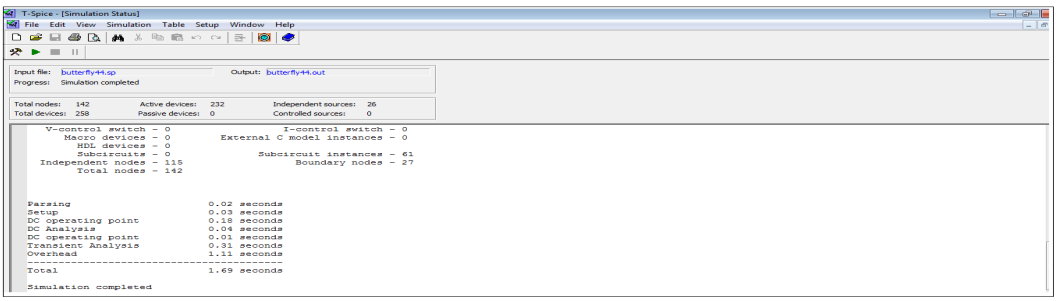

Fig 3.3(b) speed analysis of the butterfly ML scheme

Figure 3.3(b) shows the speed analysis of butterfly match line scheme and obtained speed is 1.69 Seconds.

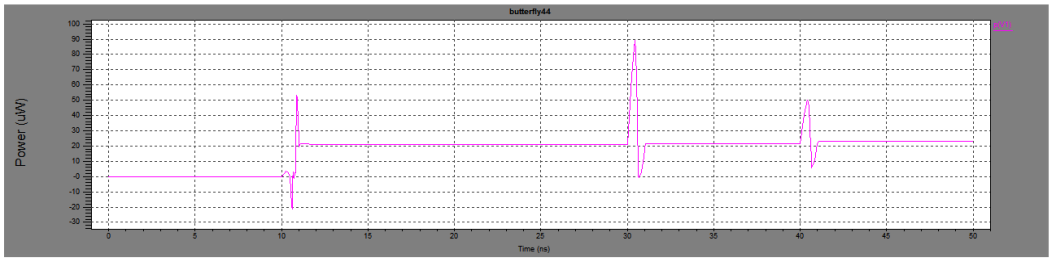

Fig 3.3(c) power analysis of butterfly ML scheme

Figure 3.3(c) shows the power analysis of 4-segment butterfly ML TCAM employing TCAM structure of Asymmetric TCAM cell model. Due to this butterfly connection style, the circuit has got high degree of parallelism since it can do search operation of all TCAM cells at a time. Hence because of this power of this circuit has been reducedwhen compared to the conventional TCAM cell. And obtained power is 90µW.and butterfly ML technique is reduce power is 82% and delay is 31% compared to conventional TCAM.

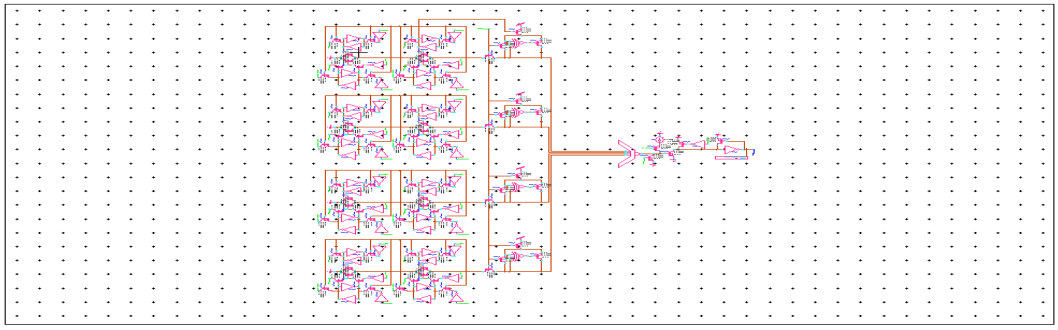

Fig 3.4(a) Schematic implementation of Proposed Novel technique

Figure 3.4(a) shows of the schematic implementation of proposed novel technique which is designed by combining the butterfly match line scheme and current race scheme.

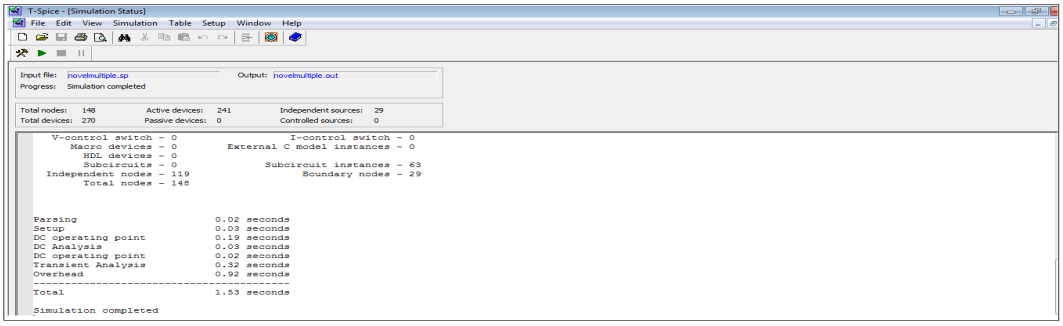

Fig 3.4 (b) speed analysis of Proposed Novel technique

Figure 3.4(b) shows the Speed analysis of proposed novel technique and obtained speed is 1.53Seconds.

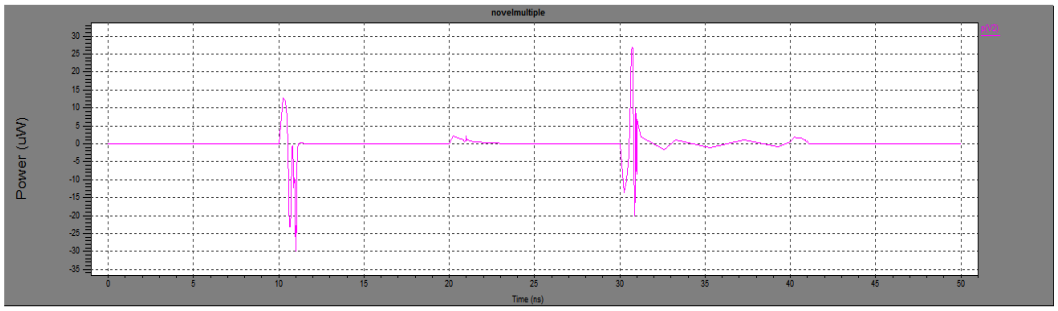

Fig 3.4(c) power analysis of Proposed Novel technique

Figure 3.4(c) shows the power analysis of the Proposed Novel technique and obtained power is 27µW. The Proposed novel technique is designed by combine the current race technique and butterfly ML technique. So combine the both techniques we obtain the power is reduced by 94% and delay is 38% compared to conventional TCAM.

Table 3.1: Tabulated Results

Proposed Configuration	**Power (µW)**	**Speed(Secs)**	**Power reduced compare to TCAM**	**Speed increased compare to TCAM**
Conventional TCAM Circuit	508	2.47		
Proposed Current Race Scheme	212	1.45	58.26%	41.29%
Butterfly Match Line Scheme	90	1.69	82.28%	31.57%
Proposed Novel Technique	27	1.53	94.68%	38.05%

CONCLUSIONS

An energy efficient Novel ternary content addressable Memory design is proposed in this paper. The reduction of high power consumption and delay which are the limiting factors of TCAM has been achieved by various power reduction techniques which are implemented in 0.18µm CMOS technology. The Novel technique is designed which is reduced power up to 94% and increased speed up to 38.05% compared to Conventional TCAM.

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WAVELET BASED ON THE FINDING OF HARD AND SOFT FAULTS IN ANALOG AND DIGITAL SIGNAL CIRCUITS

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ABSTRACT

In this paper methods for testing both software and hardware faults are implemented in analog and digital signal circuits are presented. They are based on the wavelet transform (WT). The limit which affected by faults detect ability, for the reference circuits is set by statistical processing data obtained from a set of faults free circuits .In wavelet analysis it has two algorithm one is based on a discrimination factor using Euclidean distances and the other mahalanobis distances, are introduced both methods on wavelet energy calculation. Simulation result from proposed test methods in the testing known analog and digital signal circuit benchmark are given. The results shows that effectiveness of existing methods two test metrics against three other test methods, namely a test method based on rms value of the measured signal, a test method utilizing the harmonic magnitude component of the measured signal waveform.

.KEYWORDS

Faults dectection, simulation distance measurement eudiean distance and mahanolobis distance,

1. INTRODUCTION

A software simulator is a computer program; an emulator is a hardware simulator. Simulation is used for design verification that is validating assumptions, verify logic, verify performance (timing). Types of simulation are logic or switch level simulation, timing simulation, circuit simulation; fault simulation.Fault models are analyzable approximations of defects and are essential for a test methodology [1]. For digital logic circuits, single stuck-at fault model offers best advantage of tools and experience. Many other faults (bridging, stuck-open and multiple stuck-at) are largely covered by stuck-at fault tests. Stuck-short and delay faults and technology-dependent faults require special tests. Memory and analog circuits need other specialized fault models and tests.

Ladder Filters circuits are popular for realizing analog integrated circuits and also popular for designing analog circuits in modern mixed signal IC [2]. So it can be most easily realized with Z-transform techniques and typically require anti aliasing filter, smoothing filter. Accuracies of key parameters clock frequency, as well as the capacitor ratios and remain accurate with temperature. In single stage operational amplifier doubling of the load capacitance halves the unity gain frequency and improves the phase margin. The finite slew rate may limit the upper clock speed. on-zero DC offset can result in a high output dc offset, depending on the topology chosen, especially if correlated double sampling is not used.

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.Simple faults are for the most part characterized into two indexes hard and parametric shortcomings. A hard blame that progressions the circuit netlistv, for example, a stuck at 0 and struck at 1(short or open wire)[3]. Hard blames for the most part result in an emotional change of the circuit under test (CUT) exchange capacity. In delicate deficiencies speak to parameter movements of the parts in the CUT, for example, varieties of , trans-conductance resistance Sudan changes of the coefficients in the exchange capacity of the CUT. The considerable achievement of the stuck-at shortcoming model of advanced circuits roused looks into to extend its applications to simple circuits.

Delicate faults are hard to test in labs. The fundamental issue of testing delicate flaws is shortcoming rundown of a solitary parameter comprises of interminable number of qualities The unbounded delicate issue list makes the deficiency reproduction time illogically long. To address this issue, proposed receiving the auxiliary data of the CUT to lessen the span of the shortcoming set. Another way to deal with rate

1.1 OBJECTIVE OF THE PAPER:

This paper is to verify and design the fault model that can be applied for analog circuits. In general, the fault simulation time for analog circuits is large and no exact method has been proposed yet. The fault simulation time of analog circuits is complex from the fact that multiple kinds of faults arises in analog circuits like catastrophic faults, which relates to the creation of net list, short or open wires and parametric faults which are major in number relating to change in the value of the components in the circuit.

This work includes:

(i) Design of a static linear behaviour analog fault model for ladder circuits.
(ii) Design of a test procedure, which can estimate all the parameters
(iii) In the parameter set so that the circuit under test can be tested with
(iv) Multiple parametric faults.
(iii) Finding out the component which is responsible for the error.
(iv) Calculating the percentage of the error present in the value of the component.

2. FAULT MODEL

Testing of analog and digital signal circuits has become a challenge and gained more interest in the last decade for many reasons including increasing the applications of the analog circuits, integrating the whole system on one chip, and the high cost of analog testing compared with digital testing counterpart. This measure is called ‘fault coverage ‘and is defined as:

Fault coverage= Number of detected faults/ Total number of faults

When a product is, fabricated designed and tested and it fails the test, then there must be cause for the failure. Either the test was wrong, or the fabrication process was faulty, or the design was incorrect, or the specification had a problem. Anything can go wrong. The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong, and where the process needs to be altered. Therefore, correctness and effectiveness of testing is most important for quality products. However, electronic tests are not perfect either. They may not cover certain faults and some bad chips will pass.

Many integrated circuits contain fabrication defects upon manufacture. A defect is a physical flaw in the device, i.e. a shorted transistor or an open inter connect. A fault is the logic level manifestation of the Defect, i.e. a line permanently stuck at a low logic level .An error occurs when a fault causes an incorrect logic value at a functional output. A logic gate may generate a wrong output signal because of fault in the circuitry that implements the gate. Dealing with the many different types of faults is cumbersome. Fortunately, it is possible to restrict the testing process to simple faults, and obtain generally satisfactory results. A circuit is said to be faulty if it gives output transfer function out of design specifications. Faults can occur both in analog and digital circuits and based on the fault model, efficient tests can be generated to ensure the quality of the circuits with low test cost. Generally a practical fault model helps to simplify testing problems. A fault model helps to simplify the problem by targeting only Logical Faults.

NEED FOR FAULT MODELS

i. A fault model identifies targets for testing and is essential for a testing methodology
ii Real defects often mechanical too numerous and often not analysable.
iii .A fault model identifies a fault model and targets for testing makes analysis possible.

2.1 CLASSIFICATION OF FAULTS

The diversity of VLSI defects, it is difficult to generate tests for real defects. Fault models are necessary for generating and evaluating a set of test vectors. Generally, a good fault model should satisfy two criteria:

i. It should accurately reflect the behavior of defects, and
ii It should be computationally efficient in terms of and test pattern and generation

Many fault models have been proposed but, unfortunately, no single fault model accurately reflects the behaviour of all possible defects that can occur. As a result, a combination of different fault models is often used in the evaluation and generation of testing approaches and test vectors developed for VLSI devices. When there is only one fault in the circuit, then the total number of possible single faults, referred to as the single-fault model. In reality of course, multiple faults may occur in the circuit. The total number of possible combinations of multiple faults, referred to as the multiple-fault model [3] Coming to classification of faults they are of different types and mainly they are partitioned to

I. Analog Faults II. Digital Faults

Analog faults are generally classified into two catalogs: hard and soft faults[3]. A hard fault is a fault that changes the circuit net list such as a short or an open wire. hard faults result in a dramatic change of the CUT's transfer function. On the other hand, soft faults represent parameter shifts of the component

3. WAVELET BASED ALGORITHM

A circuit test involves three major steps: signal response measurement, circuit stimulate and analysis of the results. Here, the CUT is stimulated in normal operation by an generated signal, and the *I*PS or *V*OUT signal is measured and stored. A *wavelet* algorithm is performed to stored the *I*PS or *V*OUT signal is to calculate the necessary distance values. The WTis utilized better approximation of a transient signal waveform than the Fourier transform for a fixed limiting

frequency of the measured signal[4]. Moreover, it allows the selection (in terms of minimization of the approximation error) of the appropriate basis function according to the measured signal encountered in the CUT.

For the wavelet based algorithm, the *discrete wavelet* is used. The Wavelet energy divide a discrete signal of length *n* into two sub signals [4]. One sub signal is a trend or average; the other sub signal is a fluctuation or difference. Two energy values are computed, *EF*1and *ETi*. For the computation of *ETi* (*i* = 1, 2 . . .), the trend coefficients *Tij* (*j* = 1 . . . *n*) of the *i* decomposition

$$E_{Ti} = \sum_{j=i}^{k} E_{ij}^{2} \tag{1}$$

And for *EF*1, the fluctuation or detail coefficients *F*1*j* of the first level of decomposition are taken into account

$$E_{f1} = \sum_{j=i}^{k} E_{f1}^{2} \tag{2}$$

3.1 TEST ALGORITHM UTILIZING A DISCRIMINATION FACTOR OF EUCLIDEAN DISTANCE METRIC FUNCTION

In this algorithm, the discrimination factor *Df* test metric is introduced which is actually a normalized Euclidean test metric that depends on the energy values *ET*2and *EF*1 of the WT of the measured waveform (*I*PS, *V*OUT).For the wavelet energy computation, the trend coefficients of the second-level decomposition and detail coefficients of the first-level decomposition are considered[5]. The proposed test algorithm A is a two-phase process. At the first phase (*Training Phase*), statistical processing of the fault free circuit data takes place in order to compute the wavelet energy values *ET*2,0(*z*) and *EF*1,0(*z*) for the reference circuit and the discrimination factor limit *Df*lim In the second phase(*Main Test Phase*), algorithm phases are described in the following.

Training Phase (steps)

Step 1:each fault-free circuit *i* = 1, . . . , *n*
Step 2:Measuring the waveform *z* = {*I*PS, *V*OUT}.
Step 3:Compute the values and store *ET*2,0−*i*(*z*), *EF*1,0−*i*(*z*).

$$E_{T2,0(Z)} = 1/n \sum_{j=i}^{k} E_{T2,0-i(z)} \tag{3}$$

$$E_{f1,0(Z)} = 1/n \sum_{j=i}^{k} E_{f1,0-i(z)} \tag{4}$$

$$Df_{i2,0(Z)} = \sqrt{(E_{T2,0-i(z)} - E_{T2,0(Z)} / E_{T2,0(Z)})^2 + (E_{f1,0-i(z)} - E_{F1,0(Z)}) / E_{f1,0(z)})^2} \tag{5}$$

The cut-off frequency is 1.4 kHz. It consists of 6 operational amplifiers (opamps), 4 capacitors, and 13 resistors. Each operational amplifier consists of capacitor and nine MOS transistor. All

catastrophic faults on passive components are taken into account, thus giving 51 faulty cases. For each opamp, internal hard faults are also considered: all opens and shorts in MOS transistors [gate open (GOP), drain open (DOP), source open (SOP), gate–drain short (GDS),gate–source short (GSS), and drain–source short (DSS)] and shorts and opens for the internal capacitor *C*1.

Each one of the *I*PS and *V*OUT signal waveforms and the tolerance limit *Df*lim0 (*z*)(for the test algorithm A with the *discrimination factor* metric)or *MD*lim0 (*z*) (for the test algorithm B with the Mahalanobis distance metric) are computed from the fault-free circuits

4. SIMULATED RESULTS

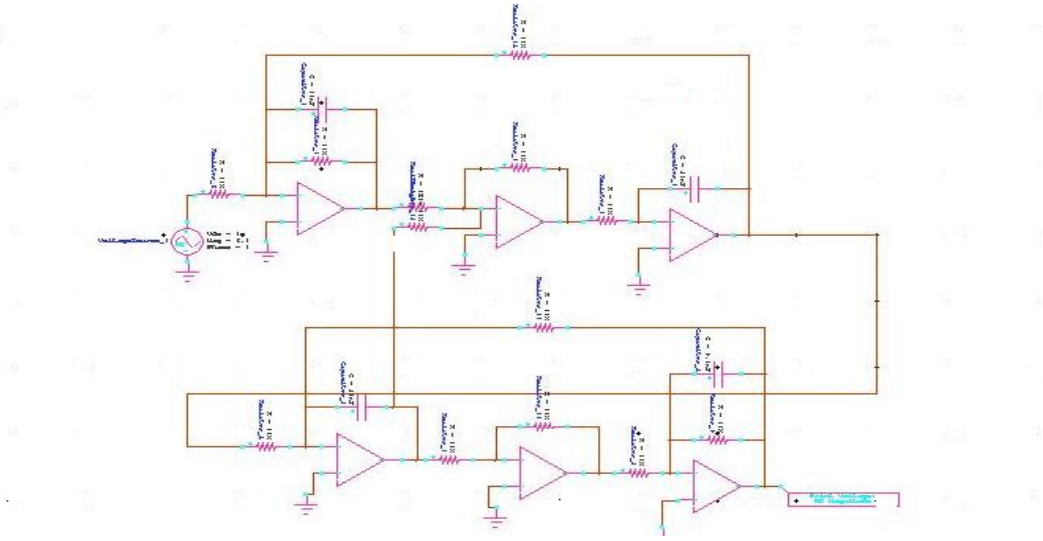

Fig 4 leaf frog filter circuit

In this circuit it can design the leaf frog filter it consists of operational amplifier resistor and capacitor it is to find out the faults of this circuits and to calculate the errors

4.1 INNER CIRCUIT DIAGRAM OF OPERATIONAL AMPLIFIER

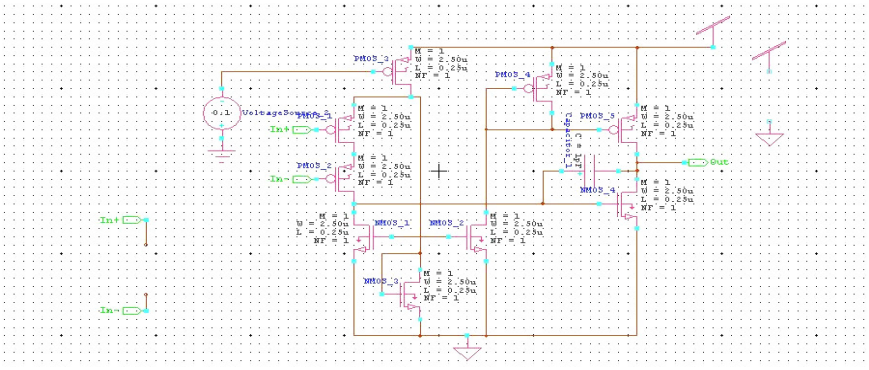

Fig 4.1 op-amp circuit of leaf frog circuit

In this op-amp circuits it consists of nmos and pmos transistor it is a internal circuit of leaf frog filter .it can be useful in to finding the faults in hardware and software faults it can estimate In which component the error has been detected to resolve the values and compare the previous values that values is to compare to existing values .in hard faults it can easily determine the

Values but soft faults it has some losses present in the circuit that has been detected

4.3 FREQUENCY RESPONSE OF FAULT FREE CIRCUIT

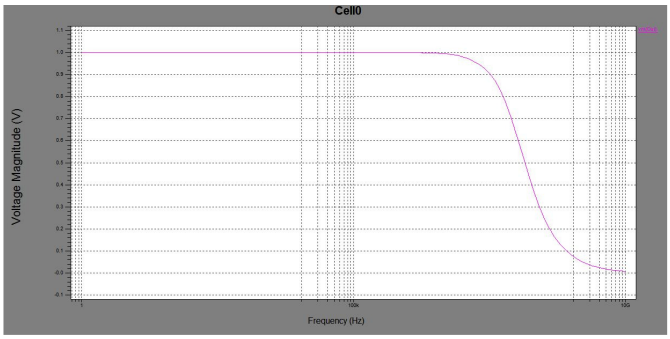

Fig 4.2 fault free of leaf frog circuit

4.4 OP AMP FAULT

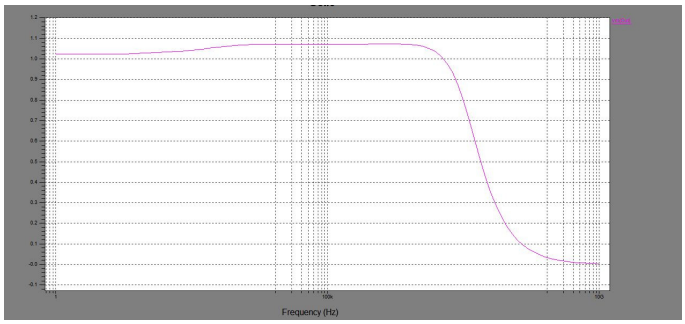

Fig 4.3soure open of leaf frog circuit

4.5 RESISTOR R4 FAULT

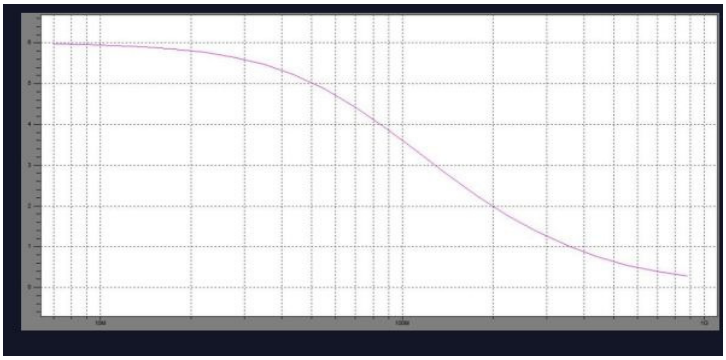

Fig 4.4 resistor r4 circuit of leaf frog circuit

4.6 BRIDGING RESISTANCE

Fig 4.5 bridging resistance of leaf frog circuits

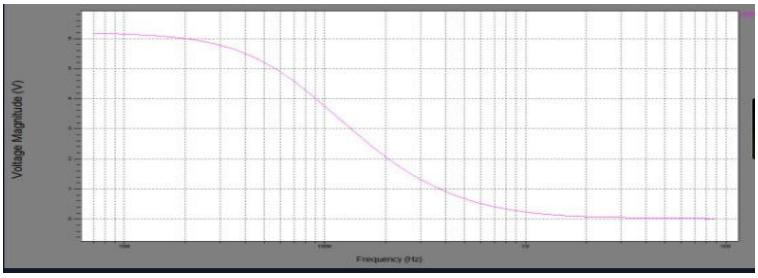

Fig 4.6 capacitor c4 leaf frog circuit

4.7 TABULAR FORM OF LEAF FROG CIRCUIT

Table 1 .distance measurement and eigen valuesof leaf frog circuit

	$Df_{(vout)}$	$Md_{(vout)}$	**Eigen value**				
			V_{maxi}	V_{min}	$K_{min,}$ $,K_{maxi}$	$B_{min,}$ B_{maxi}	Error values
Fault free circuits	1.35	1.35	18.4649	-0.433	24.245, -5.846	24.7479, -23.687	0.222
gate open	**1.3272**	**2.56**	20.122	-0.33	24.345, -5.762	24.647, -23.58	0.233
Resistor r5	0.0715	**2.75**	16.6149	-0.33	24.101, -5.456	24.54, -23.45	0.56
Capacitor fault c3	1.285	0.915	19.8140	-0.077	41.673 2, -27.988	21.228, -20.168	0.56
Drain open	1..88	**1.157**	2.621	-0.413	41.345, -27.45	21.28, -20.145	0.98
Bridging resistance	0.5039	**0.265**	19.044	-0.07	41.256, -27.045	21.023, -20.145	0.69

It ensures that the matrix Eigen values varies with the change of matrix elements. In this way the Eigen values of matrix *A[6]* and the elements of the parametric fault set of CUT can be put one-to-one correspondence. So the proposed method is available to implement the faults diagnosis for analog circuits[7]. The algebraic theory guarantees the correctness of this approach.

The tolerance limits for the fault-free(reference) circuit are also given in Table I. It is observed that, according to steps of the Main Test Phase in the *Opamp1_M1-GOP* (gate-open fault at M1 internal toopamp1) fault is not detectable using the *V*OUT [*Dfk*(*V*OUT) 1.32 < 1.35 = *Df*lim0 (*V*OUT) and *MDT*1,*k*(*V*OUT) =1.32 < 2.56 = *MD*lim *T*1,0(*V*OUT)]

When the *V*OUT signal is utilized, the fault detect ability percentage is 70.99% for the test algorithm B and 70.74%for the test algorithm A. The fault delectability percentage for the test algorithm B (70.99%) is attributed to the energy values from the trend coefficients (70.99% for "MDT1"), whereas the information from the detail coefficients results in lower fault detection percentage (64.41% for "MDF1")

5. CONCLUSION

All the analysis was made on low pass leap frog using tanner tools. The required coefficients were successfully calculated and compared with that of the given in the base paper we have got a variation of about 1-2 percent in the final values and we have extended this method to two other components apart from what are mentioned in the paper .Finally, we are successful in finding out the faulty component and also the variation in the faulty component value from its nominal values

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AN OPTIMIZED DEVICE SIZING OF TWO-STAGE CMOS OP-AMP USING MULTI-OBJECTIVE GENETIC ALGORITHM

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ABSTRACT

A novel approach for optimizing the transistor dimensions of two stage CMOS op-amp using Multi-Objective Genetic Algorithm (MOGA) is presented. The proposed approach is used to find the optimal dimensions of each transistor to improve op-amp performances for analog and mixed signal integrated circuit design. The aim is to automatically determine the device sizes to meet the given performance specifications while minimizing the cost function such as power dissipation and a weighted sum of the active area. This strongly suggests that the approach is capable of determining the globally optimal solutions to the problem. Exactness of performance prediction in the device sizing program (implemented in MATLAB) maintained. Here Six parameters are considered i.e., open loop gain, Phase Margin (PM), Area (A), Bandwidth of unity Gain (UGB), Power Consumption (P) and Slew Rate (SR). The circuit is simulated in cadence(Virtuoso Spectre) 0.18um CMOS technology.

KEYWORDS

Analog Design, complementary metal-oxide-semiconductor (CMOS), Optimization, Two-Stage Operational Amplifier, Multi-objective Genetic Algorithm (MOGA).

1. INTRODUCTION

The semiconductor industry is driven by the scaling of CMOS technology to improve the speed, performance and reduce the cost [1].the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [2]. The design process involves the two major steps, the first is the selection of the topology, and optimization of topology by obtaining the optimal dimensions of the transistors, by proposing suitable architecture to meet the given specifications and to do the hand calculations, Second step is to take the design, verify and optimize it. The hand calculations may take more design time as well as leads to mistakes but an automated optimization can save enormous design time. A new methodology is proposed to determine the transistor dimensions (i.e., Width and Length) for CMOS two-stage op-amps. This paper is planned into four sections. In section -II is

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about the Operational Amplifiers. In section-III and section-IV the Optimization Methodology and Result and Discussions are discussed. In section-V gives the conclusion of the paper.

2. OPERATIONAL AMPLIFIER

In this section, operational amplifier (op amp) design is discussed. Op-amp is used for several operations such as amplifying the signals, addition or subtraction, signal generators, and filters. In order to achieve these it must have high gain, high input resistance and it should function over a wide range of frequencies. Such op-amp can also be used in A/D converters, D/A converters, filters and sensing circuits.

2.1 Two-stage operational amplifier

This CMOS operational amplifier has four major blocks, first one is bias circuits (current mirror) is to establish the operating points of transistor in its saturation region, an input differential amplifier which provides a differential voltage or differential current as an output, improves the noise and offset performances. A compensation circuit for compensating the poles and to stabilize the circuit for example miller compensation. The second Gain circuit block is configured as a common-source amplifier to allow maximum output swings.

In this paper, for the two-stage operational amplifier, design parameters are considered. such as open loop DC gain, unity gain bandwidth (UGB), phase margin (PM), power consumption (Pc), area (A) and slew-rate (SR).

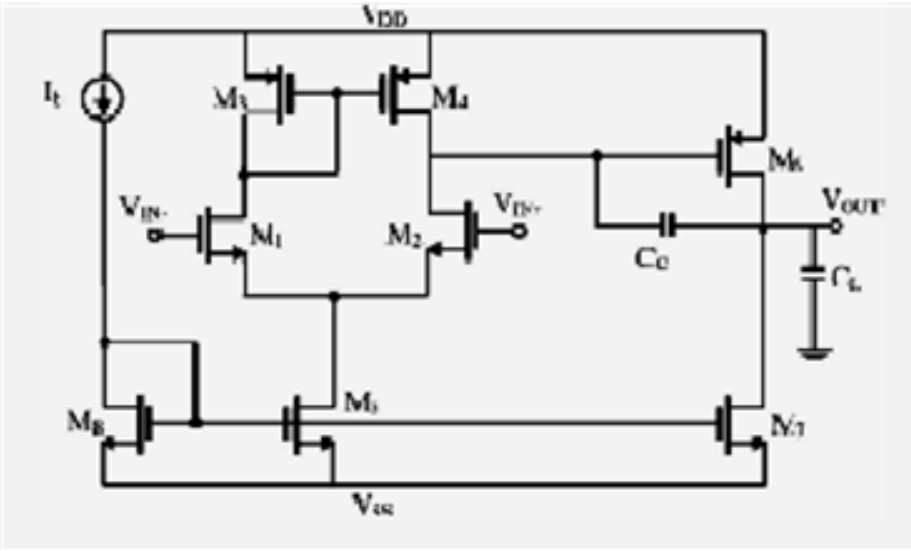

Fig.1 Two stage op-amp

2.1.1 Open loop DC Gain

$$A_V = \frac{g_{m1}}{g_{ds2} + g_{ds4}} . \frac{g_{m6}}{g_{ds7} + g_{ds6}}$$

2.1.2 UGB

The UGB is given as

$$GBW = \frac{g_{m1}}{C_c}$$

Where C_c is compensation capacitor

2.1.3 Phase Margin

The phase margin is given by the equation

PM=180-tan^{-1}(gain banwidth/pole1)- tan^{-1}(gain banwidth/pole2)- tan^{-1}(gain banwidth/zero)

2.1.4 Slew Rate

$$SR = \frac{I_5}{C_c}$$

2.1.5 Power Consumption

$$P = (V_{DD} - V_{ss})(I_5 + 2I_7)$$

3. OPTIMIZATION METHODLOGY

The op-amp design optimization employs genetic algorithms (GA's). Genetic Algorithm (GA) is concurrent evolution approach for optimization of transistor parameters, which follows the evolution of the living beings, In general The evolutionary algorithms uses three main principles: reproduction, selection and diversity of the species similar to natural evolution. Usually starts from and is an iterative process. The new generation solutions is then used in the next iteration of the algorithm then mutation, crossover operations are performed, until the satisfactory fitness level is reached for the population. After reaching the total number of generations the process is terminated. Optimal dimensions are represented as

[W1,L1,W3,L3,W5,L5,W6,L6,W7,L7,W8,L8].

The above process can be explained by using the flow chart shown in the Fig.2 below.

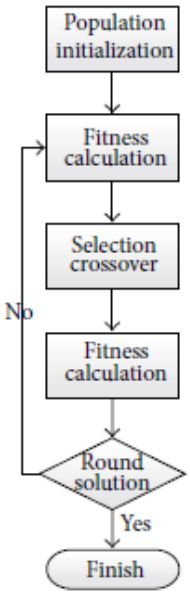

Fig.2 Genetic algorithm flowchart.

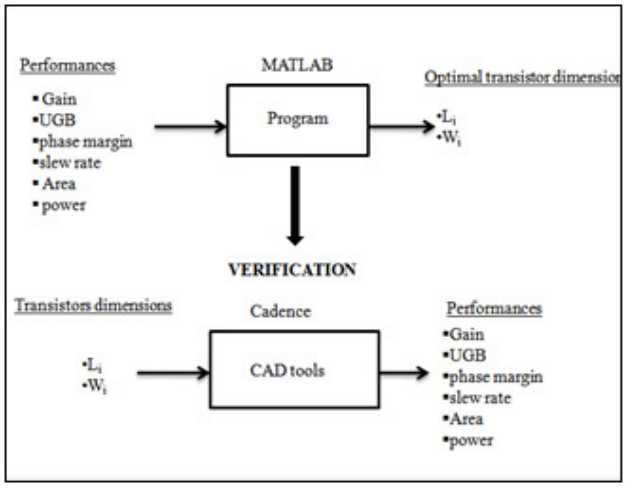

Fig.3 Op-amp design flow

4. SIMULATION AND DISCUSSION

The simulation results of an operational amplifier is measured in terms of open loop DC gain, unity gain bandwidth, phase margin(PM), slew rate(SR) and area(A). The optimization process involves the crossover, mutation, selection operations which are performed on each variable to improve the fitness score. This process will be iterated until the satisfactory fitness level is reached, if the total number of generations is generated then the process is terminated. Here the optimization method is implemented using MATLAB. The results of two-stage operational amplifier are the open loop DC gain is 85.14dB,unity gain bandwidth(UGB) is 66.5MHz,phase margin(PM) is 54^0 and slew rate(SR) is 50V/µs.

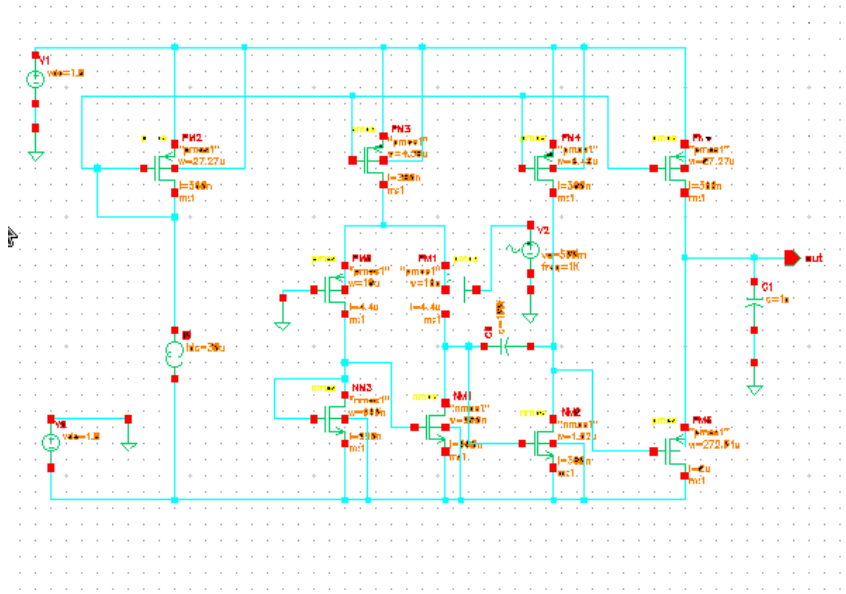

Fig.4 Schematic of 2 stage Op – amp

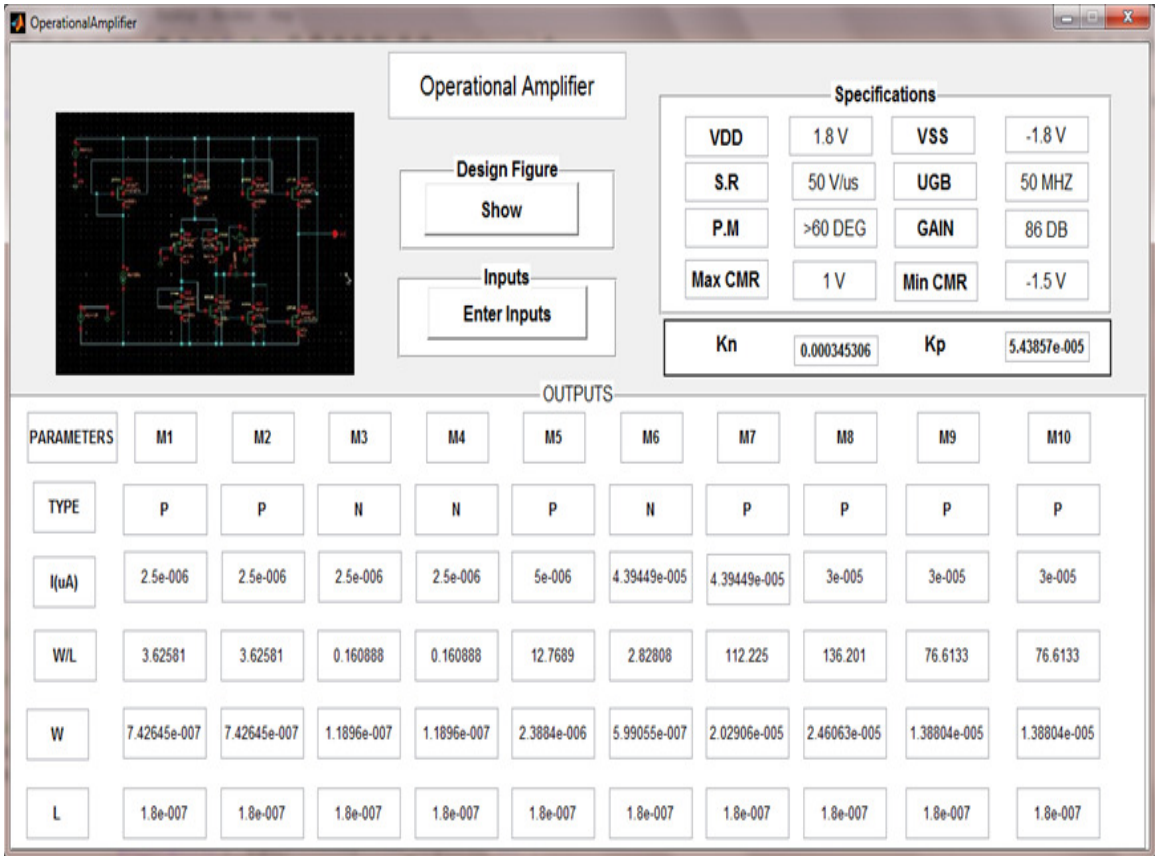

Fig.5 output window with W/L values of the 2 stage op-amp

Table I: optimized parameters of 2 stage op-amp

Transistor	W/L
M1	0.74u/0.18u
M2	0.74u/0.18u
M3	1u/0.18u
M4	1u/0.18u
M5	2.3u/0.18u
M6	0.59u/0.18u
M7	3.27u/0.18u
M8	24.6u/0.18u
M9	13.88u/0.18u
M10	13.88u/0.18u

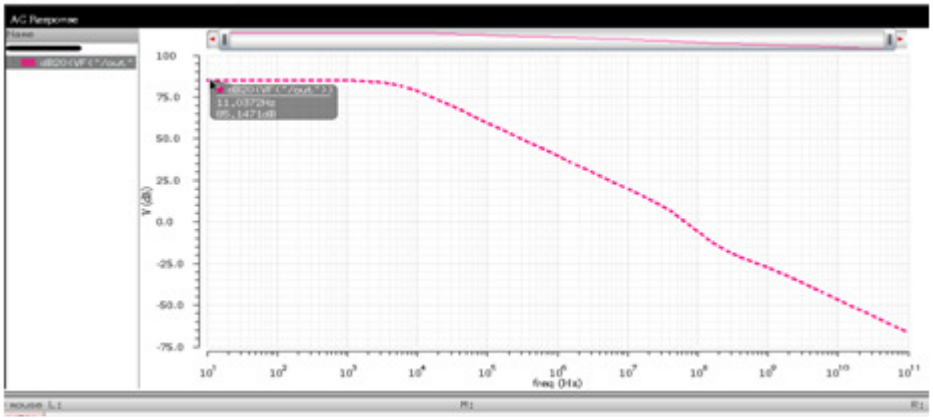

Fig.6 AC response for the 2 stage Op-amp

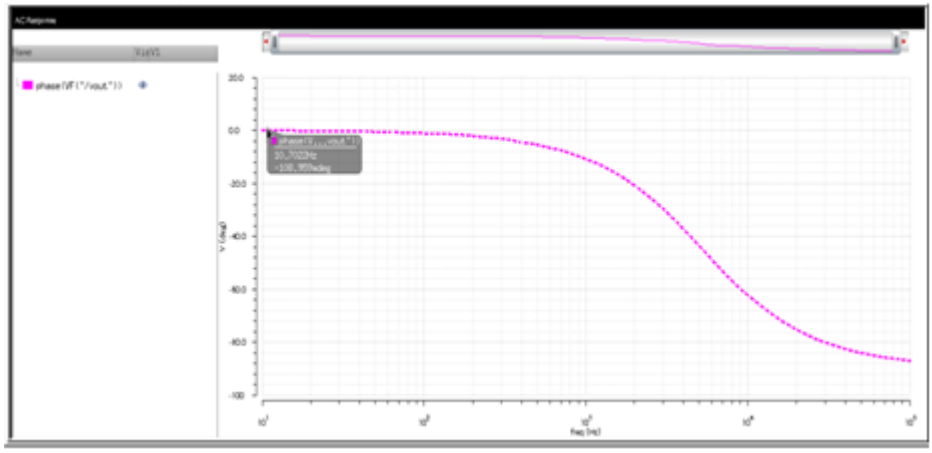

Fig.7 Phase response for the 2 stage Op-amp

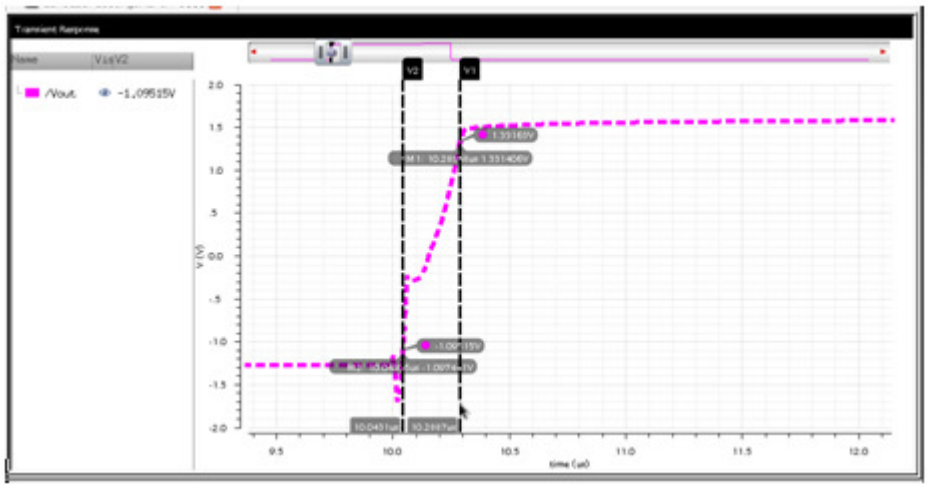

Fig.8 positive slew rate

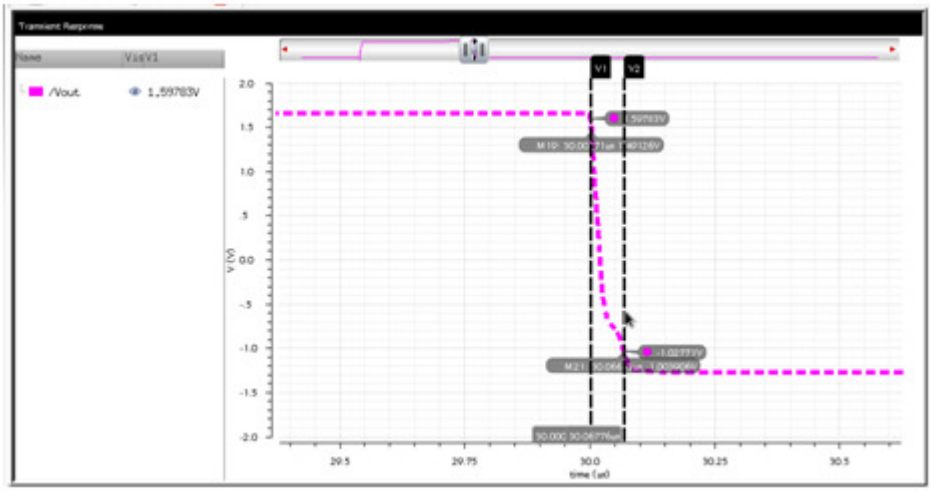

Fig.9 negative slew rate

Table II: The Optimized performance of 2-stage Op-Amp

Performance	Specifications	Simulation Results
DC gain (in dB)	≥85	85.14
Unity Gain Bandwidth(in MHz)	>50	66.5
Phase Margin(in deg)	60	54
Slew Rate(V/us)	50	48
Area(m^2)	Min	550
Power(uW)	Min	47

3. CONCLUSION

In this paper, a multi objective optimization algorithm for mixed signal circuit design is implemented using Matlab. Circuit equations and genetic algorithm is combined and produced the tool in order to determine the optimal dimensions of a two-stage op-amp. The results balance the desired and obtained specifications this shows the efficient approach in the analog design where the design time is reduced in the proposed approach. It can be concluded that the proposed multi-objective genetic algorithm based approach is efficient and gives optimized results for circuits design and reduce the design time.

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DESIGN VERIFICATION AND TEST VECTOR MINIMIZATION USING HEURISTIC METHOD OF A RIPPLE CARRY ADDER

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ABSTRACT

The reduction in feature size increases the probability of manufacturing defect in the IC will result in a faulty chip. A very small defect can easily result in a faulty transistor or interconnecting wire when the feature size is less. Testing is required to guarantee fault-free products, regardless of whether the product is a VLSI device or an electronic system. Simulation is used to verify the correctness of the design. To test n input circuit we required 2^n test vectors. As the number inputs of a circuit are more, the exponential growth of the required number of vectors takes much time to test the circuit. It is necessary to find testing methods to reduce test vectors . So here designed an heuristic approach to test the ripple carry adder. Modelsim and Xilinx tools are used to verify and synthesize the design.

KEYWORDS

Ripple carry Adder, Test vectors, Modelsim Simulator

1. INTRODUCTION

The complexity of VLSI technology has reached the point where we are trying to put 100 million transistors on a single chip, and we are trying to increase the on-chip clock frequency to 1 *GHz.* Transistor feature sizes on a VLSI chip reduce roughly by 10.5% per year, resulting in a transistor density increase of roughly 22.1% every year. An almost equal amount of increase is provided by wafer and chip size increases and circuit design and process innovations. This is evident that, 44% increase in transistors on microprocessor chips every year. This amounts to little over doubling every two years[3]. The doubling of transistors on an integrated circuit every 18 to 24 months has been known as Moore's since the mid-1970s. Although many have predicted its end, it continues to hold, which leads to several results [1].

The reduction in feature size increases the probability that a manufacturing defect in the IC will result in a faulty chip[2]. A very small defect can easily result in a faulty transistor or interconnecting wire when the feature size is less than 100 nm. Furthermore, it takes only one faulty transistor or wire to make the entire chip fail to function properly or at the required operating frequency. Defects created during the manufacturing process are unavoidable, and, as a result, some number of ICs is expected to be faulty therefore, testing is required to guarantee fault free products, regardless of whether the product is a VLSI device or an electronic system

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composed of many VLSI devices. It is also necessary to test components at various stages during the manufacturing process. For example, in order to produce an electronic system, we must produce ICs, use these ICs to assemble printed circuit boards (PCBs), and then use the PCBs to assemble the system. There is general agreement with the rule of ten, which says that the cost of detecting a faulty IC increases by an order of magnitude as we move through each stage of manufacturing, from device level to board level to system level and finally to system operation in the field. Electronic testing includes IC testing, PCB testing, and system testing at the various manufacturing stages and, in some cases, during system operation. Testing is used not only to find the fault-free devices, PCBs, and systems but also to improve production yield at the various stages of manufacturing by analyzing the cause of defects when faults are encountered. In some systems, periodic testing is performed to ensure fault-free system operation and to initiate repair procedures when faults are detected. Hence, VLSI testing is important to designers, product engineers, test engineers, managers, manufacturers, and end-users [1].

Fig. 1 explains the basic principle of digital testing. Binary patterns (or *test vectors*) are applied to the inputs of the circuit. The response of the circuit is compared with the expected response [4, 5]. The circuit is considered good if the responses match. Otherwise the circuit is faulty. Obviously, the quality of the tested circuit will depend upon the thoroughness of the test vectors. Generation and evaluation of test vectors is one of the main objectives of this paper. VLSI chip testing is an important part of the manufacturing process.

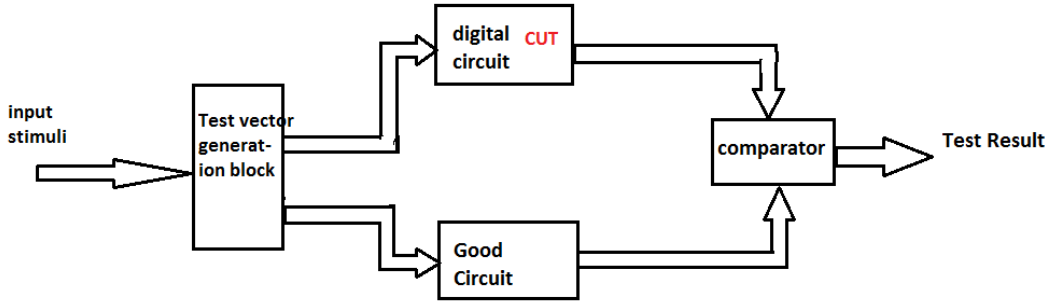

Fig.1. Principle of Testing

2. PROPOSED SYSTEM

Simulation serves two distinct purposes in electronic design. First, it is used to verify the correctness of the design and second, it verifies the tests. The simulation process is illustrated in Figure 2. The process of realizing an electronic system begins with its specification, which describes the input or output electrical behaviour (logical, analog, and timing) and other characteristics (physical, environmental, etc.)

The specification is the starting point for the design activity. The process of synthesis produces an interconnection of components called a net list. The design is verified by a true-value simulator. True-value means that the simulator will compute the response for given input stimuli without injecting any faults in the design. The input stimuli are also based on the specification.

Typically, these stimuli correspond to those input and output specifications that are either critical or considered risky by the synthesis procedures. A frequently used strategy is to exercise all functions with only critical data patterns. This is because the simulation of the exhaustive set of

data patterns can be too expensive. However, the definition of "critical" often depends on designer's heuristics.

The true-value simulator in Figure 2. Computes the responses that a circuit would have produced if the given input stimuli were applied. In a typical design verification scenario, the computed responses are analyzed (either automatically, or interactively, or manually) to verify that the designed net list performs according to the specification. If errors are found, suitable changes are made, until responses to all stimuli match the specification.

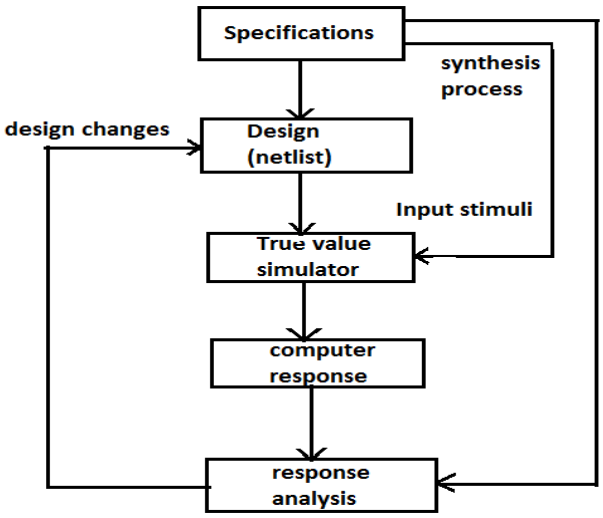

Fig. 2. Block diagram for Design Verification

2.1. Test vector Minimization method

A combinational logic circuit is designed to add two 4-bit binary numbers. This circuit has 9 binary inputs and 5 outputs. To verify the circuit the number inputs required to the circuit is 2^n ie., 512, to completely verify the correctness of the implemented logic, we must simulate input vectors and check that each produces the correct sum output.

This is clearly impractical. So, the designer must simulate some selected vectors. For example, one may add pairs of integers where both are non-zero, one is zero, and both are zero shown in Fig. 3. Then add a large number of randomly generated integer pairs. Such heuristic, though they seem arbitrary, can effectively find many possible errors in the designed logic. The next example illustrates a rather simple heuristic.

FA0			FA1			FA2			FA3			Cout
C_0	A_0	B_0	C_1	A_1	B_1	C_2	A_2	B_2	C_3	A_3	B_3	C_4
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1	0	0	1	0
0	1	0	0	1	0	0	1	0	0	1	0	0
0	1	1	1	0	0	0	1	1	1	0	0	0
1	0	0	0	1	1	1	0	0	0	1	1	1
1	0	1	1	0	1	1	0	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1

VECTOR NO.	BIT : $C_0 A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3$	Input $C_n A_n B_n$ to FAn
1	000000000	000 applied to all FAs
2	001010101	001 applied to all FAs
3	010101010	010 applied to all FAs
4	011001100	011 applied to FA0,FA2 & 100 applied to Fa1,FA3
5	100110011	100 applied to FA0,FA2 & 011 applied to FA1,Fa3
6	101010101	101 applied to all FAs
7	110101010	110 applied to all FAs
8	111111111	111 applied to all FAs

Fig.3. Binary values applied to the FA's

Design verification heuristic for a ripple-carry adder: Fig. 4. shows the logic design of an adder circuit. The basic building block in this design is a full-adder that adds two data bits, and one carry bit, to produce sum and carry outputs, and respectively. For logic verification, one possible strategy is to select a set of vectors that will apply all possible inputs to each full adder block. For example, if we set and apply all four combinations shown in Fig.3.

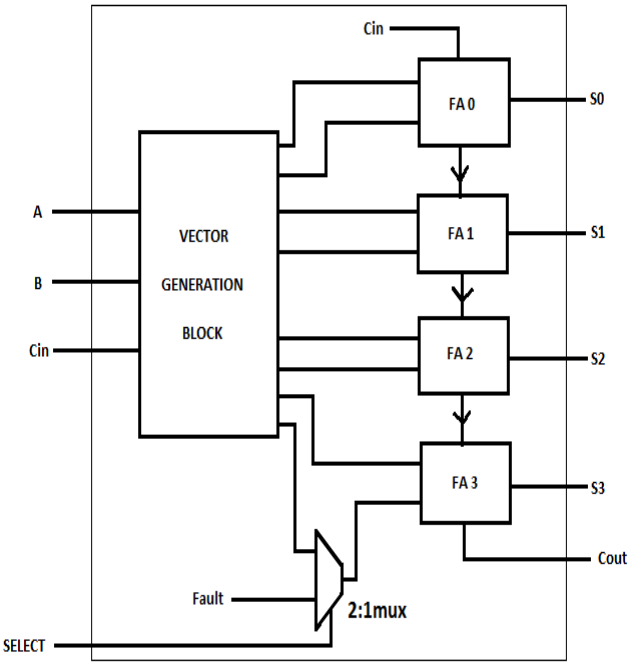

Fig.4. Heuristic method for test minimization

Test vectors are generated from the logic block. Inject the SA1 or SA0 to one input to the full adder through 2:1 Multiplexer. If the multiplexer input is 0, true bit will be selected and multiplexer input is 1, faulty input is selected at the input of the full adder. Associated carry will

be generated at the full adder and fault free and faulty outputs are compared. If the output is different fault will be detected. Depending on the input, carry will be propagated, that effects the next adder circuit also. 8 test vectors are sufficient to test the circuit. One significant advantage of simulation is that all internal signals of the circuit can be examined. This reduces the complexity of verification. The regular pattern in each vector allows us to expand the width of the vector without increasing the number of vectors to an adder of arbitrarily large size.

3. RESULTS AND DISCUSSIONS

SA1 fault is injected to the 3rd full adder of a circuit, Fault free output and faulty outputs are observed, if the two are different fault is identified and marked in the diagrams shown in Fig. 5. and Fig.6.

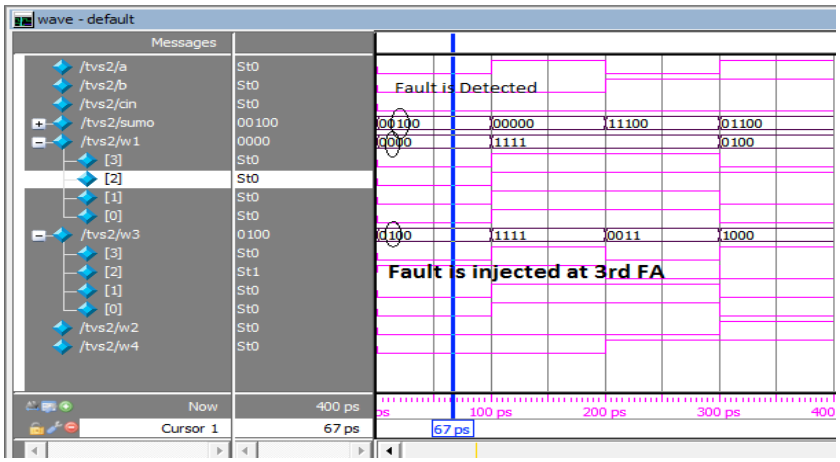

Fig. 5. Fault is detected at the output of the full adder.

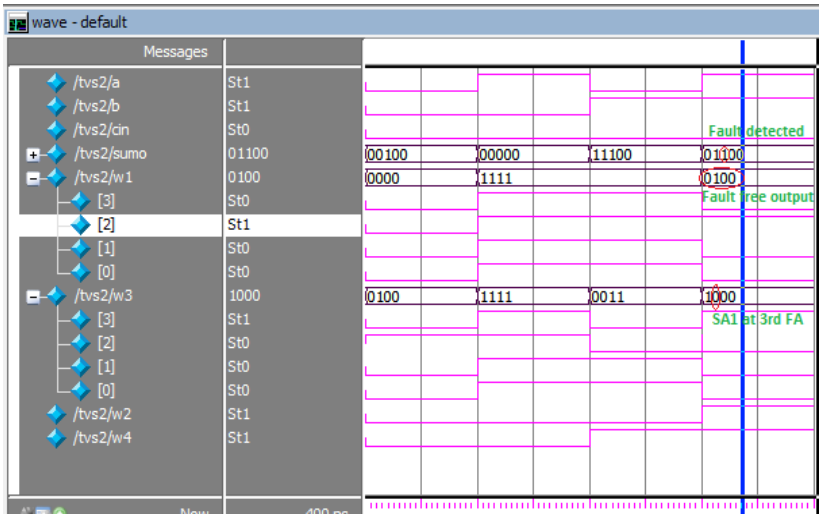

Fig.6. Fault is detected at the output of the full adder.

Output is analyzed at the output of the full adder, that fault is propagated to next full adder, with final carryout 0.

3.1. Register Transistor level diagram generated by tool shown in Fig.7.

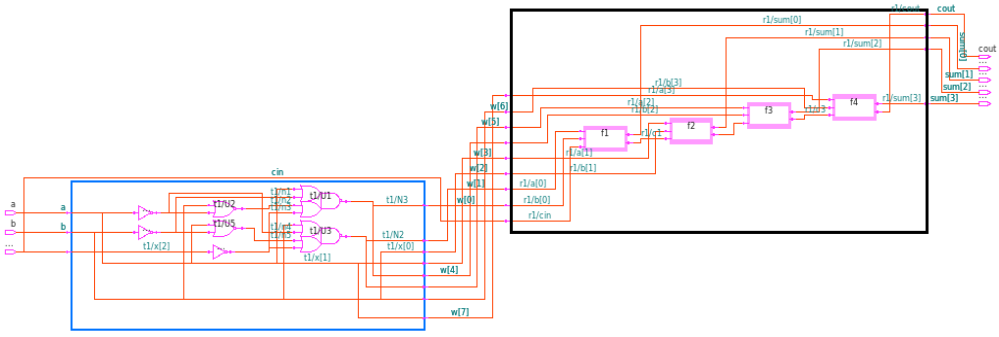

Fig.**7.** Register transistor level diagram of a Ripple Carry Adder

Dynamic power, Leakage power, Switching power given by the tool is shown in the report.

```
    Capacitance Units = 0.100000ff
    Time Units = 1ns
    Dynamic Power Units = 100nW    (derived from V,C,T units)
    Leakage Power Units = Unitless


  Cell Internal Power  =   0.0000 nW    (0%)
  Net Switching Power  =   9.4924 uW  (100%)
                         ---------
Total Dynamic Power    =   9.4924 uW  (100%)

Cell Leakage Power     =   0.0000

Error: Either dynamic power or leakage power, in the library, is unitless. Unable to display complete power group summary.
Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000               NA   (     N/A)
memory             0.0000            0.0000            0.0000               NA   (     N/A)
black_box          0.0000            0.0000            0.0000               NA   (     N/A)
clock_network      0.0000            0.0000            0.0000               NA   (     N/A)
register           0.0000            0.0000            0.0000               NA   (     N/A)
sequential         0.0000            0.0000            0.0000               NA   (     N/A)
combinational      0.0000         9.4924e+03           0.0000               NA   (     N/A)
--------------------------------------------------------------------------------------------------
Total              0.0000 nW      9.4924e+03 nW        0.0000               NA

***** End Of Report *****
```

Dynamic power, Leakage power, Switching power Report.

4. CONCLUSIONS

Test vector minimization method is designed in this paper. A heuristic method is used to reduce the test vectors of a ripple carry adder. Testing operation of the ripple carry adder is performed. This method reduces the number of test vectors to detect the faults. The regular pattern allows us to expand the width of the vector without increasing the number of vectors to an adder of arbitrary large size. Design compiler, Modelsim and Xilinx tools are used to analyze the method.

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INTENTIONAL BLANK

A 130-NM CMOS 400 MHZ 8-BIT LOW POWER BINARY WEIGHTED CURRENT STEERING DAC

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ABSTRACT

A low power low voltage 8-bit Digital to Analog Converter consisting of different current sources in binary weighted array architecture is designed. The weights of current sources are depending on the binary weights of the bits. This current steering DAC is suitable for high speed applications. The proposed DAC in this paper has DNL, INL of ±0.04, ±0.05 respectively and the power consumption of 16.67mw.

This binary array architecture is implemented in CMOS 0.13µm 1P2M technology has good performances in DNL, INL and area compared with other researches.

KEYWORDS

Current Steering, Binary Weighted, Current Source, INL(Integral Non Linearity), DNL (Differential Non Linearity), Power.

1. INTRODUCTION

Real world signals are in analog form but digital signals are processed easily with simple circuits so analog signals are converted into digital form. The digital signals are converted back to analog form to do some real world functions. The circuit that performs this conversion are digital-to-analog converters, and at the output of this DACs load is connected. In this paper binary weighted CMOS current steering DAC is designed with current sources and resistor at the output stage. Each current source has weight with respect to the position of the current source.

Basically there are three types of current steering architectures unary array, binary array, and segmented array architecture. Unary current DACs use a single-current element for each quantization step. Unary current DACs are analogous to resistor divider DACs with a resistor element for each LSB. The drawback of unary arrays is that the complexity of the digital decoder is exponentially related to the resolution.

Binary current DACs group current elements into binary multiples that are turned on or off directly with the input bits. This eliminates the decoder required in unary current DACs. Segmented arrays consist of different sub-arrays, or segments, each with a potentially different array coding. The MSB-segment is a unary array with 2^M-1 element and represents the upper M bits. The LSB-segment realizes the lower L bits in a binary array.

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The current source used here has no capacitance so the circuit need not to be charge or discharge in ON state. For high speed and high resolution designs current steering Digital to Analog Converters are more suitable. As frequencies and conversion rates increases, frequency domain parameters like SNR, SFDR parameters become more useful than static parameters like INL and DNL.

2.CIRCUIT AND LAYOUT

2.1.Current Source

The current source used here is driven by the binary input. To act as a current source the gate voltage must be constant. The current source performance is improved by improving two parameters i) small signal output resistance by increasing resistance a more constant current over a large range of Vout values. ii) Reduce the V_{min} voltage by allowing a large range of V_{out} over which current source work properly. To reduce V_{min} by increasing value of W/L and adjusting the gate to source voltage to get the same output current.

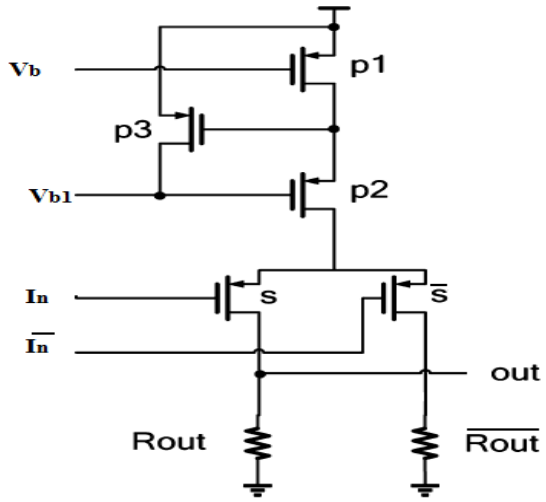

Figure1:Schematic diagram of current source

In the Figure 1: P_1 controls the value of current by varying width of P_1. The goal of MOSFETs *S* and $\overline{S}$ they act like switches. The gate terminal of *S* is connected to binary input. MOS *S* turns on the switch and $\overline{S}$ turns off the switch for a given input. The current sources that are turned on generate current flows through the output resistor R_{out} to generate an analog output from the DAC. MOSFET P_3 is used to increase the output impedance. The high output impedance can improve the performance of INL and SFDR. The 8-bit DAC requires 8 current sources and all the currents from each current sources are added at the output stage. The layout of the current source is shown in Figure 2.

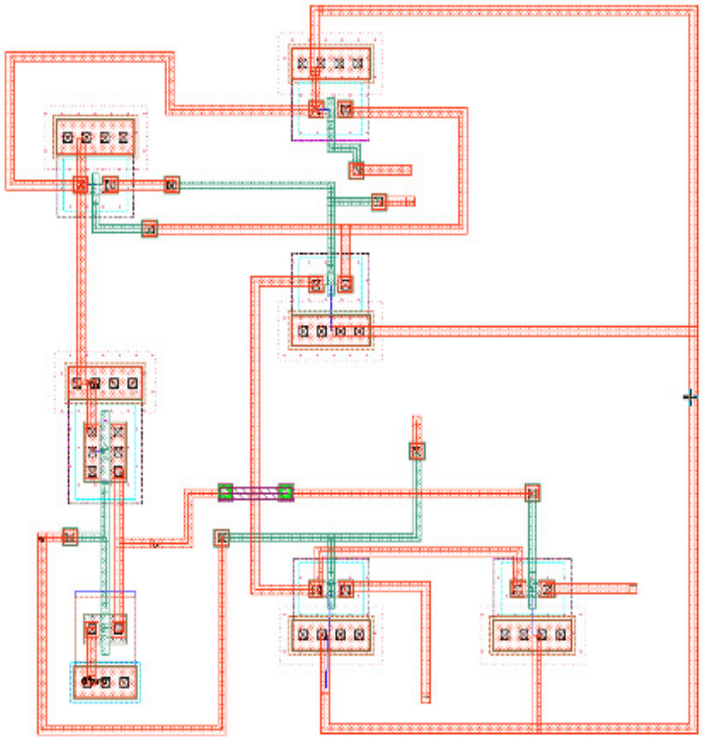

Figure 2: Layout of the current source.

2.2.Binary Weighted Dac

Now a day's the interface between the digital systems and analog systems are Digital to Analog Converters. The current steering DAC architectures are intrinsically fast, cost effective, and have high power efficiency [5][6]. The current-steering DAC replaces the resistor element in the resistor DAC architectures with a MOSFET current element and uses some form of summation of the current elements to produce the result. Binary weighted DACs group current elements into binary multiples that are turned on or off directly with the input bits. Figure 3: shows the general block diagram of binary weighted DAC. This eliminates the decoder required in unary current DACs. Unary and binary current DACs are often used together. Mostly, unary DACs are used for the MSB current elements because of their inherent monotonicity. Binary DACs are used for the LSB elements because of their much smaller size when created with weighted transistors.

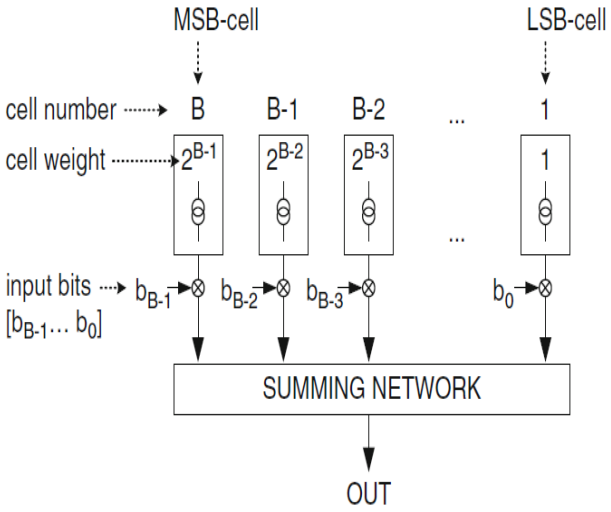

Figure 3:Binary weighted DAC architecture

Figure 4: Shows the schematic diagram of current source circuit designed by using PMOS transistors. A 50Ω resistor R_{out} is connected at the output. The relation between the output resistance and the achievable INL specification is given by:

$$INL= I*R^2_{out}*N^2/(4*R_{imp})$$

Where R_{out} is the load resistor, I is the LSB current,N is the total number of unit current sources [7].

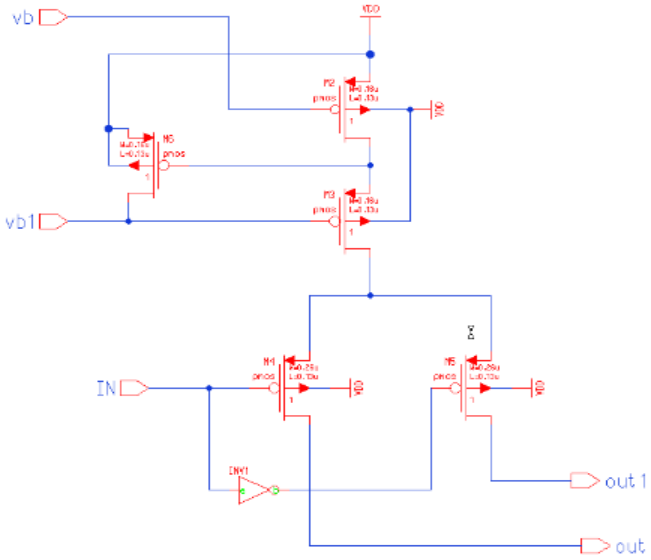

Figure 4:Schematic of Current Source

Figure 5: Shows the schematic of 8-bit DAC. This DAC using 8 current sources each current source has its own weights according to the position where it is used.

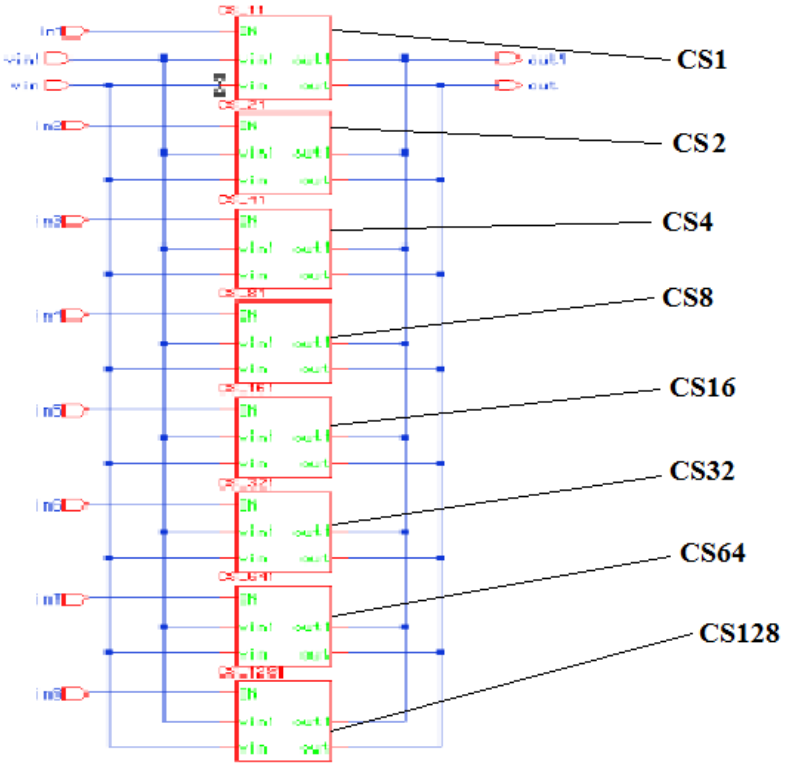

Figure 5:Schematic of 8-bit DAC

3. EXPERIMENTAL RESULTS

Figure 6: Shows the 8-bit DAC, which consists of current source modules of different weights. The digital input bits In_1 and In_2 drives the first two current sources of having weights 1 and 2 gives a current of I_1 and I_2 respectively. The current sources driven by inputs In_3,In_4,In_5,In_6,In_7,In_8 are having weights 4,8, 16, 32, 64 and 128 times of the current sources driven by In_1 respectively. The output analog values corresponding to digital inputs 00000000, 00100000, 01000000, 10000000, 11111111 are shown in Figure 7. The proposed 8-bit DAC was implemented using Mentor Graphics CMOS 0.13nm 1P2M technology with supply voltage 3.3V at sample rate 400MHz.

Differential nonlinearity is the difference of the output level between two adjacent codes. Integral nonlinearity is the measure of the actual output voltage level minus the ideal level. The values of DNL and INL after simulation are ± 0.04 and ± 0.05. The loading effect may degrade the performance.

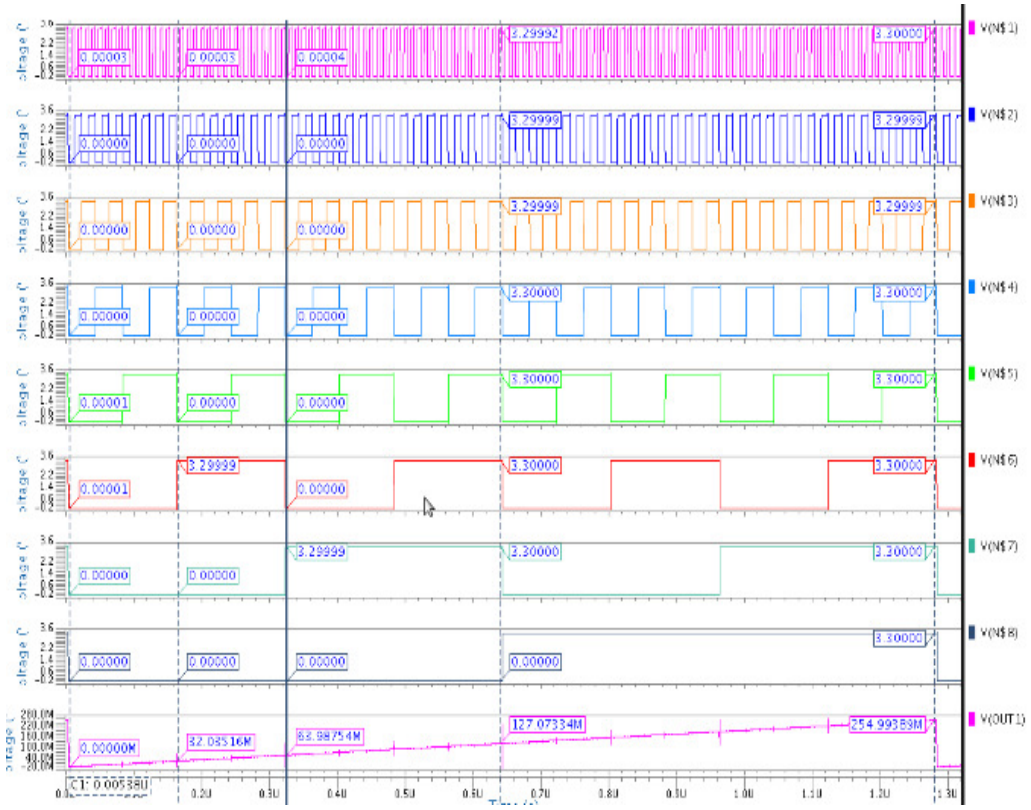

Figure 6: Simulation results of 8-bit DAC

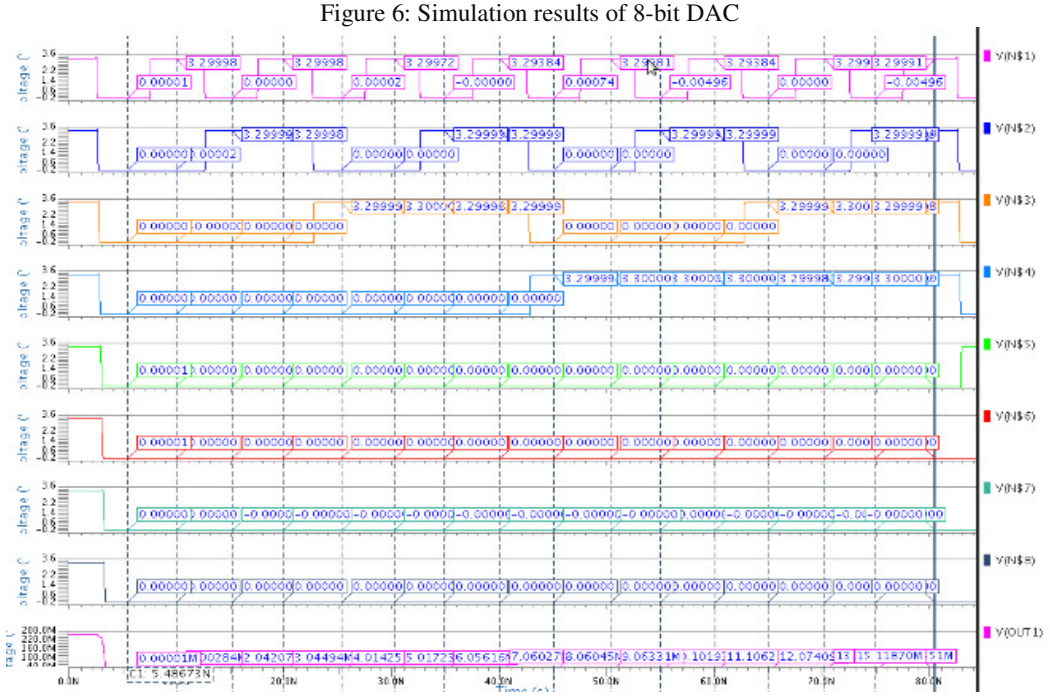

Figure 7:Results of first 15-binary values

The result of the 8-bit binary weighted DAC are shown in the Figure 6. This DAC eliminates the decoder circuit and the output of M-bit DAC is 0 to 2^M-1 i.e 0 to 255. The DAC is producing an output of 0mv, 4.014mv, 8.060mv and 15.03mv respectively for digital inputs of 0(00000000), 4(00000100), 8(00001000) and 15(00001111). The power dissipation of the DAC is 16.66mw.

Ref. [1] is a 10-bit current steering segmented DAC. Compared to this work the DNL of the circuit is less and here we are not using any decoder so the circuit complexity, the area occupied is less and transistor count is also very less.

Table 1:Summary of Experimental Results.

Parameters	[1]	[2]	[3]	[4]	This Work
Resolution	10	8	10	10	8
Sample rate(MHz)	200	100	210	80	400
DNL	±0.06	+0.31/–0.09	0.7	0.55	< 0.04
INL	±0.04	+0.26/–0.17	1.1	0.4	±0.05
Supply Voltage (v)	3.3	3.3	3.3	2.5	3.3/3
Power (mw)	7.9	27.5	83	27.65	16.67/7.211
Technology (nm)	350	130	350	250	130

4. CONCLUSION

In this paper, a 8-bit current steering binary weighted DAC was implemented. The technology used here is CMOS 0.13µm 1P2M process. The circuit is operated at two supply voltages 3.3v and 3v at the sample rate of 400 MHz. It achieved a DNL and INL of ±0.04 LSB and ±0.05 LSB, respectively.

The power consumption was about 16.67 mw at the sample rate of 400MHz. While the power supply is 3v respective power consumption is 7.211mw. This work presented a good performance when compared with researches in area, DNL, INL and power consumption.

ACKNOWLEDGEMENTS

We the authors would like to take this opportunity to extend our thanks to Department of ECE, MVGR College of Engineering, Vizianagaram for providing required tools to do research in VLSI Domain.

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DESIGN OF PROCESSING ELEMENT (PE3) FOR IMPLEMENTING PIPELINE FFT PROCESSOR

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ABSTRACT

Multiplexing is a method by which multiple analog message signals or digital data streams are combined into one signal over a shared medium. In communication, different multiplexing schemes are used. To achieve higher data rates, Orthogonal Frequency Division Multiplexing (OFDM) is used due to its high spectral efficiency. OFDM became a serious alternative for modern digital signal processing methods based on the Fast Fourier Transform (FFT).The problems with Orthogonal subcarriers can be addressed with FFT in communication applications. An 8-bit processing element (PE3), used in the execution of a pipeline FFT processoris designed and presented in this paper. Simulations are carried out using Mentor Graphics tools in 130nm technology.

***KEYWORDS*:**

Multiplexing, OFDM, FFT processor, Mentor Graphics tools.

1. INTRODUCTION

InDiscrete Signal Processing and telecommunications, Discrete Fourier Transform (DFT) is essential. Cooley and Tukey [1] proposed FFT to overcome the intensive computation, which has applications involving OFDM, such as WiMAX, LTE, DSL, DAB/DVB systems, and efficiently reduced the time complexity from $O(N^2)$ to O (Nlog 2N), where N denotes the FFT size. Different FFT processors developed for hardware implementation are classified as memory based and pipeline based architectures [2-4]. Memory-based architecture (single Processing Element (PE) approach), consists of a principal Processing Element and multiple memory units resulting in reduced power consumption and less hardware than the pipeline architecture, but have disadvantages like low throughput, long latency, and cannot be parallelized. Besides, the pipeline architecture can overcome the disadvantages of the memory based architecture style, with an acceptable hardware overhead.

Single-path Delay Feedback (SDF)pipeline and Multiple-path Delay Commutator (MDC) pipeline architectures are the two widely used design styles in pipeline FFT processors. SDF pipeline FFT [2-5] requires less memory, easy to design, utilizes less than 50% of the multiplication computation, and its control unit is used in portable devices In view of the advantages, the Radix-2 SDF pipeline architecture is considered in implementing the FFT

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processor. Three processing elements are used in the architecture of the proposed design of FFT processor [1]. In this paper, design of 8-bit processing element (PE3) is implemented.

2.FFT ALGORITHM

The DFT X_k of an N-point discrete-time signal x_n is defined by:

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \qquad ,0 \le k \le N-1 \tag{1}$$

where $W_N^{nk} = e^{-j2\pi nk/N}$ is twiddle factor.

The direct implementation of DFT is difficult to realize due to the requirement of more hardware. Therefore, to reduce its hardware cost and speed up the computation time, FFT was developed. By using Decimation-in-Time (DIT) or decomposition or Decimation-in-Frequency (DIF), FFT analyzes an input signal sequence to construct a Signal-Flow Graph (SFG) that can be computed efficiently. DIF decomposition is employed as it meets the operation of SDF pipeline architecture. A radix-2 DIF FFT SFG for N=8 is presented in Figure1.

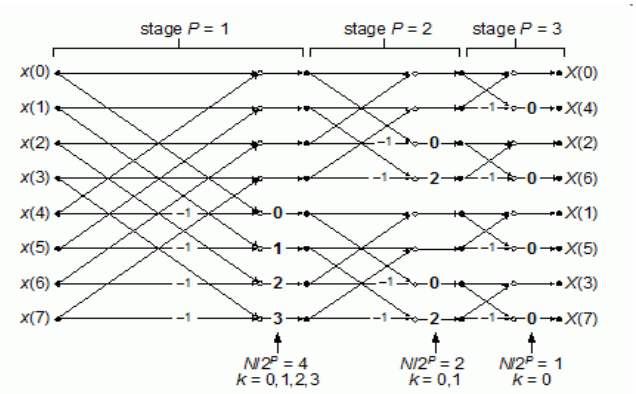

Figure1. Radix-2 Decimation-In-Frequency Fast Fourier Transform Signal Flow Graph for N=8.

To perform FFT computing, complex multiplication scheme [6-11] is used, as a result hardware cost is increased due to the use of ROM and complex multipliers.

DIF FFT is suitable for hardware implementation as it has a regular SFG and requires less complex multipliers resulting in smaller area of the chip. For example, an input signal multiplied by W^1_8 in Figure. 1 can be expressed as:

$$(x + jy)W_8^1 = \sqrt{2}[(x + y) + j(x - y)]/2, \tag{2}$$

Where $(x + jy)$ denotes a complex discrete-time signal.

Similarly, the complex multiplication of W^3_8 is given by

$$(x+jy)W_8^3 = \sqrt{2}[(x-y)-j(x+y)]/2 \tag{3}$$

Both the equations (2) and (3) will ease hardware implementation.
From symmetric property of the twiddle factors, the complex multiplications can be one of the following three operation types:

$$\text{Type 1: } W_N^k(x+jy) = W_N^{k-(N/4)}(y-jx) \qquad \frac{N}{4} < k < \frac{N}{2} \tag{4}$$

$$\text{Type 2: } W_N^k(x+jy) = -W_N^{k-(N/2)}(x+jy) \qquad \frac{N}{2} < k < \frac{3N}{4} \tag{5}$$

$$\text{Type 3: } W_N^k(x+jy) = -W_N^{k-\left(3N/4\right)}(y-jx) \qquad \frac{3N}{4} < k < N \tag{6}$$

Any twiddle factor can be obtained by combining the twiddle-factor primary elements (equations (4-6)). The three operation types are used to find the twiddle factor required to reduce the size of the ROM. Additional operation types are given below:

$$\text{Type 4: } W_N^k(x+jy) = \left[W_N^{(N/4)-k}(y+jx)\right]^* \qquad 1 \le k < \frac{N}{4} \tag{7}$$

$$\text{Type 5: } W_N^k(x+jy) = -j\left[W_N^{(N/2)-k}(y+jx)\right]^* \qquad \frac{N}{4} < k < \frac{N}{2} \tag{8}$$

Where * indicates conjugate value. A significant shrinkage of twiddle- factor ROM table can be obtained, after the third butterfly stage as the complex multiplications will be reduced by using the five operation types.

3.ARCHITECTURE OF FFT:

A radix-2 8point pipeline FFT processor is presented in Figure 2.The architecture of the pipeline FFT processor contains three processing elements namely,PE3, PE2 and PE1, a complex constant multiplier and delay-line buffers. To remove the twiddle-factor ROM, a reconfigurable complex constant multiplier is used which reduces chip area required and power consumption of FFT processor.

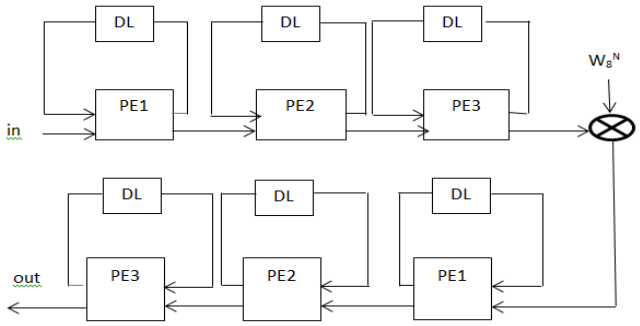

Figure 2. Radix-2 8 point pipeline FFT processor.

PROCESSING ELEMENTS

The three processing elements PE1, PE2, and PE3 of the radix-2 pipeline FFT processor are presented in Figures.3 to 5, respectively. The Processing Elements processes each stage of the butterfly presented in Figure.1. PE3 stage implements a simple radix-2 butterfly, and functions as the sub module for PE2 and PE1 stages.

In Figure 3, Iinand Iout denote the real parts, and Qin and Qoutare the imaginary parts of the input and output data, respectively. Similarly, DL_Iinand DL_Iout stand for the real parts and DL_Qinand DL_Qoutare for the imaginary parts of input and output of the DL buffers, respectively. The multiplication by *–j* or 1 is required for PE2 stage. By taking 2's complement of the input value, multiplication by -1 in Figure.4 can be done practically.

Compared to PE2 stage, calculations in PE1 stage are more complex, as it computes the multiplications by –j, $W_N^{N/8}$ and $W_N^{3N/8}$ respectively. Since $W_N^{N/8}$ =- $W_N^{3N/8}$either the multiplication by $W_N^{N/8}$followed by multiplication with *–j* or the reverse of the previous calculation can be done. The cascaded calculations along with multiplexers are used in PE1 stage calculations and forms a low -cost hardware by saving a bit-parallel $W_N^{3N/8}$ multiplier for computing

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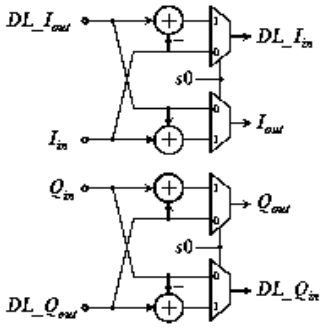

Figure 3. Architecture of PE3

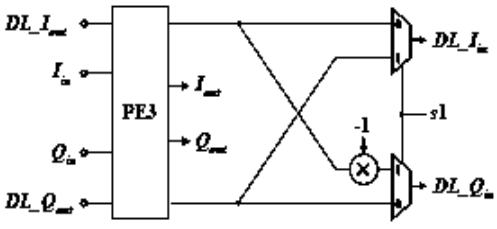

Figure 4. Architecture of PE2

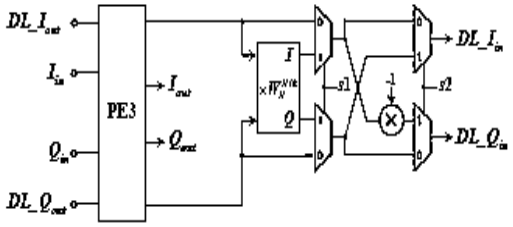

Figure 5.Architecture of PE1.

4. PROCESSING ELEMENT(PE3)

PE3 is the main component in FFT processor as it serves as the sub module for PE2 and PE1 stages. It processes the stage P=3 of the radix-2 8 point DIF FFT butterfly structure in Figure1. Hardware implementation of PE3 employs a ten transistor adder and a multiplexer.1-bit and 8-bit PE3 elements are presented in Figure. 6 and 7 respectively.

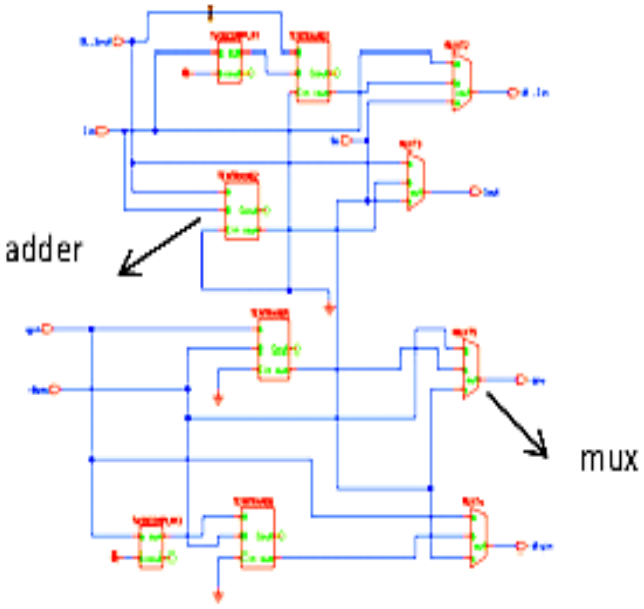

Figure 6.Schematic of 1-bit PE3.

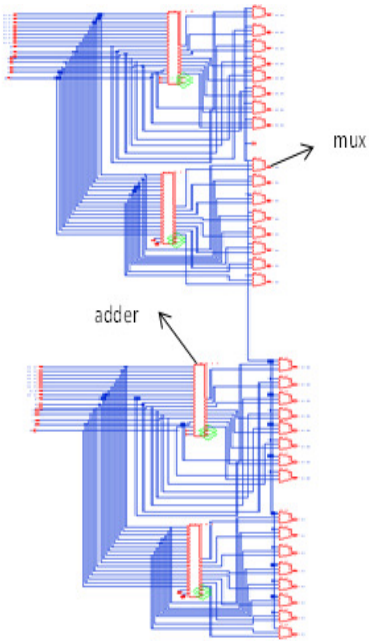

Figure 7.Schematic of 8-bit PE3.

5. RESULTS

PE3 element is simulated with ELDO software in Mentor Graphics. The simulated waveforms of 1-bit and 8-bit PE3 are shown in figure 8 and figure 9-10 respectively.

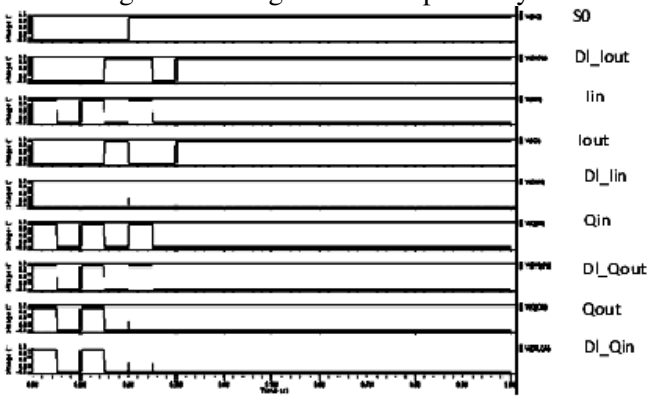

Figure 8. 1-bit PE3 simulated waveforms.

PE3 element processes the stage P=3 of theradix-2 DIF-FFT . It takes Input data (Iin) and Delay Output(DL_Iout) as the inputs and gives the Output data(Iout) and Input Delay to the next buffer(DL_Iin) based on the selection line of the multiplexer.

When S_0=0 DL_Iin = Iin (9)

Iout = DL_Iout (10)

S_0=1 DL_Iin = DL_Iout – Iin (11)

Iout = = DL_Iout + Iin. (12)

From Figure 8,

When So=0, Inputs are Iin= 1010 ; Dl_Iout=0001 then outputs are Dl_Iin=1010 ; Iout = 0001

When So=1, Inputs are Iin=1000 ; Dl_Iout=1011 then outputs are Dl_Iin=0011; Iout=0011

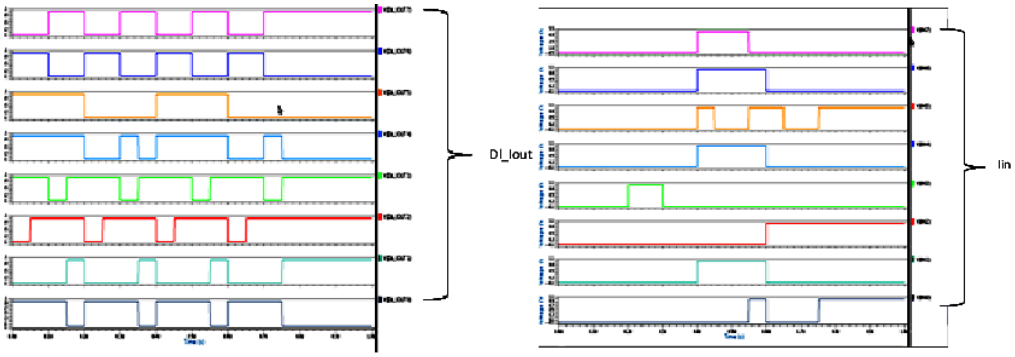

Figure 9Input waveforms of 8-bit PE3.

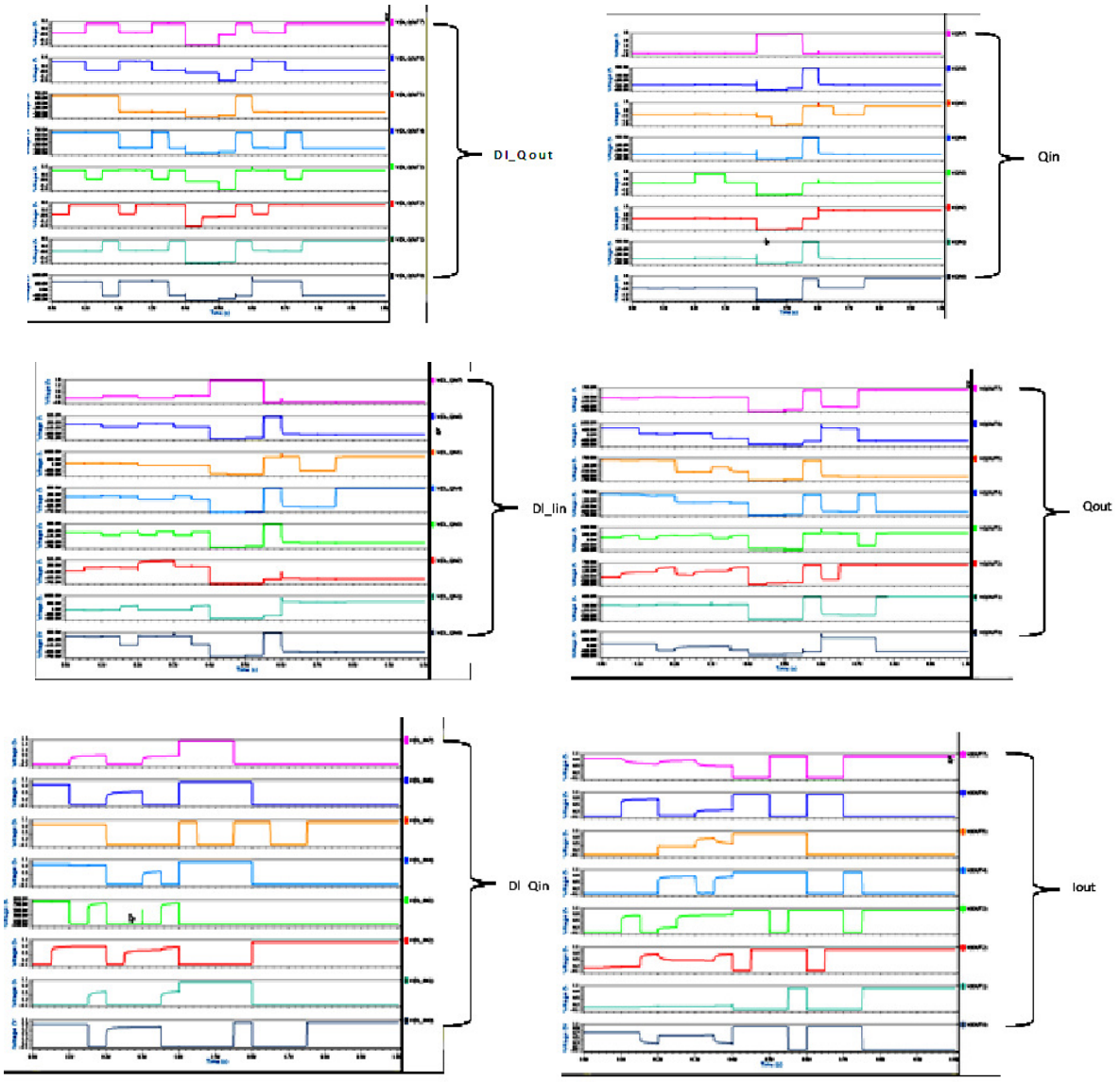

Figure 10 Output waveforms of 8-bit PE3.

The power dissipation (from the E-Z wave)of 1-bit PE3 is 0.5517 mwatts and for 8-bit PE3 it is 0.9237mwatts.

6. CONCLUSIONS

The pipelined FFT architecture contains three processing elements PE1, PE2, PE3. PE3 is the important element as it serves as a sub module to the other two processing elements PE2 and PE1.PE3 (1- bit and 8-bit) is implemented using Mentor Graphics tools and the power dissipation is observed. To implement the proposed pipelined architecture of FFT, PE2 and PE1 are to be further designed.

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IMPLEMENTATION OF LOW-COMPLEXITY REDUNDANT MULTIPLIER ARCHITECTURE FOR FINITE FIELD

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ABSTRACT

In the present work, a low-complexity Digit-Serial/parallel Multiplier over Finite Field is proposed. It is employed in applications like cryptography for data encryption and decryptionto deal with discrete mathematical andarithmetic structures. The proposedmultiplier utilizes a redundant representation because of their free squaring and modular reduction. The proposed 10-bit multiplier is simulated and synthesized using Xilinx VerilogHDL. It is evident from the simulation results that the multiplier has significantly low area and power when compared to the previous structures using the same representation.

KEYWORDS

Digit-Serial, Finite Field multiplication, Redundant Basis.

1. INTRODUCTION

In cryptography and coding theory, there are many applications using arithmetic operations for Finite Field [1]. In general, multiplication is extremely expensive in terms of time delay and physical area. Therefore, more focus is concentrated on designing high speed multipliers and on reduction of area [2]. The complexity mainly depends on representation of field elements. The most commonly used basisincludes polynomial (PB), normal (NB), dual (DB) and redundant (RB) [3]. Dual and normal basis multipliers require a conversion of basis, in which heavily rely on the simplifiedpolynomial. There is no need of conversion of basis in case of standard basis multipliers, the most commonly used multiplier is the polynomial basis multiplier due to their simple design and which also provide scalability.

Redundant basis (RB) is attractive when performing exponentiations and squaring operations [5]. The major advantage of redundant basis is squaring operation, as normal basis and also involves lower computational complexity. The multipliers of finite field are designed and classified into full parallel multipliers and word level multipliers [6]. The hardware used and power required by the bit-serial multipliers is less but it is slow.

Tounderstand the complication between area and speed, the Digit-Serial multipliers are reported previously. These are scalable multipliers and classified into different forms .An effective multipliers which utilizes RB is presented previously. Multipliers with systolic structures are presented in [7].A comb architectures are also presented formerly. Word level multipliers over finite field with high speed are also reported .And several other multipliers are also been developed for reducing complexity.

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In this paper, a low-complexity digit-serial/parallelis presented by utilizing a redundant basis over finite field (GF (2^m)).The recursive decomposition scheme for digit-serial/parallel multipliers is same as the previous, where the multiplier is modified. In his work, a low-complexity multiplier is introduced which involves significantly low area and power complexities when verified with the previous techniques.

Organization of the paper is as follows: Review of existing digit-serial RB multiplier is presented in section 2. Proposed digit-serial RB multiplier mentioned in section 3. Implementation and Comparison are shown in section 4. The paper ends with conclusion in section 5.

2. EXISTING DIGIT SERIAL RB MULTIPLIER

In Digit serial RB multiplier [4] the input operands A and B are divided into the number of integers to attain Digit Serial Multiplication, to achieve the final product the partial products are summed.

Assume x is an nth root of unity, components in Finite Field GF (2^m) are often described within the form:

$A=a_0+a_1x+a_2x^2+\cdots+a_{n-1}x^{n-1}$(1)Which a_i belongs to GF (2), for $0 \leq i \leq n-1$, alike the set {1, x, $x^2,\cdots, x^{n-1}$} is outlined as the RB for Finite Field components, wherever$n$ could be a positive number not below m.

And just then (m + 1) is prime and number 2 is a primitive root modulo (m + 1), for a finite field, there being a type I Optimal Normal Basis (ONB) [8].X is component of GF (2^m), &n= m+1
Let A, Bbelongs toGF (2^m) can be demonstrated in the form of RB:

$$A = \sum_{i=0}^{n-1} a_i x^i \quad (2)$$

$$B = \sum_{i=0}^{n-1} b_i x^i \quad (3)$$

Thus a_i ,$b_i$belongs to GF(2). , Let A and B are input operands which obtain product C, is demonstrated as follows

$$C = \text{A.B} = \sum_{i=0}^{n-1} \left(x^i b_i\right).A \quad (4)$$

$$= \sum_{i=0}^{n-1} \left(\sum_{j=0}^{n-1} b_i x^{(i+j)}\right) a_j \quad (5)$$

$$= \sum_{j=0}^{n-1} \left(\sum_{i=0}^{n-1} b_{(i-j)_n} x^i\right) a_j \quad (6)$$

$$= \sum_{i=0}^{n-1} \left(\sum_{j=0}^{n-1} b_{(i-j)_n} a_j\right) x^i \quad (7)$$

Where $(i - j)_n$ denotes modulo n reduction. Define $C = \sum_{i=0}^{n-1} c_i x^i$, where $c_i \in$ GF (2), we have [10].

$$c_i = \sum_{i=0}^{n-1} b_{(i-j)_n} a_j \quad (8)$$

3. PROPOSED DIGIT-SERIAL RB MULTIPLIER

In Digit serial RB multiplier [4], to attain Digit Serial Multiplication both the inputs are divided into a number of units and the partial products related to these units are summed to achievethe desired product.

Considering equations (1) and (7) of Digit serial RB Multiplier

Where $(i - j)_n$ denotes modulo *n* reduction. Define C in the form of:

$$\begin{bmatrix} c_0 \\ c_1 \\ \vdots \\ c_{n-1} \end{bmatrix} = \begin{bmatrix} b_0 & b_{n-1} & \cdots & b_1 \\ b_1 & b_0 & \cdots & b_2 \\ \vdots & \vdots & \ddots & \vdots \\ b_{n-1} & b_{n-2} & \cdots & b_0 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_{n-1} \end{bmatrix} \quad (9)$$

From (9), shifted form of the inputs bits B can be defined as follows

$$B^0 = \sum_{i=0}^{n-1} b_i^0 x^i = b_0 + b_1 x + \cdots + b_{n-1} x^{n-1} \quad (10)$$

$$B^1 = \sum_{i=0}^{n-1} b_i^1 x^i = b_{n-1} + b_0 x + \cdots + b_{n-2} x^{n-1} \quad (11)$$

$$\cdots\cdots\cdots$$

$$B^{n-1} = \sum_{i=0}^{n-1} b_i^{n-1} x^i = b_1 + b_2 x + \cdots + b_0 x^{n-1} \quad (12)$$

Where,

$$b_0^{i+1} = b_{n-1}^i$$
$$b_j^{i+1} = b_{j-1}^i, \text{ for } 1 \leq j \leq n-2. \quad (13)$$

The recursions on (13) can be extended further to have

$$b_j^{i+s} = \begin{cases} b_{n-s+j}^i, & for\ 0 \leq j \leq n-2 \\ b_{j-s}^i & other\ wise \end{cases} \quad (14)$$

Where $1 \leq s \leq n-1$, Let P and Q are two integers alike n = QP + r, where $0 \leq r \leq P$.for ease, assume that r = 0and divide the input of A into Q units of vectors operands A_u, where u= 0,1….Q-1follows:

$$A_0 = [a_0\, a_Q \cdots a_{n-Q}] \quad (15)$$

$$A_1 = [a_1 a_{Q+1} \cdots a_{n-Q+1}] \quad (16)$$

$$\cdots\ \cdots\ \cdots$$

$$A_{Q-1} = [a_{Q-1} a_{2Q-1} \cdots a_{n-1}] \quad (17)$$

Identically, we produce the Q units of shifted vector operandsB_u, where u= 0, 1, ⋯ ,Q -1, follows:

$B_0 = [\ B^0 B^Q \cdots B^{n-Q}\ ]$ (18)

$B_1 = [B^1 B^{Q+1} \cdots B^{n-Q+1}]$ (19)

… … …

$B_{Q-1} = [B^{Q-1}\ B^{2Q-1} \cdots B^{n-1}]$. (20)

The product $C = AB$ which is obtained from (9) are broken down intoproducts Q of vectors A_u and B_u, where u = 0, 1, ⋯ , Q-1 as:

$$C = AB = B_0 A_0^T + B_1 A_1^T + \cdots + B_{Q-1} A_{Q-1}^T$$

$$= \sum_{u=1}^{Q-1} B_u A_U^T = \sum_{u=0}^{Q-1} \overline{C}_u \quad (21)$$

Where $\overline{C_u}$ denotes

$$\overline{C_u} = B_u A_U^T \quad (22)$$

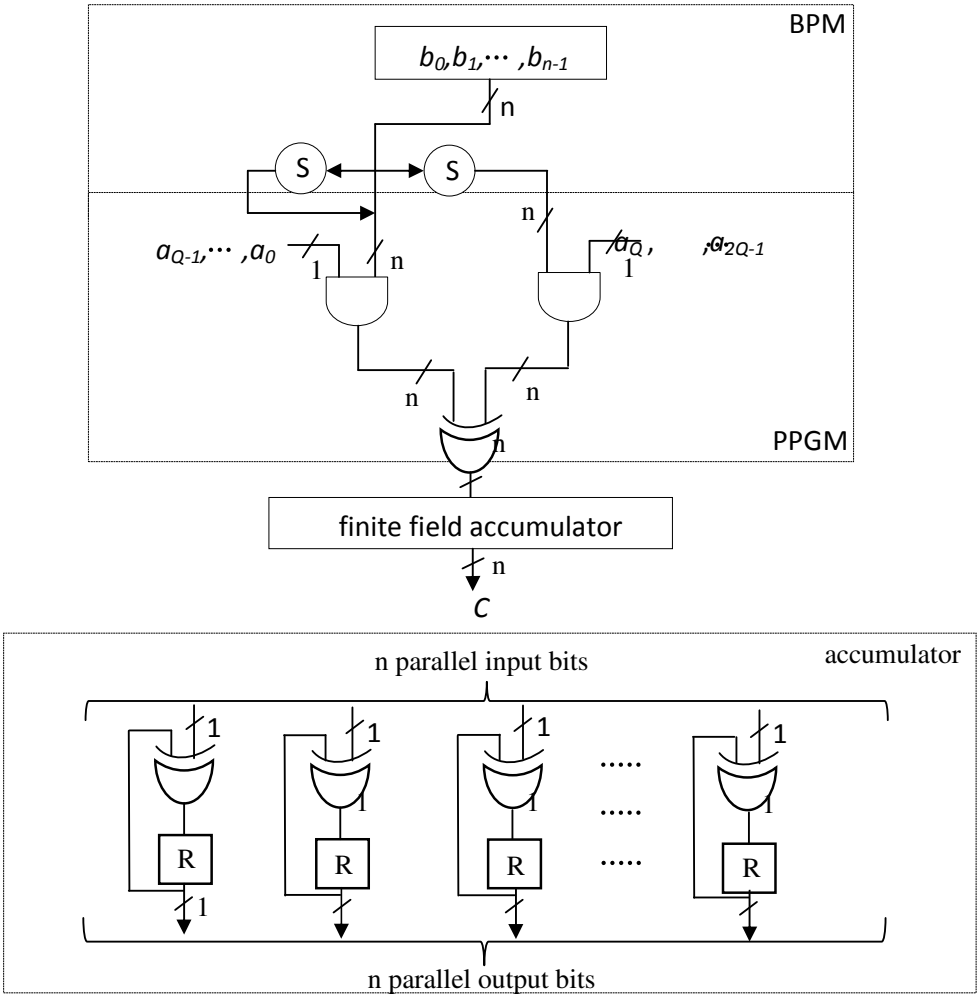
Note that A_u for u =0, 1, ⋯ , Q -1 is a P point bit – vector. B_u for u = 0, 1, ⋯ , Q – 1 is a P bit-shifted forms of operand B.

The proposed structure shown in below Fig.1 is derived from the processor space flow graph in [4], consists of S nodes, M nodes and A nodes which S node performs shifting operation and M node, A node performs multiplication and addition operation.

The proposed Digit- serial RB multiplier consists of three block, bit-permutation block, partial product generation block and finite field accumulator block. The BPB performs the rewriting of inputs of B to consume the output according the shifting S node. The PPGM consists of AND cell which performs the multiplication operation and XOR cell which performs addition operation.

And finite field accumulator blockconsistentwith n-bit parallel accumulation units. The recent input which is received is added with past accumulated result, and the sum is retain in the register cell and used in the next cycle. And successive output is obtained.Fig.2 shows the structure of finite field accumulator which consists of XOR cell and register cells with n parallel input bits and n parallel outputs bits.

In Fig.1 AND cell performs the multiplication of A input bits with the B input bits by bit-shifting form, XOR cell performs an addition operation of the outputs obtained from the ANDcells, the operation can be done concurrently and the partial products obtained at the XOR cell.



The partial products generated are fed to the finite field accumulator and result is accumulated and stored in register cell of the finite field accumulator and then finally the desired output is obtained. The partial products generatedin this multiplier are lesser in numbers than those previous multipliers, and also reduces the area complexities and reduce in power.

4. IMPLEMENTATION AND COMPARISON

The proposed digit-serial RB multiplier for 10-bit is coded using Verilog HDL in Xilinx ISE 12.2.The simulatedresults for the proposed structure are shown in Fig.3. In the above waveform the inputs are a and b and the output is c. when the 10-bit inputs a=0000000100 and b=0000000011 are given, by performing the shifting operation of the input operand b and multiplying with the each bit of the operand a, then each value is accumulated and stored inaccumulator to obtain the desired output c=00000000000000001100. And the remaining values shown are the signals.

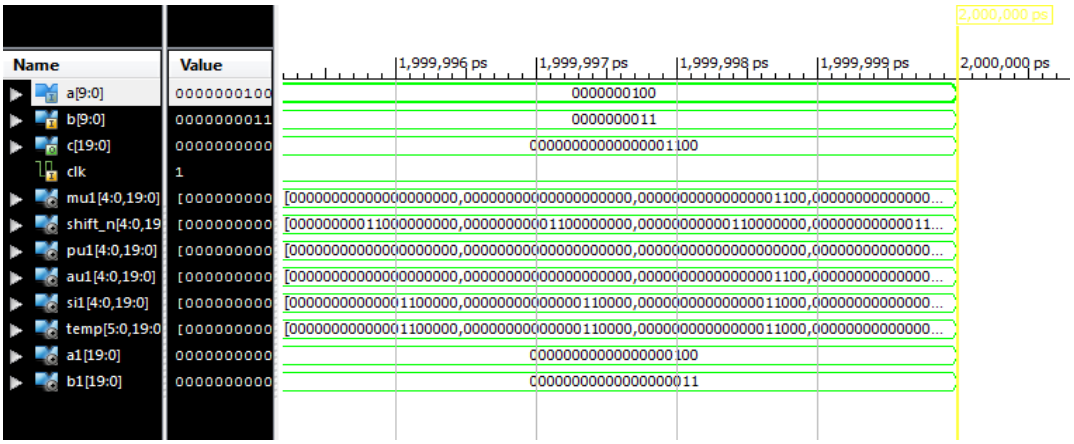


Figure 3. Simulation waveform of 10-Bit Proposed Digit-Serial RB multiplier

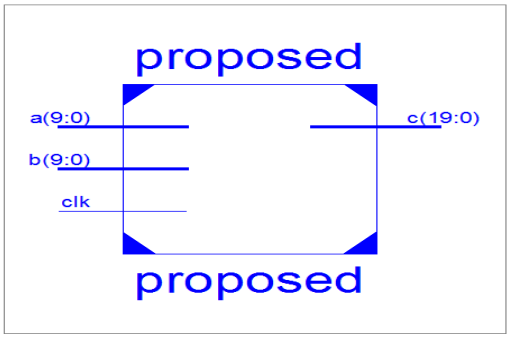


Figure 4. RTL Schematic of 10-Bit Proposed Digit Serial RB multiplier

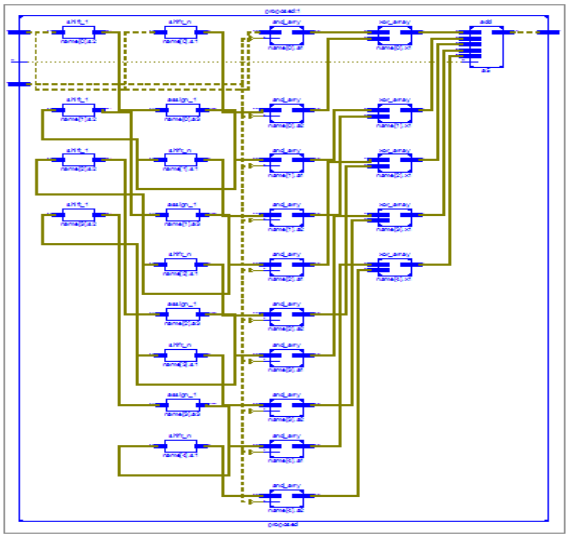


Figure 5. Detailed RTL Schematic of 10-Bit Proposed Digit-Serial RB multiplier

The RTL schematic of 10-bit Digit-Serial RB multiplier is shown in Fig.4,contain inputs a,b and clock and output c. Here a and b are the 10-bit inputs and which obtain the 20-bit output. The detailed view of 10-bit proposed digit-serial RB multiplier is in Fig.5, which gives the clear explanation of logic required.

Table 1.Comparison table

Structures	Area(Number of slices)	Power(W)
Structure-I [4]	75	0.066
Structure-II [4]	105	0.067
Proposed Structure	73	0.065

The 10-bit Structure-I, 10-bit structure-II [4] and 10-bit proposed digit-serial multiplier is implemented in Xilinx ISE .A table is formulated to show the results. The number of slices used in each structure is estimated and tabulated in table 1.This comparison table indicates the reduction in area .In similar manner; the power is also estimated and compared. The comparison result for number of slices that is area and power are also shown in fig.6 as a graphical plot for better comparison.

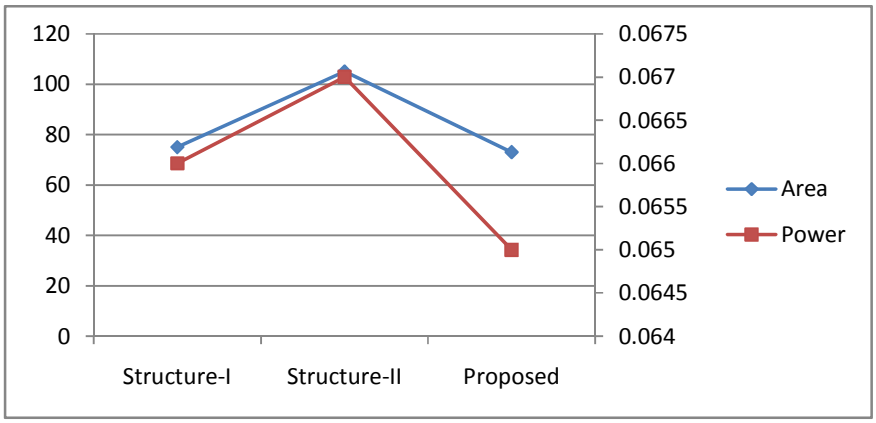


Figure 6. Area and Power comparison

5. CONCLUSION

The proposed 10-bit digit-serial RB multiplier is implemented. It is evident from comparison table that the performance of the proposed architecture is good with respect to speed and the area. Theproposed 10-bit digit-serial multiplier using redundant basis is used based on application requirement and mostly in modern cryptographic applications. The proposed multiplier is derived to obtain less complexity than the previous multipliers.

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ANALOGY FAULT MODEL FOR BIQUAD FILTER BY USING VECTORISATION METHOD

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ABSTRACT

In this paper a simple shortcoming model for a CMOS exchanged capacitor low pass channel is tried. The exchanged capacitor (SC) low pass channel circuit is modularized into practical macros. These useful macros incorporate OPAMP, switches and capacitors. The circuit is distinguished as flawed if the recurrence reaction of the exchange capacity does not meet the configuration detail. The sign stream chart (SFG) models of the considerable number of macros are investigated to get the broken exchange capacity of the circuit under test (CUT). A CMOS exchanged capacitor low pass channel for sign recipient applications is picked as a case to exhibit the testing of the simple shortcoming model. To find out error is to calculate EIGEN values and EIGEN vectors is to detect the error of each component and parameters

1. INTRODUCTION

Design of an analog circuit fault models is a challenging research problem, because of the long fault simulation time and unverified fault assumption. The major practical issues in developing an analog fault model include Zero noise margin, Nondeterministic transfer function, Too long fault simulation time and complex causal variations. Analog faults are of two types soft faults and hard faults. Parametric faults are due to change in the components of the parameter. Like resistor values and capacitance values .

A hard fault occurs due to short or opens wire. Most of the CMOS analog circuits are implemented by using switched capacitor (SC) circuits. SC circuits have the advantages of responses, good linearity wide dynamic ranges and accurate frequency .

Recently a static linear behaviour (SLB) analog fault model is proposed for linear and time invariant sampled SC circuits [1-2].Here consider a fixed z-domain transfer function. The SLB fault model covers not only parametric faults such as open loop gains of the OPAMP and capacitor ratios of the capacitors but also the catastrophic faults of the OPAMP, switches and capacitors of the CUT. This fault model deals with multiple faults when compare to the conventional fault model.

To minimizing the number of switches in a circuit the switch sharing technique is used and to improve the filter characteristics two methods are used dynamic range scaling and minimum capacitor scaling.

In this paper is organized as follows. Section 2 discusses the SFG's that are helpful in SLB fault model. Section 3 depicts the analysis that was made on the CUT, fault injections and their results are shown. Section 4. Depicts the switched capacitor common mode feedback circuit description and finally conclusion from obtained results in section 5.

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2. STATIC LINEAR BEHAVIOUR FAULT MODEL

The important parameters that effect the faultiness of the CUT are, OP-AMPS: For a given OPAMP, the open loop gain should have minimum specifications and the offsets have the largest specification.

Capacitors: Ratio of the capacitors to the corresponding feedback circuit capacitance in the CUT. Switches: Delayed switched capacitor branch and the delay free switched capacitor branch contain the switches has an additional fault.

The schematic circuit diagram for switched capacitor biquad filter is drawn as shown in Fig.1

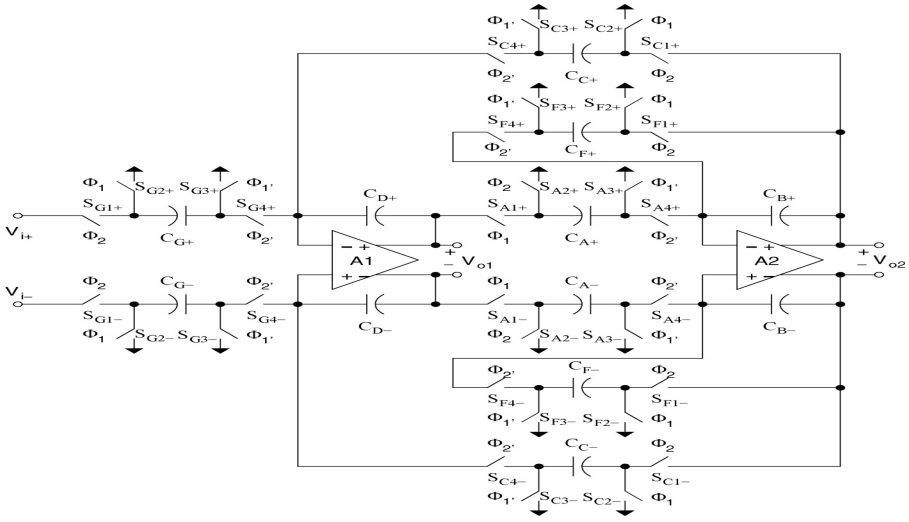

Fig.1 Schematic circuit of SC biquad filter

The specifications of the circuit are clock frequency of 6.144MHz andband pass from 0 to 20KHz, , stop band attenuation is higher than 40dB and pass band ripple is < 1dB the remaining specifications are summarized in Table .1

Parameter	Specification values
C_A	1.706 pF
C_B	3.293 pF
C_C	1.706pF
C_D	1pF
C_F	3.259pF
C_G	1.011pF
A1	80dB
A2	80dB

Table 1. Parameters of the switched capacitor circuit

The signal flow graph for the fully differential SC biquad filter of CUT is shown in Fig.2

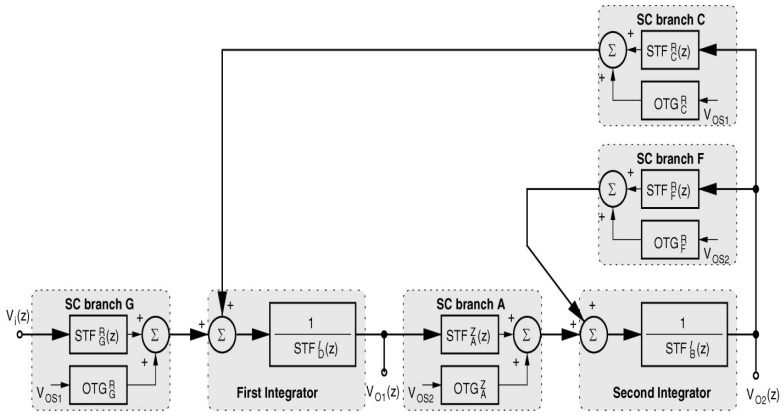

Fig.2 Signal flow graph of the CUT

By using this signal flow graph analysis calculate the overall input and output relationships of the circuit under test.

$$V_{02}(z) = STF_{R_2}(z)V_i(z) + OTG_{12}V_{os_1} + OTG_{12}V_{os_2} \qquad \cdots Eq(1)$$

Eq. (1) contains the signal transfer function (STF) and basic blocks of the SC biquad filter while the OTG's refer to the offset transfer gains of the corresponding stages the biquad. By considering Eq. (1) and SFG models, the design parameters of the STF of the biquad filter is

$$V_{02}(z) = (-(C_A/C_B).(C_C/C_D).Z^{-1}.V_i(z))/DEN(z) \qquad \cdots Eq(2)$$

Where the denominator term is expressed as:

$$DEN(z) = \left(1 + (C_F/C_B)\right) - (2 - (C_AC_C/C_BC_D) + C_F/C_B)Z^{-1} + Z^{-2} \qquad \cdots Eq(3)$$

Assuming that the fault free Op-Amps have zero offsets. There are different kind of faults can be injected in the biquad. As we seen from the Eq. (2) and Eq. (3) the faults in the CUT changes the values of the coefficients of the signal transfer function which alter nothing but the capacitor ratios. Hence it is important to maintain the capacitor ratio instead of the absolute capacitance values. Capacitors may introduce a parametric fault.

soft faults in Op-Amps include its OPG and input referred offset while the hard faults in Op-Amps are fatal due to its sensitivity in the design.. Faults due to switches are mostly same as in digital circuits i.e., stuck-at faults.

The fault free response of the CUT is simulated using MENTOR GRAPHICS tool with 0.35µm technology. The result is as shown in the Fig. 4. Here different simulated waveforms for different values of Op-Amp open loop gains. In this simulation obtain the outputs at both the output nodes in the two stage SC biquad filter.

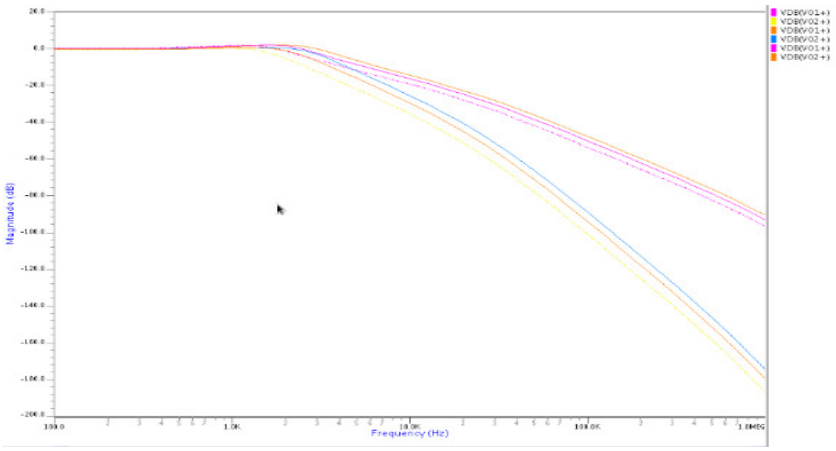

Fig. 3**.** Response of the Fault free CUT

As seen from Fig.3 outputs V_{O2} and V_{O1} illustrating outputs at first and second stages. Using EZ Wave tool in MENTOR GRAPHICS, compare the responses of the CUT for different Op-Amp open loop gains. This response can be used to verify the faultiness our CUT just by comparing the results of the faulty and fault free CUT's.

3. FAULT INJECTION TO THE CUT

Fig.4 depicts the schematic of the fault inject able Fleischer-Laker SC biquad. Like most of the analog circuit designs for IC, the CUT design is fully differential for better noise immunity and common mode interference rejection. The simulation was done on 0.35µm CMOS technology available in Mentor Graphics. Conventional folded cascode topology is used for implementing the Op-Amps. The design values of the capacitors in the fault injected CUT are given in Table 2

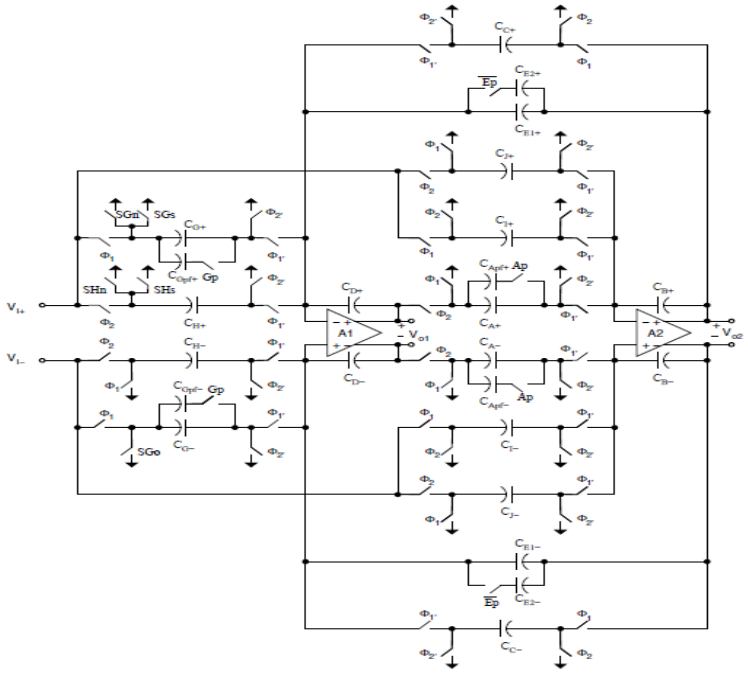

Fig. 4. Fault injected Schematic of SC biquad

SC biquad is used to realize a low-pass Butterworth filter whose band pass is 20 kHz with frequency of sampling 2.5 MHz and with stop band frequency of 400 kHz and stop band attenuation is 30dB .These are the design specification of this filter.

The SLB analog fault model covers both parametric and catastrophic faults. Parametric faults are the results of parameter deviations of components due to process, voltage, and temperature variations. Capacitance values deviations are typical parametric faults in SC circuits.

Hence, add two differential capacitor pairs C_{Apf} and C_{Gpf} to the biquad and decompose C_E into two capacitors C_{E1} and C_{E2}. By issuing the control signals Ap and Gp,. Similarly, activating the control signal Ep will reduce the effective capacitance of C_E by C_{E2} to model another kind of parametric fault. The capacitance values of these capacitors are listed in Table 2.

Parameters	Designated ratio	Absolute value (pF)
C_A	0.20289855 C_B	1.288
C_B	1 C_B	6.348
C_C	0.07246376 C_D	0.460
C_D	1 C_D	6.348
$C_E = C_{E1} + C_{E2}$	0.81159420 C_D	5.152
C_G	0.10144927 C_D	0.644
C_H	0.0289855 C_D	0.184
C_I	0.00362318 C_B	0.023
C_J	0.00724637 C_B	0.046

$C_{A_{pf}}$	0.4057971 C_B	2.576
C_{E1}	0.4057971 C_D	2.576
C_{E2}	0.4057971 C_D	2.576
$C_{C_{pf}}$	0.20289854 C_D	1.288

Table 2. Capacitor Ratios and Values of the CUT

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To verify the deductions of the SLB fault model about the catastrophic faults, add three switches including SGs, SHs, and SGo to the design. The aspect ratios of the switches SGs and SHs are designed to be much larger than those of the switches SGn and SHn which are in parallel with them.

By keeping SGs or SHs turn-on, a short fault is injected to the corresponding switch. The design allows injecting a stuck-open fault to the biquad, too. The switch SGo can be turn off for injecting the stuck-open fault.

4. FIFTH ORDER SWITCHED CAPACITOR LOW PASS FILTER

The schematic circuit diagram of fifth order SC low pass filter is shown in Fig.

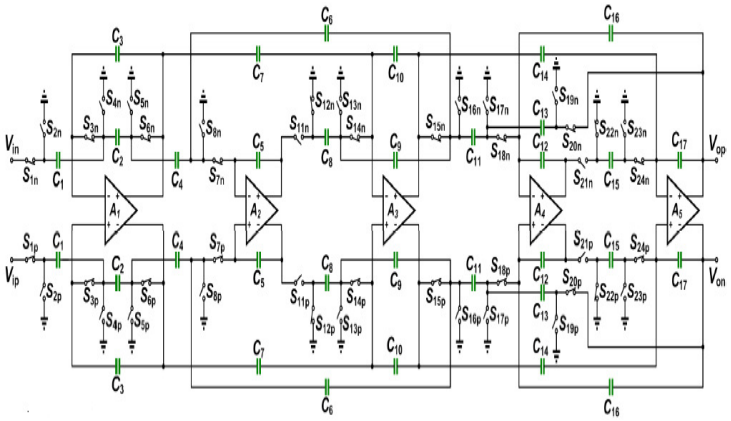

Fig.5 Schematic circuit of fifth order low pass filter

There are two approaches to design the SC low pass filter is cascade and ladder filter design. The cascade approach is done here. To design the higher order low pass filter, it consists of first and two second order circuits and the transfer function can be obtained from the second order continuous time low pass filter by using SFG analysis. The capacitance value of the capacitors of the circuit is listed in Table 3.

Table 3**.** Capacitor Values of the fifth order SC low pass filter

Capacitor (pF)	Dynamic range scaling	Minimum capacitor scaling
C_1	1.23	0.41
C_2	1.2	0.4
C_3	3.42	1.14
C_4	2.25	0.75
C_5	3.81	1.27
C_6	2.25	0.75
C_7	1.2	0.4
C_8	2.25	0.75
C_9	1.89	0.63
C_{10}	3.81	1.27
C_{11}	5.07	1.69
C_{12}	7.5	2.5
C_{13}	5.13	1.71
C_{14}	1.62	0.54
C_{15}	5.13	1.71
C_{16}	1.2	0.4
C_{17}	7.5	2.5
$C_{max/min}$		6.25

5 .VECTORISATION METHOD:

The minimum and maximum prin**cipl**e that the matrix Eigen values varies with the change of matrix elements. In this way the Eigen values of matrix *A* and the elements of the parametric fault set of CUT can be put one-to-one correspondence. So the proposed method is available to implement the faults diagnosis for analog circuits. The algebraic theory guarantees the correctness of this approach. The fault diagnosis procedure of the proposed method is described as follows.

Numbered the *n* components required for fault diagnosis from 1 to *n*.

$$\begin{bmatrix} A_{11} & A_{12} & \dots & A_{1n} \\ A_{21} & A_{22} & \dots & A_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ A_{n1} & A_{n2} & \dots & A_{nn} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_n \end{bmatrix}$$

Where as each row

$$w_i = A_{i1}v_1 + A_{i2}v_2 + \cdots + A_{in}v_n = \sum_{j=1}^{n} A_{ij}v_j$$

If it occurs that *v* and *w* are scalar multiples, that is if

$$Av = \lambda v,$$

then *v* is an **eigenvector** of the linear transformation *A* and the scale factor λ is the **eigenvalue** corresponding to that eigenvector. Equation (1) is the **eigenvalue equation** for the matrix *A*.

Equation (1) can be stated equivalently as

$$(A - \lambda I)v = 0,$$

Step-1: The output response signal of the actual is CUT stimulated by the same signal used in the simulation of software circuit is measured.

Step-2: According to the sample results, the output response matrix is generated, and the maximal and minimal eigenvalues (v_{max}andv_{min}) are calculated out.

Step-3: Assuming that $v_{max}$is produced by each fault cases, respectively, the potential parameter value $x_i$of the *i*t component is calculated out from

$$X_i=(v_{mxi}-b_{mxi})/k_{mxi}, 1 \le i \le n. \text{ ----------(1a)}$$

The potential minimal eigenvalue v_{mni}can be calculated out from the linear equation of Eigen matrix stated above and the above potential parameter $v_{mni}= k_{mni}\times (v_{max}-b_{mxi})k_{mxi}+ b_{mni}, 1 \le i \le n$.-------**(1b)**

Step-4: Now the error values are calculated out as *E*= [*e*1, *e*2, . . . ,*en*]. The element *ei* of *E* is calculated out as follows:

$$e_i= |v_{mni}- v_{min}|.$$

Fault diagnosis. Only one of the *n* assumptions in step 3)is correct, so only one of the *n* results obtained from (1b) in step 3) is closest the minimal Eigen value v_{min} obtained in step 1, i.e., the smallest element of *E* corresponds to the correct assumption. If the subscript of the smallest element of *E* is *m*, the CUT has fault when x_m obtained from (1a in step 3) exceeds the tolerance value of them component, and fault component is the component *m*

6. SIMULATED RESULTS

It is in general to employ a three tone test for the analog circuits. For this purpose, it is suggested to use a low frequency tone, a tone around corner frequency, and a high tone frequency close to the stop band frequency as a good combination for the three tone test. As per design specifications, select 22 kHz, 51 kHz, and 398 kHz as the stimulus tones. All the circuit simulations are done using Mentor Graphics and tanner 0.25µm technology EDA tools.

Fig.7 represents the schematic view of fifth order low pass filter. Fig. 8 shows the simulation results of the CUT when the parametric fault of C_{Cpf} is injected. This parametric fault makes the pass band gain and the stop band attenuation of the CUT out of the design specification. Even though the CUT fails in the test, the estimated TF still accurately Yet the estimated TFs successfully depicts the faulty frequency responses of the CUT.Fig.13 shows the frequency response of fifth order low pass filter ,from that the pass band frequency of 8MHz,pass band

ripple is <1dB, 80MHz clock frequency at the supply voltage of 1.8V and stop band attenuation is higher than 40dB ,

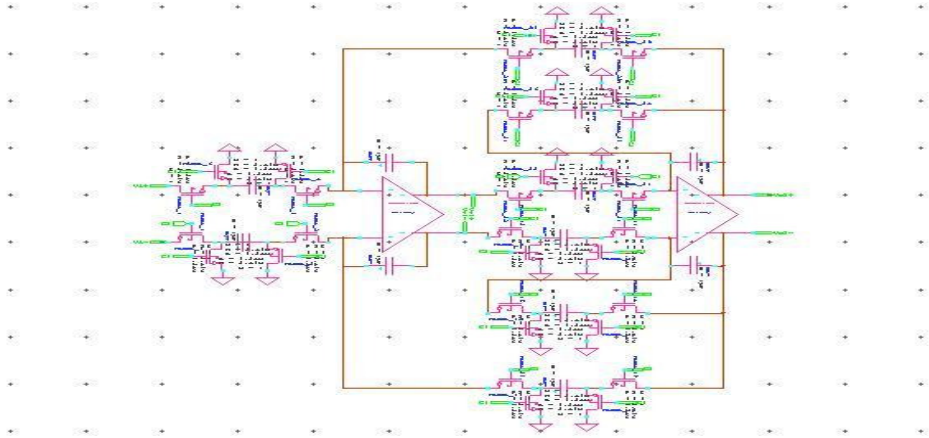

Fig 6: Biquad filter using second order low pass filter

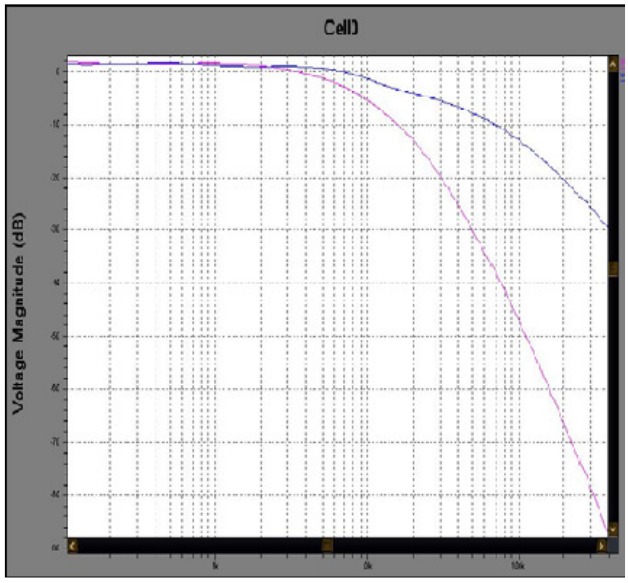

Fig 7:Frequency response of biquad filter in second order filter

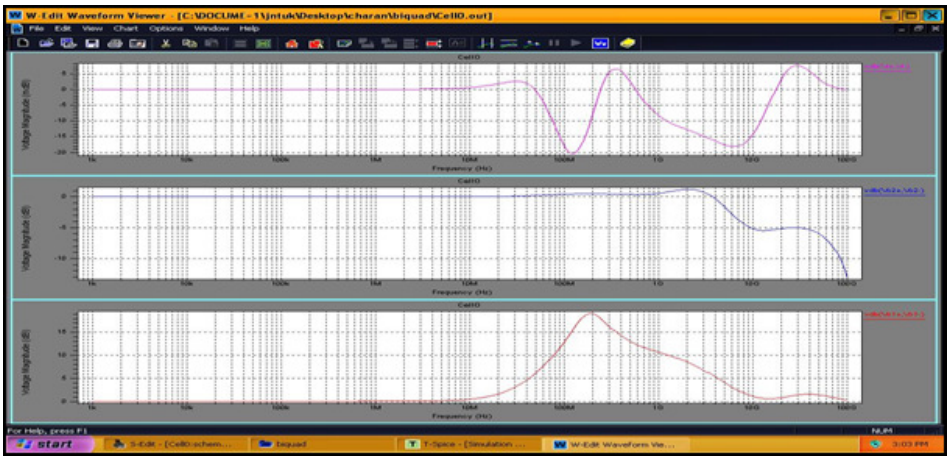

Fig8: Biquad filter output of without injecting any fault

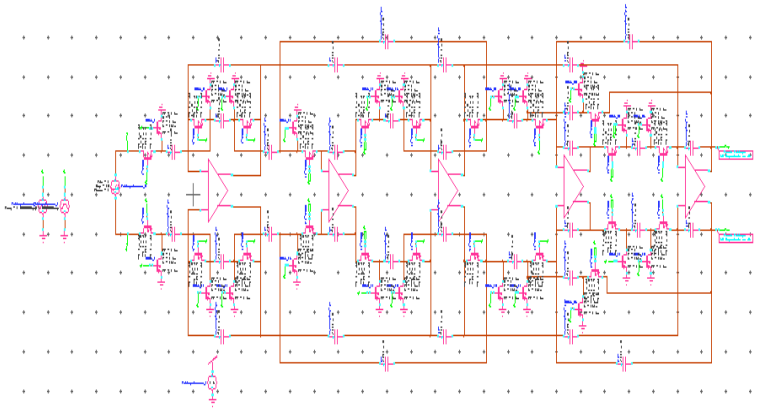

Fig 9**.** Schematic view of fifth order SC low pass filter

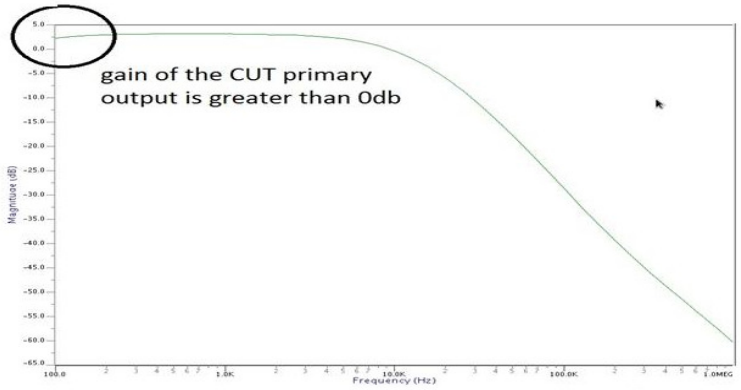

Fig 10**.** Experimental result after injecting parametric fault C_{Gpf}.

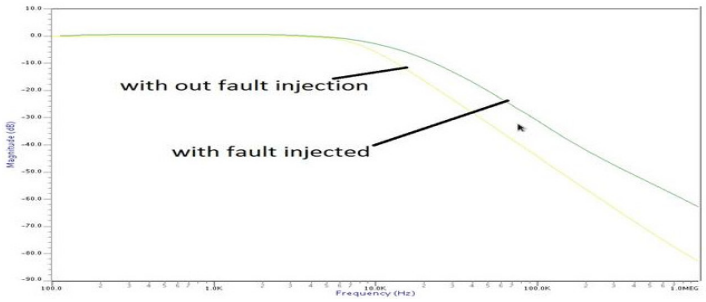

Fig 11. Experimental result after injecting parametric fault Ap

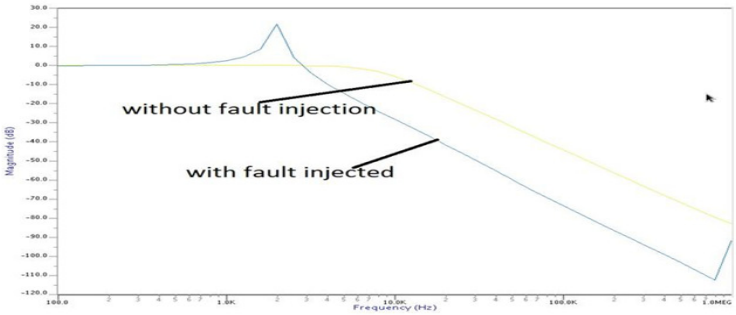

Fig 12. Experimental result after injecting parametric fault Ep.

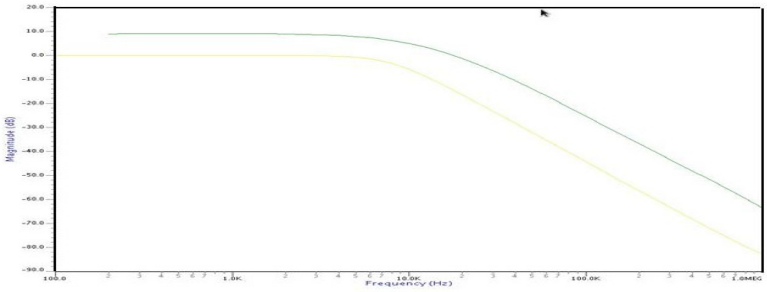

Fig 13. Experimental result when switch SHs is short.

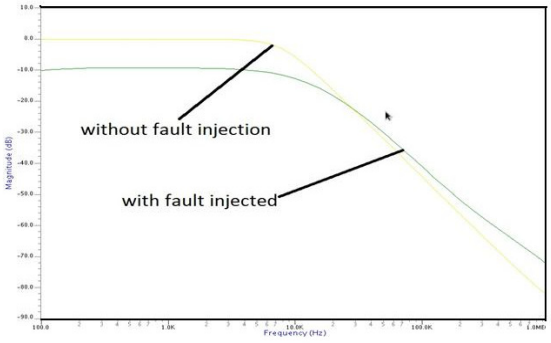

Fig 14**.** Experimental result when switch SGo is open

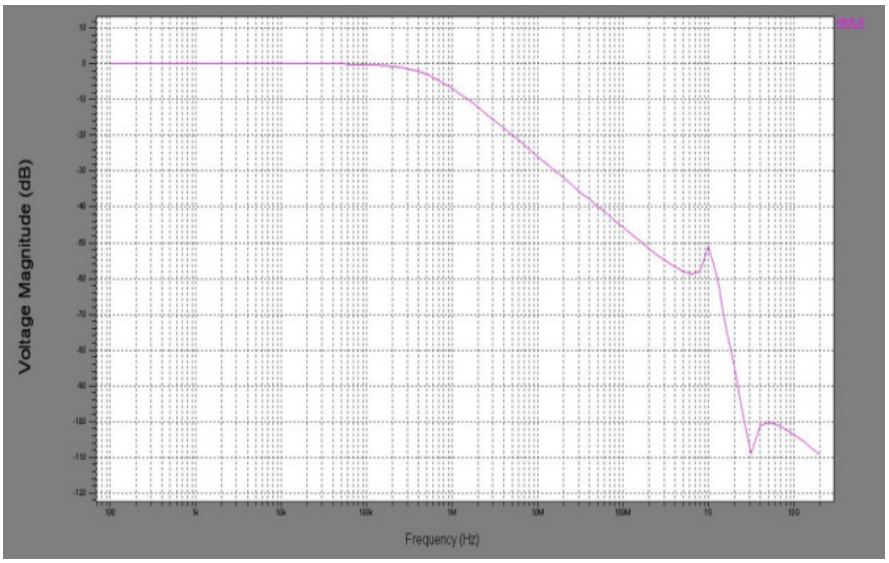

Fig 15 Frequency response of the SC low pass filter.

7. VECTORISATION METHOD RESULTS

faults	vmax vo1	Vo2	vmin Vo1	Vo2	Coefficients K, b
Capacitor enable	4.6	7.04	-80	-65	-523.906 525.0129
Capacitor ground	3.88	8.4	-70.2	-75	-711.4063 712.5129
Switches short(NMOS)	-104	3.88	-4	--70	-804.0562 805.1629
Switches open(NMOS)	-111	-0.8	-71.1	-1.6	-219.9063 218.7996

Fig.4 Faults table in eigenvectors

This result show the coefficients of eigen values of biquad filter circuit it can determine the in which component the can seen in this table

8. CONCLUSION

In this paper the SLB simple shortcoming model for straight SC circuits is been checked and a SC low pass biquad channel is taken as a case to show the adequacy of the SLB issue model. We lead with different stimulus tones and check if the test reactions fit in those anticipated by the recovered TF. Trial results check that the settled TF layout supposition holds for every one of the issues that we infused. Extending the shortcoming model to incorporate the planning related deficiencies would be a fascinating subject for the future exploration work.

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128-BIT AREA EFFICIENT RECONFIGURABLE CARRY SELECT ADDER

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ABSTRACT

Adders are one of the most critical arithmetic circuits in a system and their throughput affects the overall performance of the system. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. In this paper, we proposed an area-efficient carry select adder by sharing the common Boolean logic term. After logic optimization and sharing partial circuit, we only need one XOR gate and one inverter gate for sum generation. Through the multiplexer, we can select the final-sum only and for carry selection we need only one AND gate and one OR gate. Based on this modification 16-, 32-, 64-, and 128-bit CSLA architecture have been developed and compared with the conventional CSLA architecture. The proposed design greatly reduces the area compared to other CSLAs. From this improvement, the gate count of a 128-bit carry select adder can be reduced from 3320 to 1664. The proposed structure is implemented in Artix-7 FPGA. Compared with the proposed design, the conventional CSLA has 65.80% less area.

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KEYWORDS

,

Carry Select Adder, Area-Efficient

1. INTRODUCTION

Addition is the most common and often used arithmetic operation on digital signal processor microprocessor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. There are many binary adder architecture ideas to be implemented in such applications. However, it has been difficult to do well both in speed and in area. The easiest type of parallel adder to build is a ripple carry adder, which uses a chain of one-bit full adder to generate its output. The Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but lead to increase in area. The Carry Select Adder (CSLA) provides a compromise between small areas but longer delay Ripple Carry Adder (RCA) and a larger area with shorter delay Carry Look-Ahead Adder (CLA) [1].

In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers, power consumption is an important design constraint. Design of area- and power-efficient high-speed data path logic

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systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position [3]. Among various adders, the CSLA is intermediate regarding speed and area [2].

To add multiple inputs various types of Carry Propagate Adders (CPA) are present. Among them RCA design occupies the small area but takes longer computing time. The delay of RCA is linearly proportional to number of input bits. For some input signals carry has to ripple all the way from least significant bit (LSB) to most significant bit (MSB). The propagation delay of such a circuit is defined as the worst case delay over all possible input patterns also called as critical path delay. The Carry Skip Adder (CSKA) uses a carry skip scheme to reduce the additional time taken to propagate the carry signal in RCA. Thus, CSKA is faster than RCA at the expense of a few simple modifications. The CLA offers a way to eliminate the ripple effect. For every bit, sum and carry is independent of the previous bits. CLA is faster than RCA but consumes large area. CLA is fast for a design having less input bits, for higher number bits it shows the worse delay [5]. In RCA every full adder has to wait for the incoming carry before an outgoing carry is generated. The CSLA provide a way to get around this linear dependency is to anticipate both possible values of the carry input i.e. 0 and 1 and evaluate the result in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. The CSLA is intermediate between longer delay RCA and large area CLA.

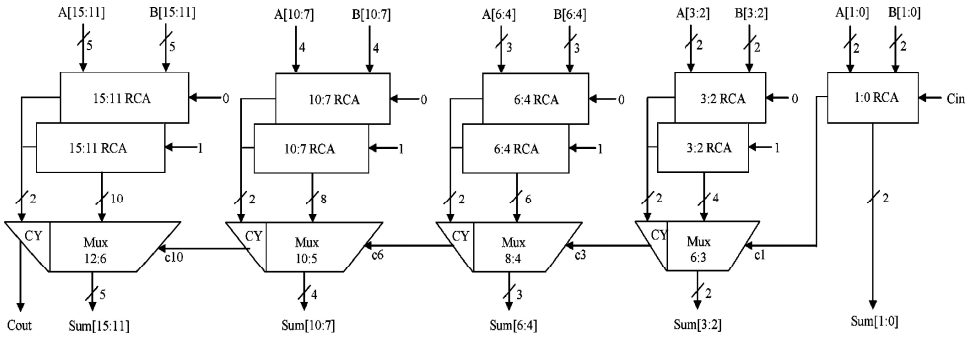

Fig. 1. 16-bit Conventional Carry Select Adder(CSLA

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin=0 and cin=1, then the final sum and carry are selected by the multiplexers (mux).

In this paper, we proposed an area-efficient carry select adder by sharing the common Boolean logic term. After Boolean simplification, we can remove the duplicated adder cells in the conventional carry select adder. Alternatively, we generate duplicate carry-out and sum signal in each single bit adder cell. By utilizing the multiplexer to select the correct output according to its previous carry-out signal, we can still preserve the original characteristics of the parallel

architecture in the conventional carry select adder. In this way, the circuit area and gate count can be greatly reduced and area delay product of the adder circuit can be also greatly lowered.

2. ARCHITECTURE OF CONVENTIONAL CSLA

A Carry Select Adder is a particular way to implement an adder, which is a logic element that computes the (n+1) bit sum of two n-bit numbers. The carry-select adder is simple but rather fast. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The architecture of conventional 16-bit carry select adder is shown in Fig. 1.

2.1 PROPOSED CARRY SELECT ADDER

TRUTH TABLE OF FULL ADDER

Cin	A	B	Carry	Sum
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

The truth table of single bit full adder is shown in Table 1. From the observation of truth table, the output of full adder sum is as carry-in signal is logic '0' is the inverse signal of itself as carry-in signal is logic '1'. The proposed logic formulation is given as

For c_{in}=0
Sum = A ^ B (1)
Carry = A&B (2)
For c_{in}=1
Sum = ~ (A ^ B) (3)
Carry = A|B (4)

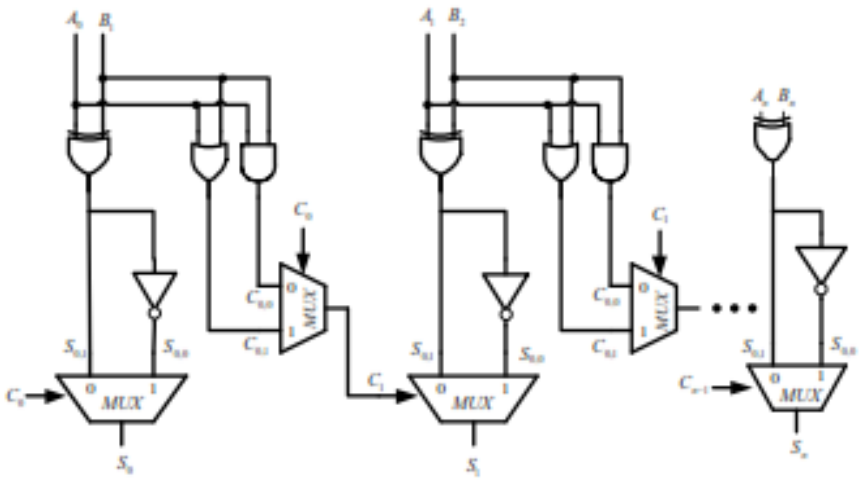

Fig. 2. The proposed adder.

The Eq. (1) and (3) are generates the sum for cin='0' and '1'. The Eq. (2) and (4) are generates the carry for cin='0' and '1'. The final sum is selects the multiplexer. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. In this way, we can keep both the summation generation circuit of XOR gate and INV gate and the carry-out generation circuit of OR gate and AND gate in parallel. Since we still retain part of parallel architecture of conventional carry select adder, we can still maintain some competitiveness in speed. On the other hand, we needn't to prepare the duplicated adder cells in the conventional carry select adder, which can greatly reduce the gate count and area delay product. The proposed area efficient adder is shown in Fig. 2. In this architecture carry selection multiplexer is replaced with one AND gate and one OR gate. The advantage of this replacement is reduce gate count and simple circuit.

3. COMPARISON and RESULTS

Theoretical Estimation of Area and Delay of 128-bit CSLA

THEORETICAL ESTIMATION OF AREA AND DELAY OF 128-BIT CSLA

Design	Delay (No. of Gate Delays)	Area (Gate count)
Conventional	49	3320
Proposed	385	1664

The Table II. Shows the theoretical estimation of area and delay of gate count. From this table area in terms gate count is greatly reduced from 3320 to 1664. Compared with the proposed design, the conventional CSLA has 99.51% excess area. The conventional carry select adder performs better in terms of speed. The delay of our proposed design increases because of logic circuit sharing sacrifices the length of parallel path. The delay difference existing between these two designs is mainly come from the length difference in their parallel paths. In the conventional carry select adder, it divided N bits into M blocks; however, our proposed design divided every single bit as individual block. In other words, we still retain N blocks in the N bits adder. Such arrangement will lead to some speed sacrifice.

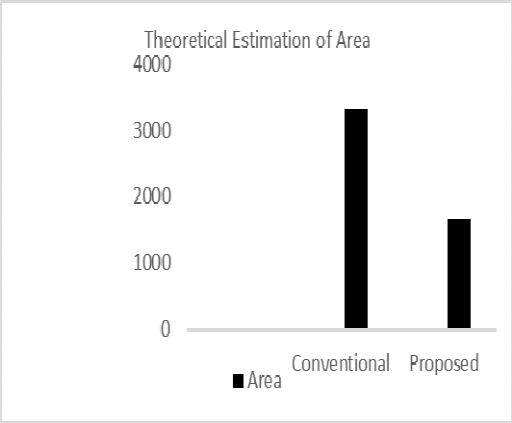

Fig. 3. The theoretical estimation of area for 128-bit CSLA.

3.1 FPGA Implementation

FPGA IMPLEMENTATION RESULTS

Design	Width(n)	Delay(ns)	Slices	SDP
conventional	16	5.902	26	153.45
	32	7.820	66	516.12
	64	11.922	138	1645.23
	128	28.17	320	9014.40
Proposed	16	6.467	24	155.20
	32	8.356	48	401.08
	64	16.134	96	1548.86
	128	45.009	193	8686.73

model to implement the proposed CSLA on the XILINX Artix 7 FPGA xc7a100t-3csg324 using the ISE Design Suite 14.5 platform. The proposed and conventional architectures are implemented 16-, 32-, 64-, and 128-bit wise. Compared with the proposed design, the conventional CSLA has 65.80% less area. The slice delay product (SDP) also less compared to conventional architecture. The implementation results in terms of logic slices and critical path latency are shown in Table III. It is obvious that our architecture has smaller hardware resource than the conventional architecture.

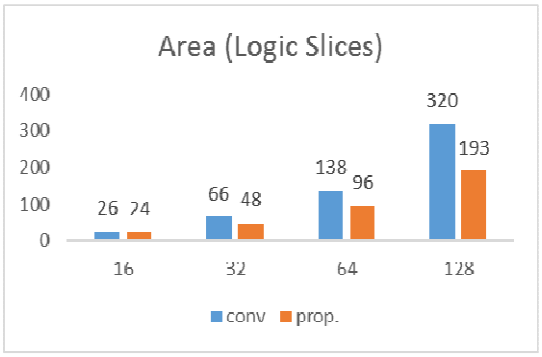

Fig. 4. Comparison of Area.

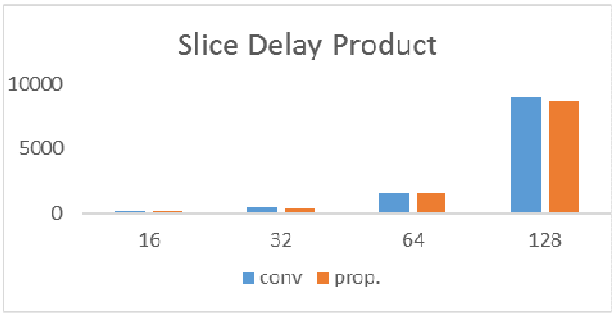

Fig. 5. Comparison of Slice Delay Product.

4. CONCLUSION

A simple approach is proposed in this paper to reduce the area of CSLA architecture. The proposed structure is implemented in Artix-7 FPGA. The proposed and conventional architectures are implemented 16-, 32-, 64-, and 128-bit wise. The reduced number of gates of this work offers the great advantage in the reduction of area, total power. From this improvement, the gate count of a 128-bit carry select adder can be reduced from 3320 to 1664. Compared with the proposed design, the conventional CSLA has 65.80% less area. The modified CSLA architecture is therefore, low area, simple and efficient for VLSI hardware implementation.

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ENHANCED OPTIMIZATION OF EDGE DETECTION FOR HIGH RESOLUTION IMAGES USING VERILOG HARDWARE DESCRIPTION LANGUAGE WITH LOW POWER CONSUMPTION AND LESS HARDWARE TECHNOLOGY

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ABSTRACT:

Edge Detection plays a crucial role in Image Processing and Segmentation where a set of algorithms aims to identify various portions of a digital image at which a sharpened image is observed in the output or more formally has discontinuities. The contour of Edge Detection also helps in Object Detection and Recognition. Image edges can be detected by using two attributes such as Gradient and Laplacian. In our Paper, we proposed a system which utilizes Canny and Sobel Operators for Edge Detection which is a Gradient First order derivative function for edge detection by using Verilog Hardware Description Language and in turn compared with the results of the previous paper in Matlab. The process of edge detection in Verilog significantly reduces the processing time and filters out unneeded information, while preserving the important structural properties of an image. This edge detection can be used to detect vehicles in Traffic Jam, Medical imaging system for analysing MRI, x-rays by using Xilinx ISE Design Suite 14.2.

KEYWORDS:

Sobel, Canny, Verilog, ISE Design Suite 14.2

1. INTRODUCTION:

Images are the Pictorial representation of an Object or a Person in a two dimensional format. If the labels of the co-ordinate functions (X, Y) represent the Intensity level or Gray level then the function "f", it represents the amplitude of the function of an image. And when those co-ordinate functions represent discrete values then that image can be represented as a Digital Image. That Digital image can be easily processed by many computer algorithms as a sub-category field in digital signal processing.

(a.) **(b.)**

Fig1 (a.) Represents the Image of a boy (b.) Represents Gray-Square of a Image

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The above figure (1) represents that each point of an original image has an 8-bit gray coded level and each pixel as a gray square.
There are no clear cut boundaries in the continuous series or a whole, no part of an image is noticeably different from different parts, although extremes of it are very different from each other for image processing at one end to the counter vision to the other. However, one useful paradigm is to consider three types of computerized processes in the continuum: Low-Mid & High level processes.

Low level processes involve primitive operations such as image pre-processing to reduce noise, contrast enhancement and image sharpening. Mid Level Processing of images involves tasks such as segmentation (Partitioning and Recognition) of individual objects. The output of the Mid-Level Processing is the attributes extracted from the image (e.g. Edges, Contours, and identity of individual objects). Finally, higher level processing involves making sense of an ensemble of recognized objects as in image analysis, at the far end of the continuum, performing the cognitive functions normally associated with the vision.

In the existing method, we preferred Mid-Level Processing for edge detection which has image as an input and the attribute of the image as output.

2. EDGE DETECTION:

Edges are the outlines of an image which serves as a boundary between background and the forefront part of an image. So Detection of edges plays a crucial role in image segmentation and object recognition. The main goal of our paper is to use different operators for edge detection and compare the results between them by looking at the less hardware technology and the power comparison between them under variety of conditions to determine which operator is useful or not.

The fundamental and most commonly used important task in image processing is Image Segmentation which determines the accuracy of the computational analysis which are determined by two primitive properties such as, image intensity values that is finding out the edges of an image and partitioning of image into different segments based on primitive factor such as thresholding, region growing and splitting.

As in the first Criteria, detection of discontinuities in a digital image, our basic approach leads to Edge detection instead of Point and Line Detection.

The two most serious errors in Edge Detections are anisotropic edge detection and wrong estimation of direction of the edges.

While optimizing the Edge Detection in Image Processing, Properties of the edges has to be considered where averaging filters suppresses structures with high wave numbers. Edge detection can be done by using three different techniques. Such as,

1. Gradient-Based Edge Detection
2. Edge Detection by Zero Crossings
3. Regularized Edge Detection

In our existing work, the main principle of Edge detection is done by using Regularized edge detection using two operators such as CANNY and SOBEL. Whereas, the other two techniques such as Gradient and Zero-Crossed Edge Detection technique has poor performance mostly in noisy images because of their small mask sizes. And as the high noise images had high wave numbers with greater mask size least performance would be achieved by using these two techniques.

Thus the regularized edge detection is used in high wave numbers to achieve maximum signal to noise ratio.

And also we need to derive some standard filters to perform a derivation in one direction and smoothening in all directions. Smoothing has no negative coefficients in higher dimensional signals as smoothening in all directions perpendicular to the gradient doesn't blur the image. The derivative filters used after the edge detection is called as the "**Regularized Edge Detective Filters**" and they provide estimating derivatives even from the ill-posed problems of discrete signals.

The Sobel operator is a discrete differential operator with smallest differences with odd number of coefficients averages the images in the direction perpendicular to the differentiation. It utilizes two 3*3 Matrices where one utilizes gradients in x-direction while the other utilizes gradients in y-directions.

-1	0	+1
-2	0	+2
-1	0	+1

Gx

+1	+2	+1
0	0	0
-1	-2	-1

Gy

Fig2. Sobel Operator using 3*3 matrices

The matrices here are multiplied with a 1/8 factor to get the right gradient value. Smoothing can be used after the Sobel operation to remove the noise after the edge detected image. The image is convolved finally with the two gradients horizontal and vertical and at each point the magnitude of the gradient can be approximated as

However it is faster to compute the magnitude of the Gradient with

$$G = /Gx/ + /Gy/$$

The Canny Edge Detector can be done by selecting the threshold either for thick or thinning edges. This operator is widely known as Optimum operator and it has three steps to implement the edge detection. Such as, first, a Gaussian filter to smooth the image and to remove the noise and the second is to compute the horizontal and vertical gradients (Gx) and (Gy) similar to the Sobel operator. And the third one is non-maximal suppression which is the algorithm to remove unwanted pixels in the image.

The first step in the canny operator is done by using hysteresis thresholding along the edges. The two types of hysteresis thresholding techniques are

1. Upper threshold (which selects the pixels as an edge having higher gradients)
2. Lower threshold (Which discards the pixels having higher gradients)

And if the pixel gradient is in between the two thresholding points then the pixel which has highest gradient than threshold will be selected as an edge of the image.

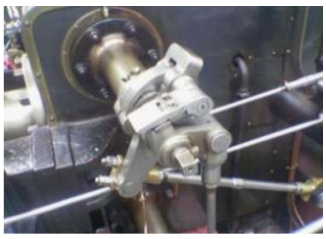


Fig3 (a.) Original Image, (b.) Edge detected image using Sobel operator

Table1. Comparison of Performances of Sobel and Canny Operators

S.No	Sobel Operator	Canny Operator
1	Algorithm is Simple and easy to operate within less time	Complexity in algorithm and takes large time response
2	Inaccurate and Sensitive to Noise	Utilizes Smoothing effect to remove noise
3	Good localization and response and immune to noise environment	Localization will be compromised for higher wave numbers

3. PROPOSED WORK

In the Proposed work, the complexity of programming the algorithmic steps of Sobel and Canny operators using Matlab is resolved by implemented the edge detection using Verilog Programming language. Thus Complexity in algorithm is greatly reduced which in turn reduces the cost and complexity of the system with less optimized power.

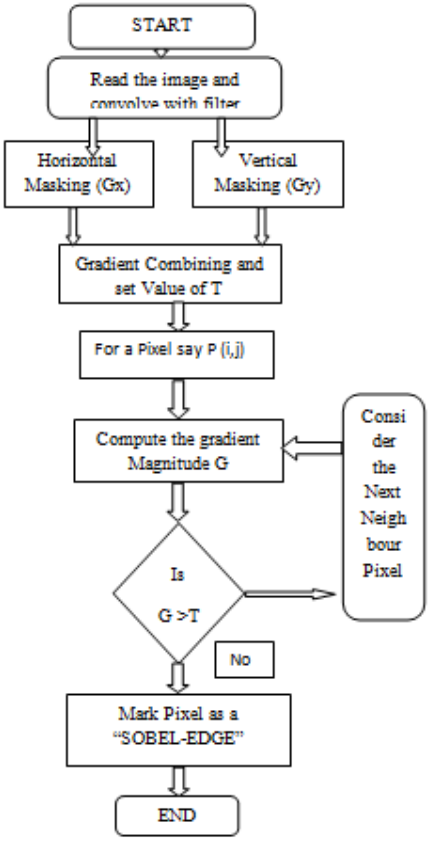
In the Sobel operator, the horizontal and vertical masking is used to calculate the horizontal and vertical gradients (Horizontal and Vertical edges of the image). And then we calculate the overall gradient by using the overall square root for the summation of the square of both the horizontal and vertical gradients (Gx and Gy).

Steps for Sobel operator:

1. Read the Pixels of the image and convolve with the filter.
2. After Horizontal and vertical masking is done separately find out the Overall Gradient of the image.

3. Then Consider the First Pixel, Let's say "P"
4. For "P", If G is greater than "T" then move to next Pixel otherwise mark the Pixel as an Edge.
5. Continue the process for overall gradients of all the pixels.

The Flow Chart for Sobel Operator is shown below:



Sobel Edge detector is compromised in such a way to use a Smoothing filter to increase the noise immunity under certain conditions but it hurts the localization factor.

The implementation of Sobel Edge detection algorithm is as follows; Consider we have the image G(c, r), Then Gx is given by

$$Gx= [G(c+1, r-1) +2*G(c+1, r) +G(c+1, r+1)-G(c-1, r+1)-G(c-1, r)-G(c-1, r-1)];$$

Also Gy is given by

$$Gy= [G(c-1, r-1) +G(c, r-1) +G(c+1, r-1)-G(c-1, r+1)-2*G(c, r+1)-G(c+1, r+1)];$$

Once you have the Gx and Gy its sum is calculated to obtain the gradient magnitude and is compared with the threshold value. If the compared value is higher than threshold then the pixel is replaced by a one otherwise with a zero. The same is done with all the pixels of the image to find the edges.

Using Canny Operator:

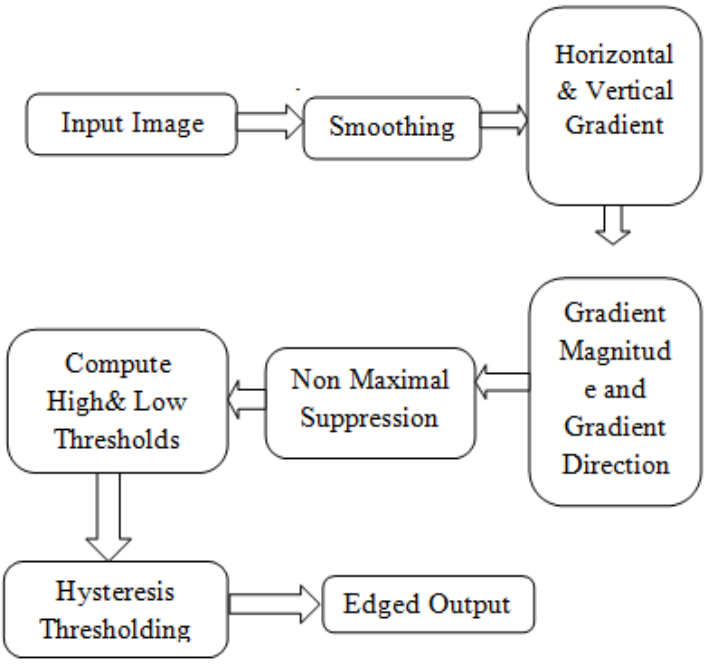
Canny operator is the best optimal operator which uses three architecture types such as:

1. Low error rate (i.e. no edges has to be missed and no non-edges has to be considered)
2. Edge points must be confined with less distance among them
3. Only one reaction to a single edge.

In the Canny operator, Smoothing is computed first and then the gradients are calculated individually with highest masks. The one with the least will be marked as zero otherwise it is set as one. Hence it has higher immunity to Gaussian noise than Sobel and other operators.

In this operator the gradient arrays are removed by using Hysteresis. The one with highest hysteresis will mask as one otherwise the pixel is masked as zero. If the gradient mask is in between the two verges then also it is masked as zero (i.e. Non-edge)

Block diagram of Canny Operator:



The Canny Edge Detection Algorithm:

Step1:

Smooth the image with two Gaussian Operators for both horizontal and vertical gradients and remove the noise part in the image.

Step2:

Consider the Horizontal and Vertical gradients of the image along x and y axes.

Step3:

If there exists an error, in the complete resultant gradient then it is set to either 0 or 90 degrees. This can be done by setting y-axis to 0 or complete x-axis to 0 by using the formula shown below:

Is set to 0 if denominator is 0 otherwise it is set to 90 degrees.

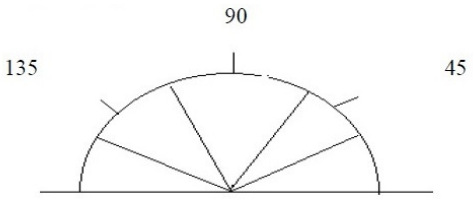
Step4:

Once the edge direction is recognized, the coming step is to agnate the edge direction to a direction that can be marked in an image. So if the pixels of a 5x5 image are arranged as follows

x xxxx
x xxxx
x x a x x
x xxxx
x xxxx

It can be seen by looking at pixel "a", there are only four possible directions when describing the surrounding pixels - 0 degrees (in the horizontal direction), 45 degrees (adjacent the actual diagonal), 90 degrees (in the vertical direction), or 135 degrees (adjacent the negative diagonal).

So now the edge position has to be adjudicate into one of these four directions depending on which direction it is closest to (e.g. if the orientation angle is found to be 3 degrees, adjust it zero degrees). Think of this as taking a semicircle and dividing it into 5 regions.



Therefore, any edge direction falling within the range (0 to 22.5 & 157.5 to 180 degrees) is set to 0 degrees. Any edge direction lies in the range (22.5 to 67.5 degrees) is equal to 45 degrees. Any edge direction lies in the range (67.5 to 112.5 degrees) is equal to 90 degrees. And lastly, any edge direction lies within the range (112.5 to 157.5 degrees) is set to 135 degrees

Step5:

Suppress the non-edges and give a thin line to the edges.

Step6:

Hysteresis thresholding is used to eliminate streaking. It makes use of both a high threshold and a low verge. If a pixel has a value above the high verge, it is equal to an edge pixel. If a pixel has a value above the low threshold and is the neighbour of an edge pixel, it is equal to an edge pixel as well. If a pixel has a value above the low verge but is not the neighbour of an edge pixel, it is not equal to an edge pixel. If a pixel has a value below the low verge, it is never equal to an edge pixel.

Canny local operator gives Smoothing to the noisy images and also supports localization but consumes more time because of its complex algorithm.

Implementation of Verilog for any operator

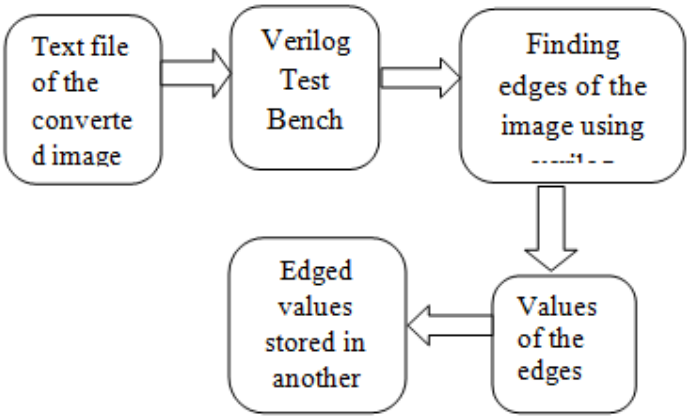


Fig 4. Block Diagram for Any Operator In Verilog.

4. RESULTS:

Canny operator:

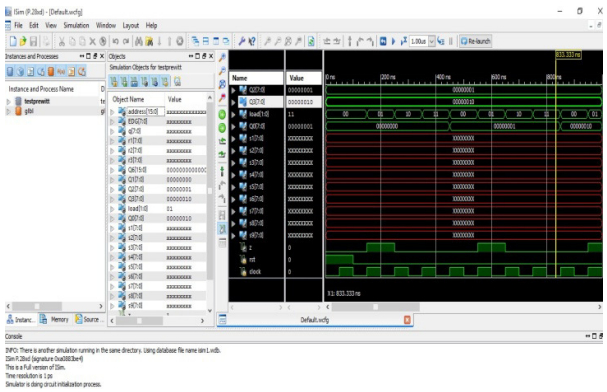


Fig5. Timing Diagram of Canny Operator

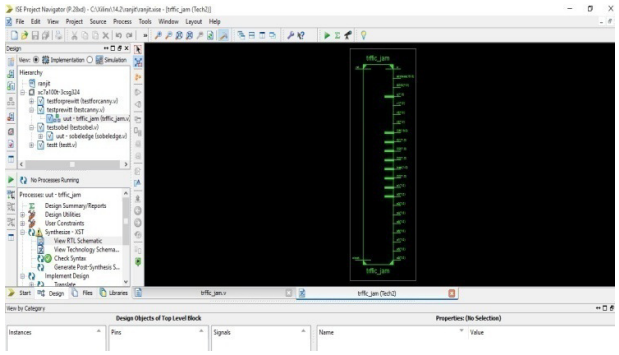


Fig6. RTL Schematic of Canny operator

Logic utilization	Used	Available	Utilization
Number of Slice Registers	11443	149760	7%
Number of Slice LUTs	26223	149760	17%
Number of fully used LUT-FF pairs	3440	34226	10%
Number of bonded IOBs	23	680	3%

Fig7. Device utilization summary of canny operator (previous work)

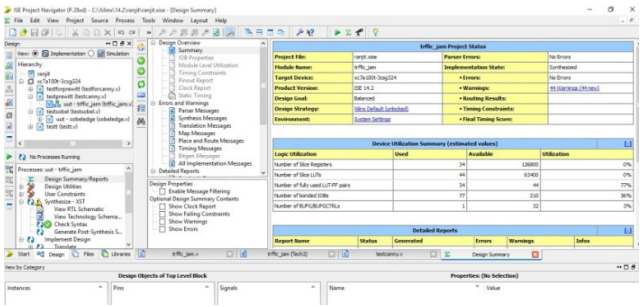


Fig8. Device Utilization summary of canny operator (Proposed work)

From the above figure 6 represents the timing waveforms, figure 7 represents the RTL schematic diagram,

Figure 8 represents device utilization summary of canny operator in previous work figure 9 represents device utilization summary of our present work, when compared to the previous work number of slice registers, slice LUTs, LUT flip flop pairs used are decreases, hence our system is better than the previous one.

Sobel Operator:

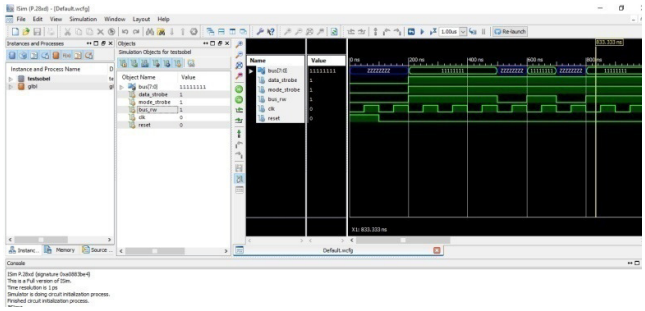


Fig9. Timing Waveform of Sobel operator

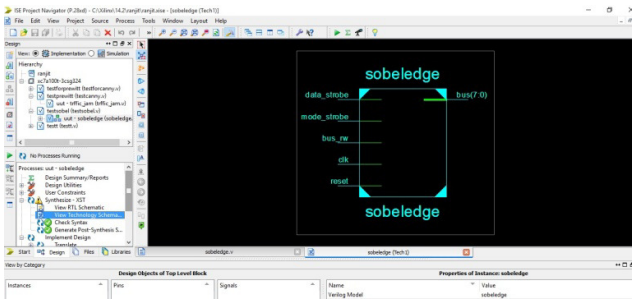


Fig10. RTL Schematic Diagram of Sobel Operator

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2890	3584	80%
Number of Slice Flip Flops	845	7168	11%
Number of 4 input LUTs	4989	7168	69%
Number of bonded IOBs	22	97	22%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Wed Apr 29 10:49:48 2009	0	3 Warnings (3 new, 0 filtered)	5 Infos (5 new, 0 filtered)
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

Fig11. Device utilization summary of Sobel operator (Existing work)

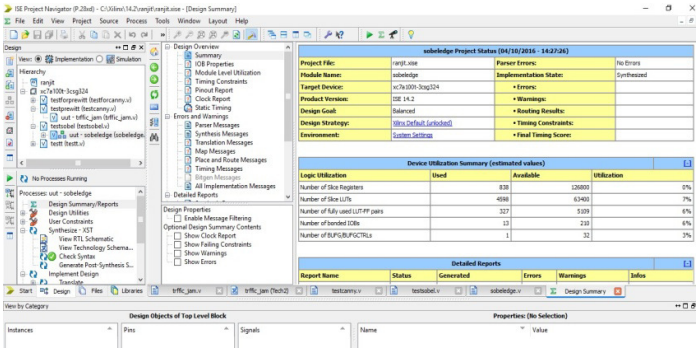


Fig12. Device utilization summary of Sobel operator (Proposed work)

From the above figure 10 represents the timing waveforms, figure 11 represents the RTL schematic diagram, figure 12 represents the design utilization summary of Sobel operator.

Figure 12 represents device utilization summary of Sobel operator in previous work figure 13 represents device utilization summary of our present work, when compared to the previous work number of slice registers, slice LUTs, LUT flip flop pairs used are decreases, hence our system is better than the previous one.

5. CONCLUSION AND FUTURE SCOPE

In our paper, edge detection is done by using three techniques using Verilog module. They are Sobel, canny and prewitt. By using these techniques high end images can also be edge detected in desired fashion by taking Pixel intensity and separate quantization levels. This procedure is very easy when compared to the other modules implemented using mat lab and vhdl and requires less number of flip-flops, logic gates with low power consumption.

Future scope:

This paper can be implemented on FPGA and CPLD kits and high end images can be edge detected and viewed by using different display devices, which could be a most powerful tool in image processing and visualization techniques.

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