A SURVEY ON MACHINE LEARNING APPLICATIONS IN VLSI CAD

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ABSTRACT

The incorporation of machine learning (ML) methodologies into VLSI computer-aided design (CAD) procedures is gaining prominence owing to its capacity to enhance design efficiency, forecast performance, and diminish time-tomarket. This literature overview examines the advanced machine learning techniques used at many phases of VLSI design. This review synthesizes data from current research articles, emphasizing the strengths, limits, and prospective avenues for machine learning implementations in VLSI CAD.

KEYWORDS

Machine Learning; Very Large Scale Integration; Integrated circuit; Computer-Aided Design;

1. INTRODUCTION

In the past, the development of VLSI has been primarily dependent on human expertise and rule-based computational tools. However, the complexity and size of contemporary integrated circuits necessitate sophisticated methodologies. Machine learning is a viable solution because it employs vast data sets to train models that can predict outcomes, enhance designs, and simplify numerous components of the VLSI design process.

It is becoming increasingly important to incorporate machine learning (ML) methodologies into VLSI computer-aided design (CAD) procedures in order to enhance design efficacy, forecast efficiency, and reduce time-to-market. This literature review assesses the implementation of sophisticated machine learning methodologies during critical phases of VLSI design. This article provides a concise summary of the advantages, challenges, and prospective future of artificial intelligence in VLSI CAD, as well as data from previous studies.

Power consumption significantly influences the efficacy, performance, and overall expense of VLSI circuits, underscoring its critical role in design considerations. Conventional power evaluation procedures may be inaccurate and time-consuming, which can lead to subpar designs. Conversely, machine learning has emerged as a reliable instrument for forecasting the power consumption of future circuits by analysing historical data. Throughout the design process, from synthesizing to post-layout validation, machine learning approaches provide precise power projections. Machine learning methodologies enhance efficiency and accuracy when contrasted with conventional methodologies. This section investigates the specific attributes of various machine learning algorithms, their capacity to predict the future, and their efficacy in enhancing power estimations in VLSI CAD.

1.1. Power Estimation Techniques in VLSI Design

Diana et al. [16] utilized information theory in "Information Theoretic Measures for Power Analysis in VLSI CMOS" to estimate VLSI power consumption. The basic principle is to use average entropy or informational energy to calculate circuit switching frequency. More entropy indicates more frequent signal transmission modifications. Contrarily, informational energy measures average signal transition power utilization.

Farid N. Najm's et al. [7] addressed the challenge of estimating multi-output combinational logic circuit size and power consumption using Boolean equations. The model estimates the area of the multi-output Boolean function after converting it to a single-output format. Power use evaluation requires circuit size and average output estimation. The study describes a gate count-based capacitance estimation method employing several gate types and capacitance values. The authors test their models on many benchmark circuits to prove they accurately estimate circuit size and power usage.

Pedram et al. [3] underlined power's relevance in VLSI system design and the challenges of predicting and forecasting power use at high abstraction levels. The study compares gate-, transistor-, and architectural level power modelling methods. Models at the gate level are precise but need lots of processing power. Transistor-level models balance accuracy and computational efficiency, whereas architectural-level models are helpful but less realistic due to their high abstraction level. Static and dynamic modelling approaches exist. Dynamic approaches mimic the circuit to forecast power consumption more accurately than static ones. Architectural approaches improve designs by selecting data paths and memory layouts. By choosing transistor sizes or controlling switching, circuit-level methods increase power efficiency. The paper thoroughly discusses power modelling concerns and methods in VLSI design at different abstraction levels.

Eiermann M. et al. [4] offered a basic switching activity-based model for assessing circuit switching activity. The model evaluates switching activity using the Hamming distance between input vectors. The individual switching activity-based model allows for hamming distance and combines input switching pattern differences to improve this method. Although it takes more characterization data, the individual switching activity-based model forecasts electricity use more accurately.

Bogliolo A et al. [5] provided a framework for RTL power model generation and optimization. The work emphasizes the need for precise and practical functional macro power consumption models in RTL power calculations. Building experts must automate these models and ensure they provide accurate average power estimates. We use linear regression and nonparametric expansions to correctly characterize power dissipation's dependency on input and output activity levels.

Luca Benini and his team [9] discussed the advancements in logic synthesis that can reduce the power consumption of digital circuitry. Among their methods to reduce power consumption are gate-level and register-transfer-level restructuring, low-power silicon technologies, and technology-dependent circuit optimization. The work emphasizes the following points: These methodologies underscore the comprehensive strategy articulated in this work to address power consumption challenges with advanced logic synthesis methods.

- Gate resizing involves reducing the size of non-essential gates to lower their capacitance and subsequent power consumption.
- Retiming involves altering the circuit's logic to slow down critical paths, thereby reducing switching activity and power consumption.

- Activity-based optimization involves identifying and enhancing circuit elements that frequently switch to reduce energy consumption.
- Low-power design methodologies involve the utilization of power-efficient techniques such as gated clocks and domino logic to enhance overall power efficiency.

Farid N. Najm et al. conducted an extensive examination of VLSI circuit power estimation methods [2]. The paper begins by discussing power estimation in VLSI design and its challenges. It then examines VLSI circuit power dissipation and power estimation methods. The research divides power estimation into statistical and analytical techniques. In accordance with circuit characteristics, analytical methods determine power dissipation using mathematical models. Conversely, statistical methods quantify circuit switching activity to measure power dissipation. This work examines numerous statistical power estimation approaches, including Monte Carlo simulation and statistical modelling, where several random input combinations are created to represent circuit power dissipation and forecasting power dissipation using statistical models of circuit switching activity, respectively. This work covers analytical and statistical methods for estimating VLSI circuit power consumption.

Duong Tran et al. [8] suggested measuring digital CMOS VLSI chip power consumption. It divides the chip into logic circuitry, on-chip memory, connectivity, clock distribution, and off-chip drivers. Each component's power consumption is calculated independently and combined to determine the chip's power consumption. Discrepancies in circuit design make behavioural power estimations challenging to predict, especially the power dissipation of individual gates at the Register Transfer Level (RTL).

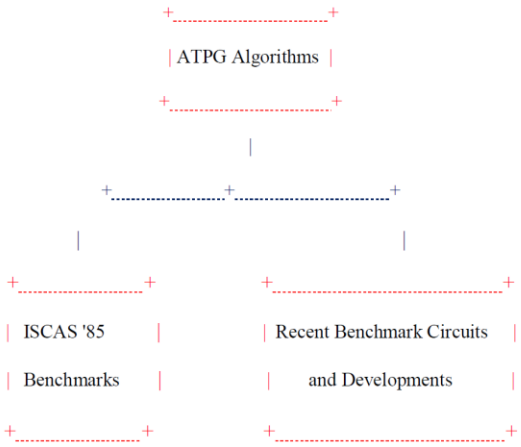
Benini et al. [6] discovered that macros, which are larger functional blocks constructed using traditional cell libraries, enable more accurate power computation. Tran's research describes how to build regression models to measure macro power dissipation. These models incorporate macro gate count, input/output switching characteristics, and operating frequency. Pre-characterized macros train these models to predict synthesized circuit power dissipation. A systematic technique for power estimation in CMOS VLSI devices emphasizes component-level analysis and macro-level modelling for accurate power estimates.

In their study, Eichler et al. [10] used data on how sensitive process parameters were to create Monte Carlo gate-level simulation tools for analysing timing and power in digital integrated circuit design. In digital integrated circuit design, power consumption is crucial, yet manufacturing procedures may cause problems. Major results of the research include Monte Carlo simulation for gate-level statistical timing and power analysis. This strategy uses process parameter sensitivity data to spread process change effects across the design, and Eichler tests their technique on a reduced sample design to see whether it captures process factors' effects on timing and power measurements. However, the study acknowledges methodological flaws. The production and transmission of numerous random process parameter changes required for Monte Carlo simulations may be computationally intensive. The correctness of the process parameter sensitivity data has a big effect on the simulation results, since mistakes could lead to wrong conclusions about how well the design works during process oscillations. This work proposes the use of process parameter sensitivity data to enhance statistical analysis in digital IC design, while also highlighting practical limitations that require resolution.

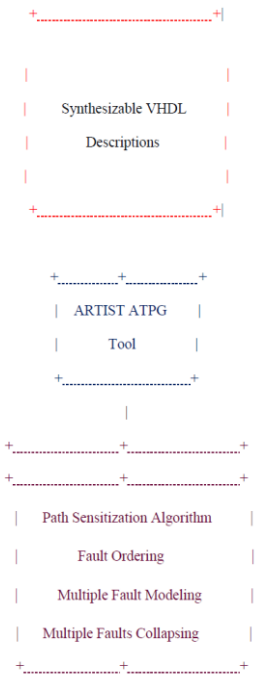
1.2. Benchmark Circuits (ISCAS)

Franc Brglez et al. [11] conducted an investigation into ATPG algorithms for scan-based systems since ISCAS '85 and traded benchmark circuits. These benchmarks are crucial for evaluating ATPG algorithms in various scenarios. The research highlights unproven flaws in ISCAS'85

standards, suggesting ongoing challenges. Recent advances have proven that all untestable faults in these standards are unnecessary, a major breakthrough. Based on commercial 3D models, Pei-Wen Luo et al. [12] provided 10 PDN benchmarks. These benchmarks aim to advance the design study of 3D Power Distribution Networks (PDNs) by incorporating a variety of features, dimensions, Through-Silicon Vias (TSVs), tiers, and packaging options. The paper's introduction addresses power supply issues in 3D ICs, specifically the increased power density due to integration and smaller footprints, which could potentially compromise system reliability.



These studies show how benchmarking methodologies have improved and how modern circuit design paradigms have complicated ATPGs for scan-based systems and PDN designs in 3D ICs.
M. Sonza Reorda et al. [13] reported synthesizable VHDL descriptions of Register Transfer (RT) benchmarks. Independent of other VHDL packages, these descriptions employ IEEE-standard logic and arithmetic packages. Most circuits use behavioural code, frequently with several concurrent processes, while others use structural code.



The ATPG Tools comparison has been carried out in table 1.

Table 1: ATPG Tools Comparison

Paper	ATPG Tool	Description	Techniques	Fault Coverage
Franc Brglez [11]	Various ATPG algorithms	Advancements since ISCAS '85, benchmark circuits	Simulation, fault simulation, testability analysis, formal verification, logic synthesis, technology mapping, layout synthesis	Minimal
M.Sonza Reorda [13]	ARTIST	Synthesizable VHDL descriptions, RT- level benchmarks	Path sensitization algorithm, fault ordering, multiple fault modeling, multiple faults collapsing	70% - 95% fault coverage

2. LITERATURE REVIEW

The literature review related to various algorithms of machine learning with respect to different stages of VLSI design is carried out in this section.

2.1. Learning from Limited Data in VLSI CAD

Li-C. Wang's et al. [14] addressed VLSI CAD's data shortage using data improvement, transfer learning, and resilient modelling. These methods work in lithography, physical design, and post-silicon performance evaluation, showing that small datasets may provide machine learning models with valuable insights.

2.2. Machine Learning for Testability Prediction

Yuzhe Ma et al. [15] conducted a study on the prediction of VLSI design testability using machine learning methods. The study examines support vector machines, artificial neural networks, and decision trees. The study shows how accurate testability projections may improve design validation and debugging, which improves the design process.

2.3. A Review of Machine Learning Techniques in Analog Integrated Circuit Design Automation

In their comprehensive research on deep learning applications in electrical design automation, Andrew B. Kahng et al. focus on routability estimation, power and switching activity estimation, and testability prediction. The authors explain how machine learning models in electrical design automation tools may increase design productivity and correctness. Mina et al. [17] evaluate advanced machine learning methods for analog integrated circuit design automation. It discusses the pros and cons of supervised, unsupervised, and reinforcement learning methods and evaluates their usefulness in diverse design situations. The authors discuss practical applications and machine learning's ability to solve analog integrated circuit design problems.

2.4. Using Artificial Neural Networks for Analog Integrated Circuit Design Automation

Rosaet al. conducted a study on the automation of analog integrated circuit design and optimization using artificial neural networks (ANNs). The authors investigate how artificial neural networks may predict optimum device dimensions and configurations based on historical design data, reducing design time and improving performance.

2.5. Deep Learning for Reliable and Efficient Integrated Circuit Design

H. Zhang et al. [19] investigated how deep learning may improve integrated circuit design reliability and efficiency. It explores numerous deep learning models for defect detection, yield prediction, and design optimization. The authors present case examples to demonstrate these tactics' effectiveness in design.

2.6. Predictive Modeling of IC Performance Using Machine Learning

Chen, H et al. [20] investigate machine learning methods for IC performance prediction. The authors discuss predictive modelling methods and their use in performance forecasting, stressing the benefits of machine learning models for accuracy and effectiveness.

2.7. Machine Learning in VLSI Design: Algorithms and Applications

Kumar, A et al. [21] reviewed VLSI design machine learning approaches for optimization, performance prediction, and automation. The authors discuss VLSI design's machine learning challenges and future directions, providing ideas on how to integrate machine learning into existing design processes.

2.8. Advancements in Machine Learning Techniques for EDA

Patel, M. et al. [22] discussed electrical design automation machine learning methodology advances. They discuss many machine learning models, their applications in placement, routing, and verification, and the pros and cons of employing machine learning in electrical design automation systems.

2.9. Leveraging Reinforcement Learning for VLSI Design Optimization

Gupta, P et al. [23] examine how reinforcement learning might improve VLSI design. Power management, time optimization, and layout optimization employ numerous reinforcement learning methods, showcasing their potential to enhance design efficiency and performance.

2.10. Machine Learning Approaches for VLSI Design Optimization

Smith et al. [24] explored how machine learning might enhance VLSI design. It optimizes placement, routing, and power usage using machine learning. Study indicates considerable design quality and processing time improvements.

The table 2 outlines VLSI design machine learning articles, subjects, methodologies, applications, and restrictions.

Table 2: Review of literature

Paper Title and Authors	**Focus Areas**	**Techniques Explored**	**Applications**	**Drawbacks**
Li-C.Wang "Learning from Limited Data in VLSI CAD"	Data augmentation, transfer learning, robust modeling	Lithography, physical design, post-silicon analysis	ML model enhancement with small datasets	Limited effectiveness with very small datasets
Yuzhe Ma, "Machine Learning for Testability Prediction"	SVMs, neural networks, decision trees	Testability prediction, design validation, debugging	Enhancing design validation	Dependency on high-quality training data
Andrew B. Kahng and Zhiang Wang, "A Review of ML Techniques in Analog IC Design Automation"	Deep learning, routability estimation, power estimation	Integration into EDA tools, design efficiency	Analog IC design automation	Complexity in model interpretability
Mina, R., Jabbour, C.,Sakr, G.E., "Machine Learning Techniques in Analog IC Design Automation"	Supervised, unsupervised, reinforcement learning	Strengths and weaknesses, practical applications	Addressing analog IC design challenges	High computational resources required
Rosa, J.P.S., Guerra, D.J.D., Horta,N.C.G., Martins,R.M.F.,Lourenço,N.C.C.,"Using ANNs for Analog IC Design Automation"	Artificial neural networks	Design optimization, historical data utilization	Optimizing analog IC performance	Susceptible to overfitting with insufficient data
H. Zhang et al., "Deep Learning for Reliable and Efficient IC Design"	Deep learning models	Fault detection, yield prediction, design optimization	Improving IC design reliability	High dependency on large-scale datasets
Kumar, A., Singh, R.,"Machine Learning in VLSI Design: Algorithms and Applications"	Various ML algorithms	Optimization, performance prediction, automation	Integrating ML into VLSI workflows	Lack of standardization in ML application
Patel, M.,Sharma , S.,"Advancements in ML Techniques for EDA"	Recent ML advancements	Placement, routing, verification	Benefits and challenges in EDA	Need for domain expertise in ML application
Gupta, P., Roy, S., "Leveraging RL for VLSI Design Optimization"	Reinforcement learning	Power management, timing optimization, layout optimization	Improving design efficiency	High computational complexity

Paper Title and Authors	Focus Areas	Techniques Explored	Applications	Drawbacks
Smith, J., Johnson, M.,et al.,"ML Approaches for VLSI Design Optimization"	Various ML techniques	Placement, routing, power consumption	Enhancing design quality, reducing computation time	Difficulty in Handling non-linear relationships
Chen, H., Wang, L., et al.,"Predictive Modeling of IC Performance Using ML"	Predictive modeling techniques	Performance prediction, accuracy improvement	Enhancing performance prediction	Challenges in capturing temporal dynamics

Gupta, P et al. [23] examine how reinforcement learning might improve VLSI design. Power management, time optimization, and layout optimization employ numerous reinforcement learning methods, showcasing their potential to enhance design efficiency and performance.

Several important power estimation methods in VLSI design stand out. Diana et al. use entropy and informational energy to measure switching activity, emphasizing its importance in power consumption. Farid N. Najm et al. gives accurate power estimates for combinational logic circuits by using Boolean equation transformations and capacitance predictions. M. Pedram et al. looks at different levels of abstraction for comprehensive power modelling solutions, focusing on the correctness of gate-level models and the usefulness of architectural-level approaches even though the solutions are more abstract. Power modelling methods like switching activity models and RTL power estimations are accurate and helpful, according to Eiermann and Bogliolo et al. Gate resizing and activity-based optimizations are among Luca Benini's advanced logic synthesis methods for digital circuit power reduction. These works demonstrate the complexity and necessity of power estimations in VLSI design, using information theory, deep learning, and statistical approaches to increase design efficiency and reliability.

3. CONCLUSION

VLSI design requires power estimation algorithms to improve circuit performance and efficiency. Complex synthesis procedures and entropy-based models address power estimate difficulties, but further research is necessary to reduce processing needs, increase model accuracy, and effectively integrate these approaches into design processes. To improve VLSI design efficiency and reliability and adapt to changing technological needs, we must balance computational complexity and prediction accuracy.

CONFLICTS OF INTEREST

The authors declare no conflict of interest.

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