ANALYSIS OF RANDOM DISTORTIONS IN THE ELEMENTS OF THE BASIC CELL FOR AN ANALOG-DIGITAL PIPELINED CONVERTER

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ABSTRACT

This paper presents an analysis of random distortions in the elements of the basic cell for an analog-digital pipelined converter. Pipelined converters are popular for their high sampling rates and resolution ranges. Each basic cell has a few-bit digital-analog converter connected to its output with a digital-to-analog converter to compare the input signal. This study aims to analyze the effects of random variations in the converters' elements. The proposed system is designed, with experiments conducted to observe the effects of distortions. The results of simulated architecture and distortion tests are presented, and the reached conclusions are presented in the fourth section.

The basic cell used to build the converter is described in Equation 1, which describes the cell's operation. Six cells cascade-connected were used to construct the converter, with the input of the first block being the input and its output connected to the input of the second station. The true output of the converter is constructed by each of the output bits of each cell, with the bit of the first station being the most significant bit until reaching the output bit in the last cell.

KEYWORDS

Analog-digital converter, basic cell, output signal analysis

1. INTRODUCTION

Pipelined analog-to-digital converters have become the most popular converter architecture, with sampling rates ranging from a few mega samples per second to hundreds of mega samples, and with resolution ranges from eight bits to 16 bits. [1].

The architecture of these converters can be very varied, but they have similarities. Each basic cell has a few-bit digital-analog converter, which is connected to its output with a digital-to-analog converter to compare the input signal. After the comparison, its result is multiplied by two, and the output of said multiplication is sent to the next cell, unlike [2][3], and [4]. For the present proposal it was decided to omit the retaining element, this causes the system to operate in free stroke, which may be negative in a possible implementation, but for the present proposal, it is not so inconvenient.

The analysis of variations in the converters is a regular study in this type of system since it must be analyzed how robust the converter is to changes in its internal conditions, which can be caused by many things such as variations in the power supply. [5], details in the manufacturing of the elements [6], among others.

For this last reason, it was decided to analyze the effects that this type of converters suffer from random variations in the elements that make them up. This work is composed of three additional sections. The second section constitutes the design of the proposed system, as well as the experiments carried out to see the effects of the distortions. The results of the simulated architecture and distortion tests are presented in the third section. Finally, the fourth section shows the conclusions reached as a result of this work.

2. CONVERTER'S DESIGNING

The philosophy behind pipeline converters is that they are fast, which is why they work through stations. Based on the above, we describe the basic cell used to build the converter. The mathematical function that describes the cell's operation is presented in Equation 1.

$$y=\begin{cases} 2x & x<1 \\ 2(x-1) & x\geq 1 \end{cases}$$

Equation 1

As can be seen for both conditions, it must be multiplied by two; Therefore, that operation is done at the end of the block. The conditional is done mathematically using a sum element and a logic block that evaluates whether the input is greater than unity. The output of the logic block in turn serves as the output bit, that is, it delivers the result of the conversion for that station. In Figure 1 you can see in detail the internal arrangement that constitutes the basic cell of the converter.

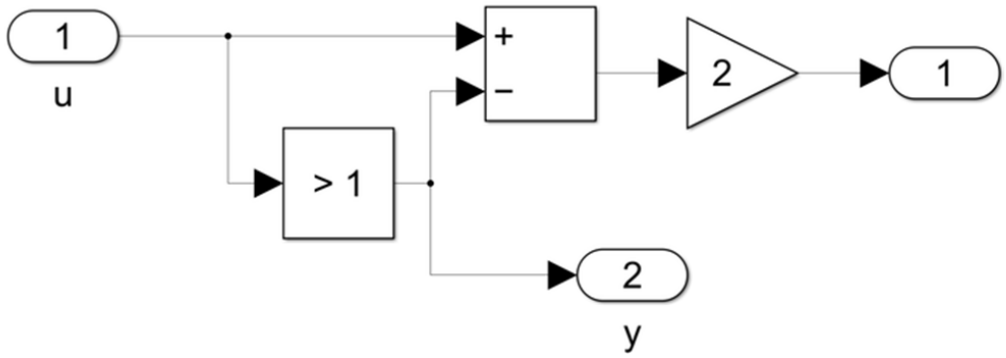

Figure 1. Inner basic cell architecture to construct analog-digital converter.

To build the converter, six cells cascade-connected were used, where the input of the first block is the input of the converter, and its output is connected to the input of the second station, and so on until reaching the sixth station, whose output is the output, although it only delivers the residue of the converter. The true output of the converter is constructed by each of the output bits of each cell, with the bit of the first station being the most significant bit of the converter until reaching the output bit in the last cell, which corresponds to the least significant bit. The distribution described above can be seen in greater detail in Figure 2.

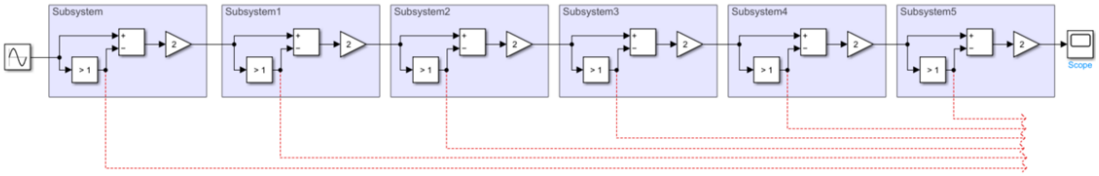

Figure 2. Cascade construction of the analog-digital converter

A digital-analog converter was developed to validate that the output bit of each of the stations in the converter was correct. Therefore to carry it out, the mathematical definition described in Equation 2 was followed.

$$y = \sum_{i=0}^{N} 2^{i} \cdot x_i$$

Equation 2

Where N is the total number of stations or bits that you want to convert analogically, xi is the value of the output bits of each station. Using the definition of Equation 2, we have that the range of the output "y" is in the range of (0.63), and for the present application it is preferred that it be normalized, therefore the output of the adder is divided by 64, leaving the normalized output of "y" in the range (0,1). Said digital–analog converter can be seen in Figure 3.

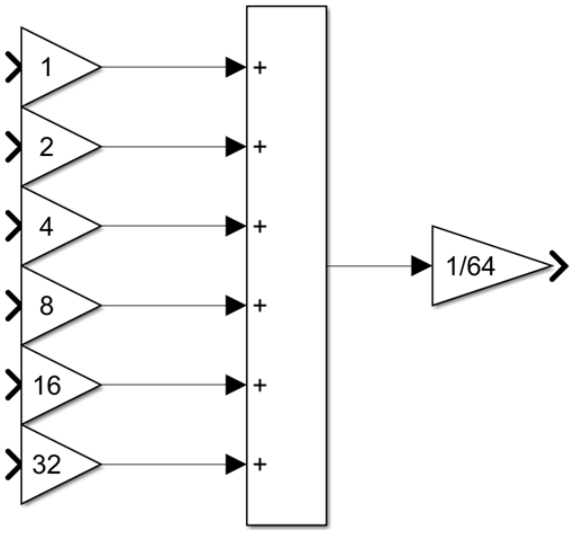

Figure 3. A Digital-analog converter was created to evaluate the output bits of the stations connected in cascade form.

With all the design elements of the pipelined converter already described, we proceed to properly interconnect them to evaluate their operation. Additionally, the modifications and considerations made to the architecture presented in Figure 4 will be presented, to analyze the effects that produce variations in each of the effects that constitute it.

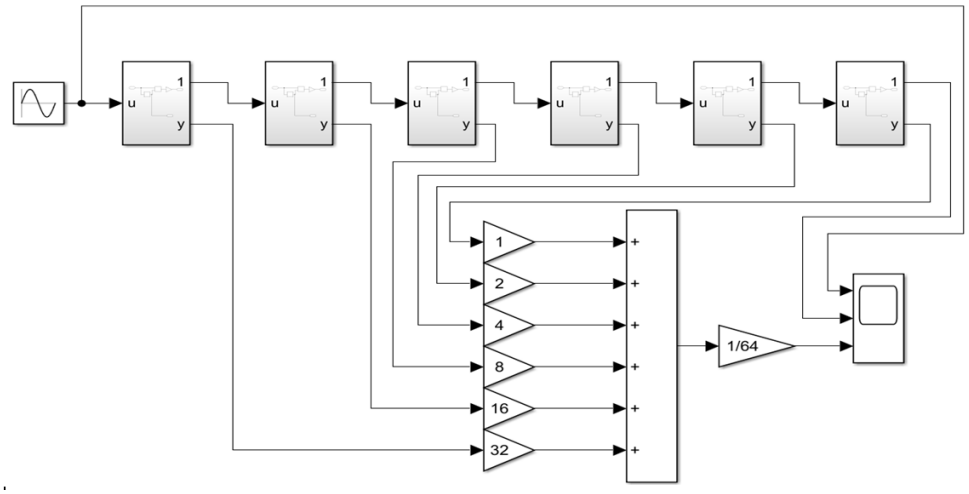

Figure 4. Pipeline architecture for the analog-digital converter, as well as the element to check its operation

2.1. Design of the Experiments to Observe Random Effects on the Elements of the Basic Cells

There are two experimental proposals for the present project. Their aim is to evaluate the robustness of this type of converter against the variations of its components, which are the comparator, adder, and multiplier. These three elements were altered from their original form to add a source of randomness, which was created by using a block of random numbers.

The random number block generates random numbers periodically, however for this application, it is required that it be only one number throughout the simulation; Therefore, it is configured so that it is generated every ten seconds, which is the simulation time, thus giving the appearance that it is constant. Another peculiarity lies in the configuration of the distribution of the generated numbers and is that it allows defining the mean and variance, as well as the seed. To define the mean, the nominal value used for the simulation without alteration was used, while the variance is defined at 0.001.

The last value to be defined in the block of random numbers is the seed, and it is at this point that the two proposals of the experiment are created. The first is with equal seeds, that is, regardless of the block or the station, all blocks of random numbers would have the same seed. The idea is to have maximum impact, as the random numbers generated will be sparsely dispersed. For the other experiment proposal, we choose to vary the seed between negative and positive numbers in equal parts, so that the numbers generated are balanced, in terms of their statistical dispersion. In Figure 5 you can see the modifications made to the basic cell to be able to carry out the experiments mentioned above.

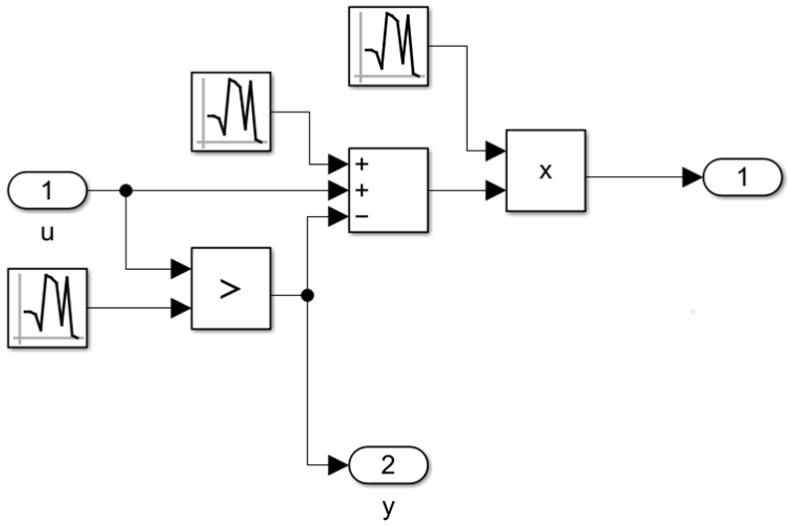

Figure 5. Inclusion of random number blocks in the basic cell of the analog-digital converter

3. RESULTS

The first result presented is the one corresponds to the output of the analog-digital converter (ADC) that serves as a complement to the present pipeline converter work. Of the signals presented in Figure 6, the one at the top corresponds to the input signal, that is, the signal to be converted, and has a peak-to-peak value of two. The second signal that appears is the output of the supporting ADC to monitor the operation of the pipelined converter. Its peak-to-peak output is one, this is due to the conversion factor, although it is easily adjustable. The important thing is that the output signal does not present significant distortions.

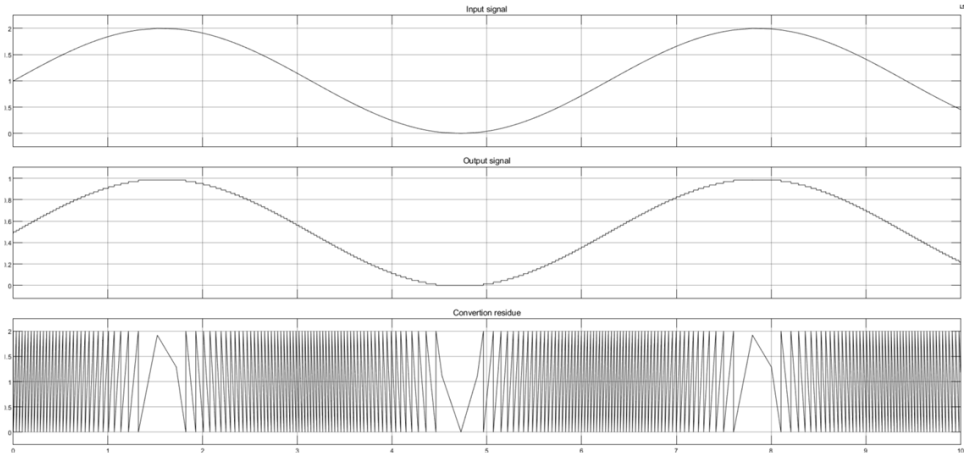

Figure 6. Output signals in the case of the digital-analog converter without disturbances.

The signal below corresponds to the remainder of the last station of the pipelined converter, which would serve as input for subsequent stages if a converter with a greater number of output bits is required.

Now, the comparison is presented between the output signal from the system without disturbances and that which presents the disturbances produced with equal seeds. The output

signal of the system with disturbances is greater than that without disturbances, it is seen in Figure 7; although it presents certain variations that make it smaller at some points, they are the least.

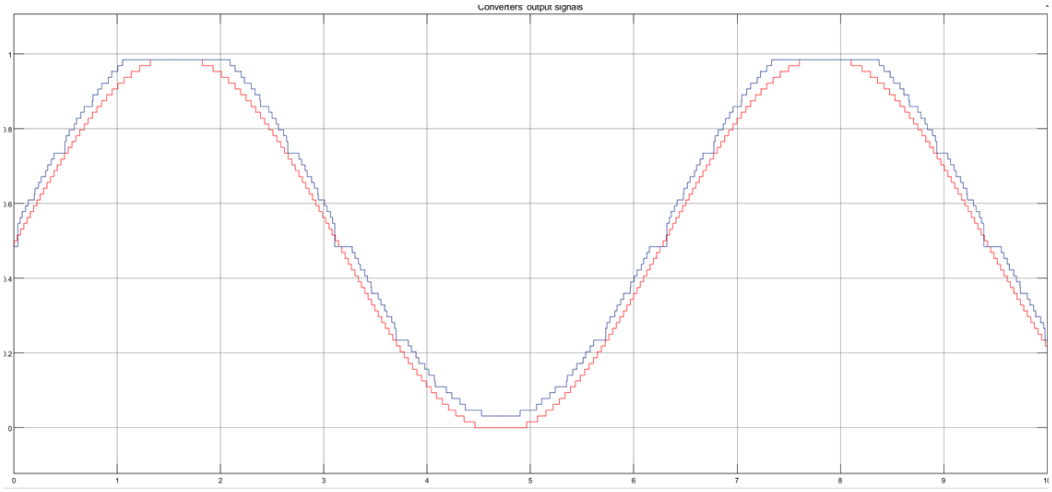

Figure 7. Comparison between the output non-disturbed system output (red) and the disturbed from same seed randomness one (blue).

On next, we present the comparison between non-disturbed system with the disturbed one, using distributed seeds. As it is shown on Figure 8, both signals are similar but some instantly variations.

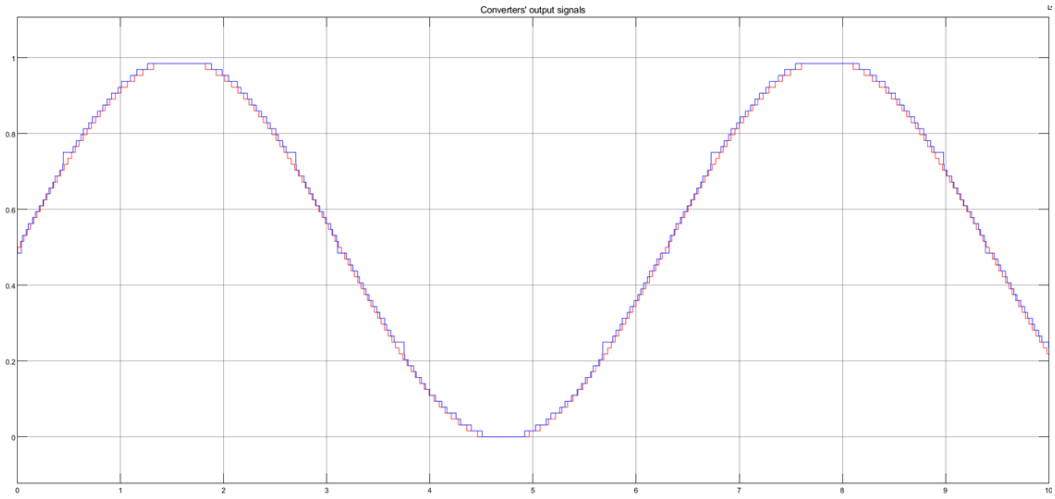

Figure 8. Comparison between the output non-disturbed system output (red) and the disturbed from different seed randomness one (blue).

To make a fairer comparison, we proceed to find the difference between the signals with disturbances and the signal without disturbance. To do this, a simple subtraction is chosen, and the absolute value of the output is calculated. The results of these absolute differences are presented in Figure 9. The signal above is from the difference with the perturbation signal through distributed seeds. The signal has values between 0.015 and 0, although with peaks that reach 0.045.

On the other hand, the signal below in Figure 9 presents the difference with the disturbance signal from the same seed. Their values are between 0.045 and 0.03; however, they have areas where this difference falls down to zero but also it has peaks where it exceeds 0.06.

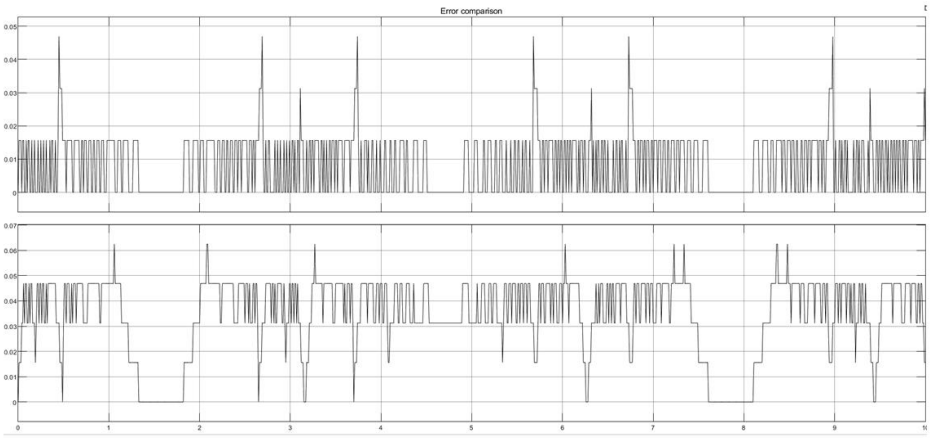

Figure 9. Comparison of the differences caused by the randomness introduced in the basic cells.

Finally, an adder is made in a feedback loop to keep the accumulated differences. Figure 10 shows the evolution of the accumulated, and it can be seen that for the case in which the same seed is used (lower graph), the accumulated difference reaches almost the value of 35; while for the difference with the signal produced from homogeneously distributed seeds, the accumulated difference exceeds a value of eight.

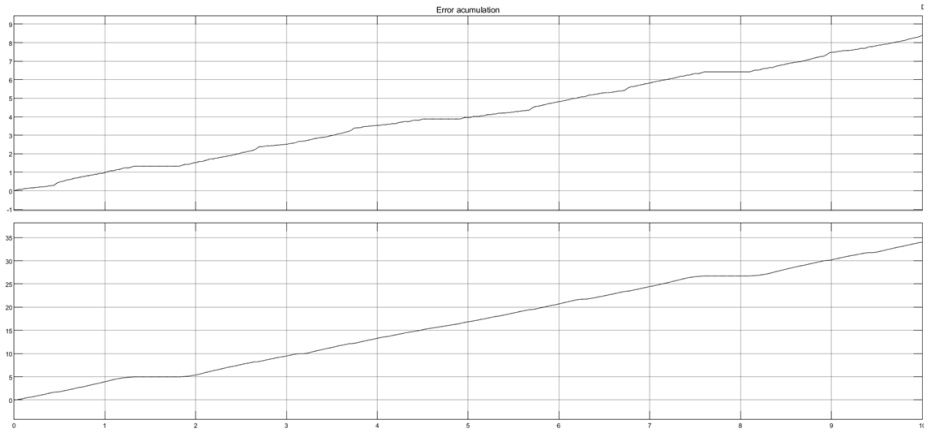

Figure 10. Accumulative difference between the system without disturbances and disturbed system from the same seed (bottom) and homogeneously distributed seeds (top).

4. CONCLUSIONS

From the results obtained, two conclusions can be reached: The first conclusion is that the smaller the distribution of the generated numbers the greater the effect on the converter. However, due to the nature of the disturbances, this is usually unlikely, which results in a second conclusion. The proposed system seems more robust than originally thought since an error in the

first station does not result in a clear deterioration of the last ones; moreover, the entire system has adaption capability.

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