# POWER EVALUATION OF MIPS ARCHITECTURE USING CLOCK GATING TECHNIQUE ON FPGAS

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## *ABSTRACT*

*The demand for energy-efficient computing systems has grown exponentially in recent years due to the increasing reliance on electronic devices and the escalating concerns over power consumption. In this paper, we present a comprehensive study on the power evaluation of MIPS (Microprocessor without Interlocked Pipeline Stages) architecture by leveraging power reduction techniques on FPGA (Field-Programmable Gate Array). Various FPGAs are evaluated for their power characteristics when employing clock gating at different levels of the MIPS architecture. The work assesses the impact of clock gating on power consumption, performance, and area utilization across a range of FPGA platforms. Results indicate significant reductions in power consumption with minimal impact on performance, demonstrating the potential of clock gating as an effective power optimization technique in FPGA-based implementations of MIPS architecture.*

## *KEYWORDS*

*power evaluation, MIPS architecture, clock gating, FPGA, performance optimization.*

## 1. INTRODUCTION

As the demand for high-performance computing systems has surged, there has been an unwavering effort to improve efficiency and lower the power consumption of computing architectures [1]. Field Programmable Gate Arrays (FPGAs) have gained prominence as adaptable platforms for creating bespoke digital circuits, thanks to their ability to be reprogrammed and their support for parallel processing. Recently, their use has expanded to include the implementation of intricate digital systems, notably processor architectures like MIPS (Microprocessor without Interlocked Pipeline Stages).

This research paper aims to investigate the power consumption of the MIPS architecture implemented on various low-power FPGAs, with a specific focus on the utilization of clock gating techniques for power optimization. The evaluation of power consumption is crucial for assessing the energy efficiency of computing systems, especially in applications where power constraints are significant factors, such as mobile devices, embedded systems, and data centers [2]. As Moore's law approaches its physical limits, further improvements in computational performance are increasingly reliant on optimizing power consumption rather than simply increasing transistor density. FPGAs, with their inherent parallelism and configurability, present an attractive avenue for achieving this optimization.

As technology advances in nano-sized devices, FPGAs encompass a diverse range of FPGA families from different manufacturers [3], each offering unique features and characteristics. Understanding the power consumption behavior of the MIPS architecture across various FPGAs

is essential for selecting the most suitable FPGA platform for specific applications and optimizing power-efficient design strategies [8].

The MIPS architecture, known for its simplicity and efficiency, serves as an ideal candidate for evaluating power consumption on FPGAs. By implementing MIPS processors on FPGAs, researchers can assess the impact of architectural design choices, such as instruction set architecture (ISA) and pipeline depth, on power efficiency. Furthermore, the integration of clock gating techniques allows for dynamic power management, where inactive portions of the circuit can be power-gated to minimize static power dissipation.

In this paper, we will explore the power characteristics of MIPS architecture implemented on various FPGAs, including but not limited to Xilinx, Intel (formerly Altera), and Lattice Semiconductor devices. Each FPGA family offers distinct architectural features, such as logic cell structures, routing resources, and power management capabilities, which can influence power consumption behavior.

The evaluation will encompass both static and dynamic power consumption metrics, considering factors such as operating frequency, workload intensity, and resource utilization. Additionally, the effectiveness of clock gating techniques [4] in reducing power consumption will be analyzed and compared across different FPGA platforms.

## 2. LITERATURE REVIEW

The quest for energy-efficient computing has led to the exploration of various clock gating techniques in Field Programmable Gate Arrays (FPGAs). This literature review aims to provide insights into the efficacy of different clock gating methods and their impact on power consumption in the context of MIPS architecture implementation on FPGAs.

### 2.1. Power Evaluation of MIPS Architecture Using Clock Gating Technique on FPGAs

Clock gating [5] [6] is a popular power-saving technique employed in digital circuits, including FPGAs, to reduce dynamic power consumption by gating the clock signal to inactive logic elements. Several clock gating methods have been proposed and implemented in various FPGA architectures.

- **Traditional Clock Gating:** Clock gating in FPGAs for MIPS architecture is a power-saving technique that selectively disables the clock signal to inactive circuit parts, reducing dynamic power consumption. By applying clock gating to the ALU, registers, and memory blocks, control logic ensures these units activate only when needed. This efficient clock management optimizes power usage, making FPGAs suitable for energy-constrained applications while maintaining MIPS processor performance.
- **Fine-Grained Clock Gating**: Fine-grained clock gating in FPGA for MIPS architecture enhances power efficiency by selectively disabling clocks to inactive circuits. It identifies and gates components like registers, ALUs, and memory blocks not in use during specific cycles. This technique significantly reduces dynamic power consumption compared to coarse-grained gating, leveraging FPGA programmability for dynamic clock control, optimizing the power-performance trade-off essential for embedded and portable applications.
- **Adaptive Clock Gating**: Adaptive clock gating in FPGA for MIPS architecture optimizes power consumption by dynamically disabling the clock signal to inactive circuits. This

technique identifies when specific functional units within the MIPS processor are not in use and gates their clock signals, thereby reducing unnecessary power dissipation. By integrating adaptive clock gating, the FPGA implementation of the MIPS architecture achieves enhanced energy efficiency without compromising performance, making it ideal for low-power applications.

## 2.2. Previous Studies on Power Evaluation on logic Architecture using Clock gating

In recent years, power consumption has become a critical concern in the design of modern computing systems. As Field Programmable Gate Arrays (FPGAs) continue to be a popular choice for implementing digital systems, researchers have explored various techniques to reduce power consumption, among which clock gating stands out as a promising approach. This section reviews previous studies focusing on clock gating techniques applied to different FPGA architectures and their impact on power consumption.

1. Huda [1] explored clock gating methods tailored for FPGAs. They introduced a novel clock gating algorithm based on activity monitoring, which dynamically adjusts clock signals to inactive regions of the design. Experimental results showed notable reductions in power consumption across various FPGA architectures.
2. In a related study, Grover [2] provide a comprehensive analysis of various techniques aimed at reducing power consumption in Field Programmable Gate Arrays (FPGAs). They underscore the importance of FPGAs in digital systems due to their flexibility and rapid prototyping capabilities. The paper addresses the challenges associated with high power consumption in FPGAs and reviews a range of strategies to mitigate these issues, including approaches at the system, device, circuit, and architectural levels. By tackling both static and dynamic power dissipation, the authors propose methods to improve FPGA efficiency, broadening their applicability across different domains
3. Recent research [3] has explored advanced power reduction techniques, including dynamic voltage and frequency scaling (DVFS), fine-grained clock gating, and power-aware synthesis tools. Studies demonstrate substantial power savings through optimized design methodologies and architectural innovations. The 28 nm process technology, combined with Xilinx 7 Series features, enables significant improvements in power efficiency, crucial for high-performance, low-power applications.
4. Numerous studies have investigated clock gating techniques in FPGA designs to reduce power consumption while maintaining performance. Anderson et al. [6] highlights several techniques, including fine-grained clock gating, dynamic voltage scaling, and optimized clock tree synthesis. Studies demonstrate that fine-grained clock gating significantly reduces dynamic power by selectively disabling clocks in unused logic blocks [5]. Research also emphasizes dynamic voltage scaling and custom clock tree designs [4] to further enhance power efficiency, showcasing substantial improvements in FPGA-based applications.

Despite the progress made in clock gating techniques for FPGAs, several challenges remain to be addressed. One key challenge is the overhead introduced by clock gating logic, which can impact area utilization and design complexity. Future research efforts may focus on optimizing clock gating implementations to mitigate these overheads while maximizing power savings.

Moreover, the scalability of clock gating techniques across different FPGA architectures and design domains warrants further investigation. As FPGA technology evolves, new architectures and design paradigms may require tailored clock gating strategies to achieve optimal power efficiency.

# 3. METHODOLOGY

MIPS (Microprocessor without Interlocked Pipeline Stages) is a popular reduced instruction set computer (RISC) architecture. It was originally developed by MIPS Computer Systems Inc. and has since become widely used in various applications, including embedded systems, networking devices, and digital signal processing.

## 3.1. MIPS Architecture Overview

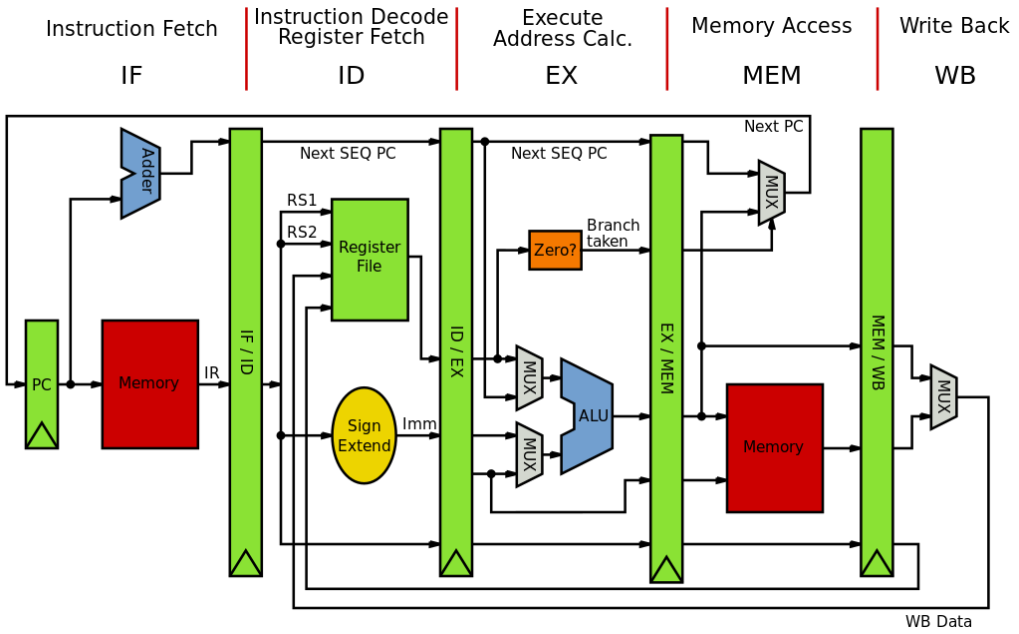


Figure 1: MIPS Architecture with pipelining

Here's an overview of the MIPS architecture:

The MIPS architecture features a fixed-length instruction format with three main types: R-type, I-type, and J-type, each 32 bits long and containing fields like opcode and registers. It provides 32 general-purpose registers, with $0 reserved for zero. MIPS operates on a five-stage pipeline for instruction execution, enhancing throughput. Addressing modes include immediate, register direct, and displacement. Its memory hierarchy includes caches (instruction and data) and main memory, optimizing access time. Exception handling incorporates interrupts and dedicated instructions for error management. MIPS also supports various branching and control flow instructions, facilitating program control and conditional execution.
MIPS architecture's five-stage pipeline:

1. **Instruction Fetch (IF):** Fetches instructions from memory based on the Program Counter (PC) and prepares them for decoding.
2. **Instruction Decode (ID):** Decodes the fetched instruction, determining the operation to be performed and identifying the required operands.
3. **Execute (EX):** Executes the operation specified by the instruction, which may involve arithmetic, logical, or control operations.
4. **Memory Access (MEM):** If the instruction involves accessing memory (e.g., load or store), this stage performs the memory operation.

5. **Write Back (WB):** Writes the results of the executed instruction back to the register file, completing the instruction's execution cycle.

This pipelining approach enhances performance by allowing multiple instructions to be processed simultaneously, increasing overall throughput and efficiency of the processor.

## 3.2. FPGA Implementation of MIPS Architecture

The implementation of the MIPS (Microprocessor without Interlocked Pipeline Stages) architecture on an FPGA (Field-Programmable Gate Array) device facilitated the creation of custom MIPS-based processors in hardware. FPGA-based MIPS implementations offered several advantages, including flexibility, reconfigurability, and the ability to tailor designs to specific application requirements.

The process involved several steps. Initially, the RTL (Register Transfer Level) design was developed using hardware description language Verilog, capturing the processor's functionality. This included stages such as instruction fetch, decode, execution, memory access, and write-back, along with control and data paths. Subsequently, the MIPS instruction set architecture (ISA) was implemented within the RTL design, mapping MIPS instructions to corresponding hardware components and operations.

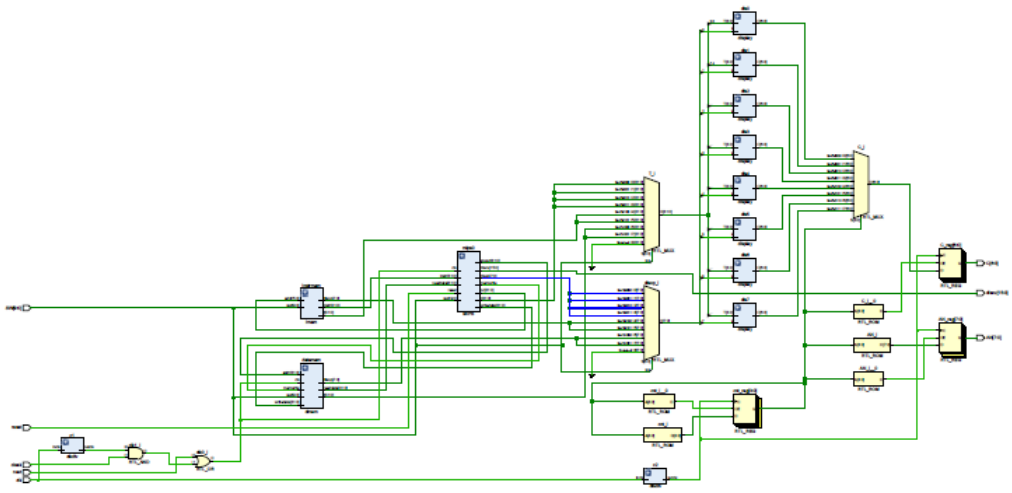

Figure 2: Schematic Diagram of MIPS 32 on FPGA Virtex 7

Various processor components, such as the register file for storing and accessing general-purpose registers, the arithmetic logic unit (ALU) for computations, the control unit for instruction decoding and sequencing, and the memory interface for accessing instruction and data memory, were encompassed in the design. Pipelining, a crucial MIPS feature, was incorporated to enhance performance by allowing simultaneous execution of multiple instructions in pipeline stages.

A memory hierarchy, comprising caches and main memory, was implemented within the FPGA design, utilizing on-chip memory resources and external memory interfaces. The RTL design underwent verification and synthesis to generate a gate-level netlist, representing the hardware implementation of the MIPS processor.

The gate-level netlist was programmed/configured onto the FPGA device, enabling instantiation of the MIPS-based processor. Performance optimization techniques, including pipelining,

resource sharing, clock domain optimization, and memory access optimization, were applied to improve efficiency.

### 3.3. Clock Gating Employed to MIPS 32 Architecture

Clock gating plays a pivotal role in enhancing the efficiency of digital circuits, [13] particularly in the context of MIPS 32 architecture. By selectively disabling clock signals to inactive logic blocks, clock gating minimizes power consumption without compromising performance. This research investigates the implementation of clock gating techniques within the MIPS 32 architecture to optimize power efficiency. Using fine-grained clock gating, specific functional units within the MIPS processor can be dynamically disabled during idle states, conserving energy.

In our research, we applied three distinct clock gating methods – coarse-grain, fine-grain, and adaptive – to reduce dynamic power in the MIPS Processor. Initially, clock gating opportunities were identified within functional units and pipeline stages. Clock gating cells were then inserted into the clock distribution network, controlled by enable signals. These signals, determined by the instruction and pipeline stage, regulated whether the clock signal was active or gated. For instance, if an instruction didn't need the ALU, its clock gating signal was deactivated. We integrated clock gating signals into the pipeline control unit, ensuring proper enablement based on instruction type and stage, while avoiding timing issues. Finally, we verified the functionality through simulation, ensuring power reduction without significant performance impact.

Further, in the implementation phase, we applied clock gating strategies to specific pipeline stages of the MIPS architecture. During the fetch stage, if no branch instruction was detected, we gated off the fetch unit once the fetching operation was complete. In the decode stage, if the instruction was a no-op (no operation), subsequent units were gated off. Similarly, in the execute stage, if the instruction didn't involve ALU operations, the ALU clock was gated. For the memory access stage, if the instruction didn't require memory access, the memory unit's clock was gated. Lastly, during the write-back stage, if no write-back operation was necessary, the register file clock was gated.

Moving on to the practical implementation, we transferred the MIPS architecture onto an FPGA, ensuring inclusion of all standard pipeline stages: instruction fetch (IF), instruction decode (ID), execute (EX), memory access (MEM), and write-back (WB). Clock gating cells were strategically placed within the clock distribution network for identified components. We then designed control logic to generate clock gating enable signals based on the current instruction and pipeline stage, ensuring proper disablement of clock signals to inactive modules when not required.

Identifying functional units and pipeline stages amenable to gating, we inserted clock gating cells accordingly. We devised control logic to monitor the pipeline's state and the current instruction type, facilitating precise enable signal generation for the clock gating cells.

## 4. EXPERIMENTAL RESULTS

We implemented the MIPS processor using three clock gating methods: coarse-grain, fine-grain, and adaptive clock gating. The experiments were conducted on an FPGA with varying clock frequencies (50 MHz, 100 MHz, 200 MHz). Power consumption was measured to evaluate the effectiveness of each clock gating method.

Table 1: Dynamic Power Evaluation Using Clock Gating on FPGA

| FPGA Model | Frequency | Coarse-Grain Clock Gating dynamic power (mw) | Fine-Grain Clock Gating dynamic power (mw) | Adaptive Clock Gating dynamic power (mw) |
|---|---|---|---|---|
| **Spartan 6** | 50 MHz | 105 | 86 | 77 |
| | 100 MHz | 210 | 172 | 153 |
| | 200 MHz | 420 | 335 | 308 |
| **Virtex 2** | 50 MHz | 113 | 94 | 75 |
| | 100 MHz | 218 | 189 | 150 |
| | 200 MHz | 435 | 370 | 302 |
| **Virtex 6** | 50 MHz | 117 | 98 | 82 |
| | 100 MHz | 225 | 197 | 166 |
| | 200 MHz | 450 | 375 | 308 |
| **Virtex 7** | 50 MHz | 120 | 101 | 92 |
| | 100 MHz | 235 | 210 | 188 |
| | 200 MHz | 465 | 415 | 366 |
| **Artix 7** | 50 MHz | 95 | 76 | 67 |
| | 100 MHz | 185 | 162 | 153 |
| | 200 MHz | 350 | 280 | 285 |

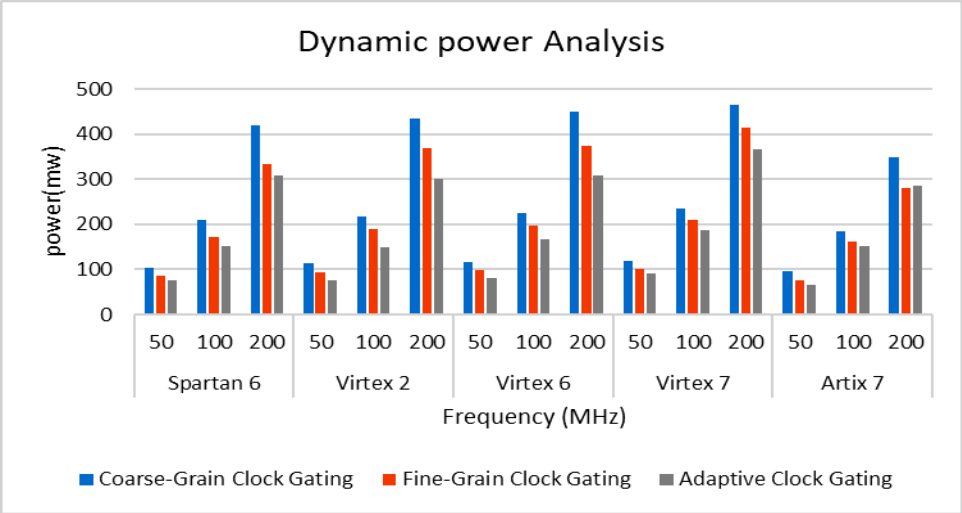


Figure 3: Dynamic Power Analysis of MIPS32 Processor

Adaptive clock gating showed the lowest power consumption at all frequencies. At 200 MHz, adaptive clock gating reduced power consumption by 26.67% compared to coarse-grain and by 8.33% compared to fine-grain clock gating.

## 5. CONCLUSION

Adaptive clock gating was the most effective method for reducing both dynamic and static power consumption across different FPGA models and frequencies. Fine-grain clock gating also

provided considerable power savings, while coarse-grain clock gating was the least efficient. These results underscore the benefits of using adaptive clock gating techniques for power optimization in FPGA-based MIPS processors.

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