DESIGN OF A HIGH PRECISION, WIDE RANGED ANALOG CLOCK GENERATOR WITH FIELD PROGRAMMABILITY USING FLOATING-GATE TRANSISTORS

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ABSTRACT

This paper presents a circuit of a high-precision, wide ranged, analog clock generator with on-chip programmability feature using Floating-gate transistors. The programmable oscillator can attain a continuous range of time-periods lying in the programming precision range of Floating Gates. The circuit consists of two sub circuits: Current Generator circuit and Wave Generator circuit. The current of current generator circuit is programmable and mirrored to the wave generator to generate the desired square wave. The topology is well suited to applications like clocking high performance ADCs and DACs as well as used as the internal clock in structured analog CMOS designs. A simulation model of the circuit was built in T-Spice, 0.35µm CMOS process. The circuit results in finely tuned clock with programmability precision of about 13bit [1]. Simulation results show high amount of temperature insensitivity (0.507ns/°C) for a large range of thermal conditions. The proposed circuit can compensate any change in temperature. The circuit design can be operated at low supply voltage i.e., 1v.

KEYWORDS

Square wave generator, floating gate FET, field programmability

1. INTRODUCTION

There are many oscillators like crystal oscillators; Novel RC oscillator [2], RC active frequency Oscillator [3], etc., have been developed, to accomplish the need of internal clock for synchronization between cells in VLSI circuit designs. However due to large size limitation, op-amp offsets and complicated designs respectively, many digitally on-chip trimmed RC oscillator

circuit designs [4], [5], [6] have also been developed. These clock generators are temperature insensitive and produce accurate clock which can be digitally trimmed using array of resistors or weighted capacitors.

With time the need for high speed data transmission and accuracy increases in the system designs. Hence a highly flexible and high precision clock generator is required to optimize for the next generation of wired or wireless network equipment that demands highly accurate clock generator and distribution for robust high speed transmission. Thus the research went in some other direction; clock generator using organic thin film transistors (OTFT) and inverters with bootstrapped transistors have been developed [7]. However it generates very low frequency clock. The wide and continuous ranged, accurate clocks are required in optical networks, mixed signal circuits, ATE, medical imaging and automated test equipments. Solutions proposed for such clock generation in recent years include usage of large devices and careful layout or some trimming and calibration techniques.

In this paper we use floating gate p-channel field effect transistor (FG-pFET) as a method for field programmable trimming of clock frequencies. The design can generate fine-tuning of the clock. In FG-pFET, by changing the charge at the gate we can program the variable frequency range. Tunable FG-pFET resistor offers good precision while passive resistors implemented using polysilicon, diffusion or well strips in CMOS technology exhibit around 0.1% matching accuracy and around 30% tolerance [8]. As well as tunable FG-pFET resistor will acquire less chip area as compared to other on-chip digital trimming circuit designs.

In section 2, we give the circuit diagrams of floating gate transistor, its programming and simulation model of tunable FG-pFET resistor. We perform the simulations for output clock generation and explained the design and programming methodology of the proposed circuit design. In section 3 and 4, we compared our proposed clock generator with digitally trimmed clock generator [4]. In section 5 and 6 technique used for on-chip programming and topology to widen frequency range of the output clock are briefly described. The temperature analysis of the proposed circuit is also shown in section 7.

2. PROPOSED CIRCUIT

This paper presents a simple RC Oscillator circuit based on the charge variation at the floating-gate of a FG-pFET which provides the flexibility of achieving a continuous range of resistance value, which in turn provides variable current required to generate the output clock. The clock generated can be precisely tuned with approximately 13 bit resolution [1]. The continuous, fine-tuned and wide ranged clock can be obtained. Compensation of variations due to change in temperature can be obtained by just tweaking the floating gate voltage of FG-pFET according to the specified temperature.

2.1 Floating-gate Transistor

Before introducing the basic floating gate clock generator, a brief discussion of floating gate transistors is beneficial. Though there are different types and variations of floating gate transistors, their basic construction and operation remain the same. Floating gate transistors are usually MOS transistors wherein memory is stored in the form of charge trapped on floating gate, affecting its threshold voltage. Since the gate is electrically isolated due to oxide completely surrounding it, the charge on the gate is fixed and is responsible for establishing the

amount of current flowing through the transistor. While the charge on the gate will not change on its own, that the processes such as UV photo injection, Fowler-Nordheim tunneling, and Hot-electron injection can modify that amount of charge. The last two are the primary means of programming floating-gate transistors to precise currents [9]. Once the desired charge is pushed onto the floating gate, it can be utilized to provide a constant bias to other transistors in a design, from which a precisely tuned clock can be generated.

Figure.1 shows the structure of a floating gate transistor. Due to their architecture, floating gate transistors are small, easily manufactured in CMOS processes, and provide simple post-fabrication programmability; characteristics which make them very useful in designing clock generator circuits.
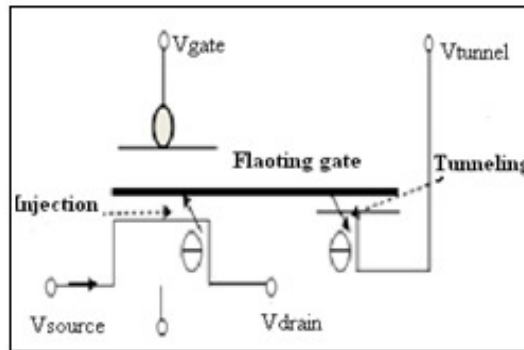

Figure 1:   Structure of floating-gate transistor [9]

Programming ability of the oscillator is obtained by modifying the charge stored on the floating gate. There are two programming topologies: direct and indirect programming. However, indirect programming provides real time applications to the design. It removes the necessity of a separate programming phase and an operational phase. As, in indirect programming, one pFET is connected to the programming structure while the source and drain of the other transistor are connected to the respective circuit (proposed circuit). The first pFET is programmed with hot-electron injection and tunneling. Since the charge on this "programmer" pFET (Mp) is modified, the current of the other transistor (the "agent") (Ma) will also be set as explained in figure2. With this programming technique, multiple FETs can share a common floating gate, and hence output range can be extended as explained in section 6.
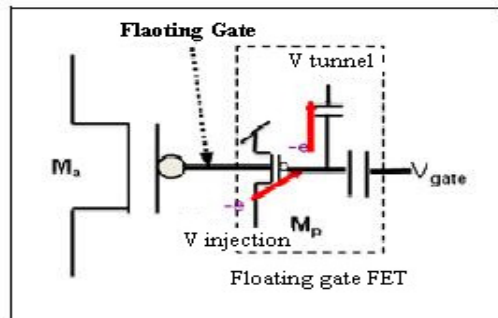

Figure 2: Indirectly programmed FG-pFET [10]

2.2 Tunable FG-pFET Resistor

The fundamental requirement to operate a single MOS transistor in the triode region as a linear resistive element is to suppress its nonlinearities by applying a function of the input signal to its gate [11] and/or its body [12]. The three principal nonlinearities in the drain current of a long-channel transistor in the triode region are identified as the body effect, the mobility degradation, and the fundamental quadric component due to the common-mode of the drain and source voltages [13]. Therefore to attain linearization in CMOS resistor a common mode and large voltage is employed at the gate. However, this technique does not completely eliminate the body effect and the mobility degradation. The gate linearization is achieved by using model from [13].

Since the transistor does not need to be disconnected from the circuit to program it, the switch count is reduced, resulting in fewer parasitic and better overall performance [10]. With the reference from [14] we have implemented FG-pFET indirectly programming circuit. Voltage dependent current sources and programmable PMOS have been used for tunneling and hot-electron injection to the floating gate as shown in figure3. For injection drain to source voltages of the programming PFET is varied and for tunneling V_{tun} is varied. Thus charge at the floating gate voltage changes and consecutively range of resistance can be obtained across the transistor.
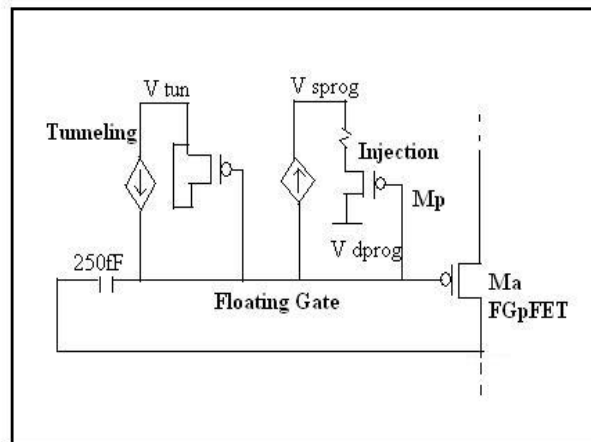

Figure 3. T-Spice 0.35um CMOS process Simulation Model of indirectly programmed tunable FG-pFET resistor

The simulation model of the indirectly programmed tunable FG-pFET was built in T-Spice, 0.35um CMOS process. The characteristics have been obtained from the simulation model. The hot-electron injection and tunneling currents have been plotted with respect to the floating gate voltage, as shown in figure 4. Due to these injection and tunneling currents variation which in turn, varied by using V_{tun}, V_{s_prog} and V_{d_prog} in the simulation model in figure 3, the floating gate voltage changes and hence the tunable resistance range can be obtained. Thus, the tuning range of FG-pFET resistor with change in floating gate voltage has been catered in figure 5.
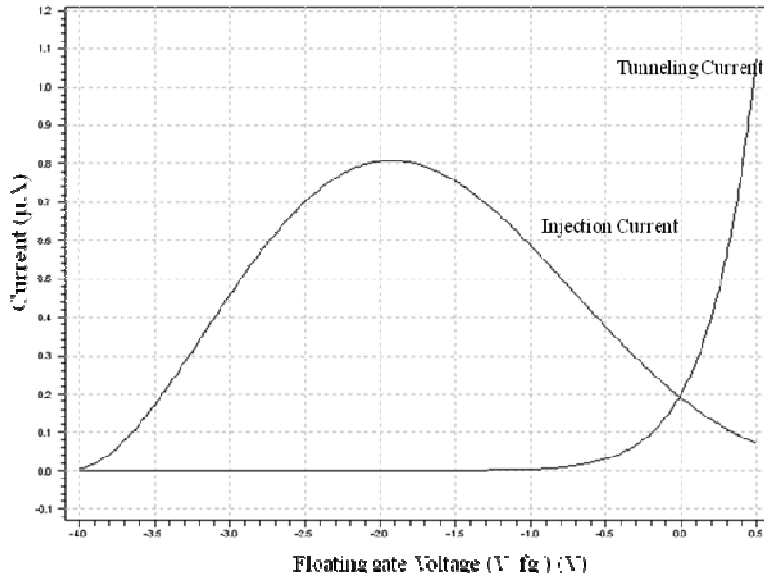
Figure 4: Characteristic currents of the indirectly programmed Floating gate transistor
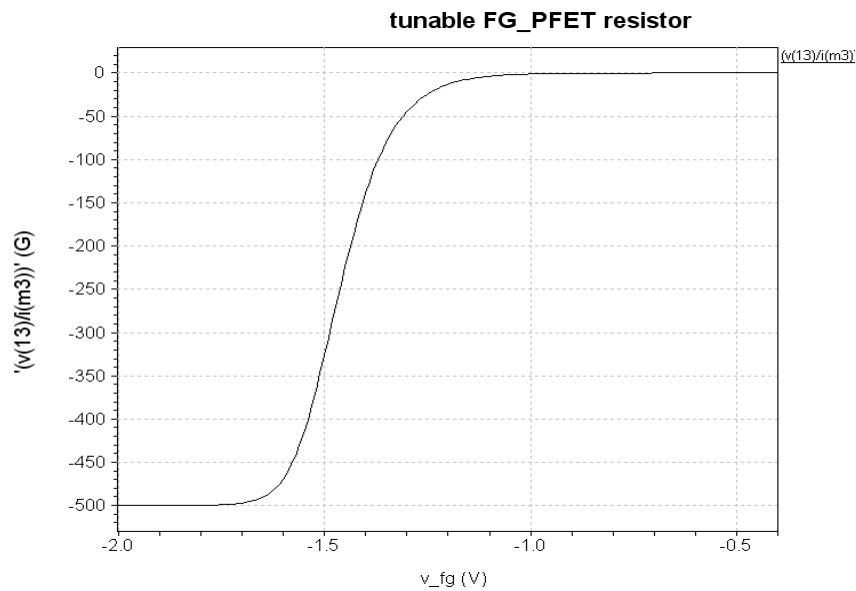

Figure 5: Tunable FG-pFET resistor range with respect to varying floating gate voltage, obtained from its simulation model implemented in T-Spice 0.35um CMOSS process.

2.3 FG-pFET Programmable Clock Generator

The proposed Clock generator circuit using floating gate pFET as shown in Figure 6 consists of a current source sub-circuit and a wave generator sub-circuit [4]. The current generator is a kind of current mirror whose current is controlled by FG-pFET. The current from the current generator sub-circuit is mirrored to the wave generator sub-circuit. The wave generator uses a switch (nmos) to control the charging and discharging function of the capacitance to generate a triangular wave. Then this triangular wave is transformed to spikes by the combination of invertors, which in turn feed to the clock input of the D flip-flop where, input of the D flip-flop

is shorted with the inverted output of the D flip-flop to generate the square wave from the spikes.
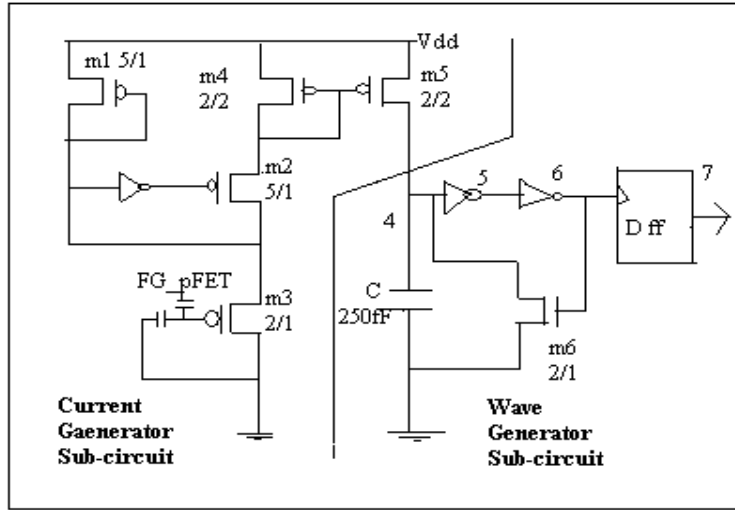

Figure 6: Proposed Clock generator circuit design simulated using T-Spice 0.35um CMOSS process.

In the current source sub-circuit, a FG-pFET is employed which is programmed by indirect programming as explained in the last section. The continuous ranges of resistance value are obtained to generate varying current which in turn mirrored to the wave generator circuit. Thus, continuous and finely tuned square wave is generated.

2.4 Design Methodology

The architecture consists of the two sub-circuits as shown in figure 6:

Wave generator circuit:

Voltage at the capacitor C depends on the current transferred from current mirror (i.e. current at node 4)

$$V_c = \frac{I \times \Delta t}{C} \tag{1}$$

Threshold of invertors, turn on the low impedance NMOS switch to discharge the capacitor to zero voltage. Hence, period of the triangular voltage waveform is:

$$T_c = \Delta t = \frac{C \times \Delta V_c}{I} \tag{2}$$

Current generator circuit:

A constant current source is built using current mirror. The current is generated from a PFET (source follower). A feedback circuit always stabilizes the voltage above floating-gate PFET (V1). Therefore, the floating gate PFET will decide the current.

$$I_{FG-PFET} = \frac{\mu C_{ox} W}{L} (V_{gs} - V_{th}) V_1, V_1 = V_{ds} \tag{3}$$

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This current is substituted to get the period of charging/ discharging of capacitor as:

$$T_c = \frac{C \Delta V_c L}{\mu C_{ox} W (V_{gs} - V_{th}) V_1} \qquad (4)$$

The threshold voltage of the floating-gate PFET decreases/increases with increase/decrease of floating gate voltage (to maintain transistor in linear region). Hence, the resistance of the transistor changes which in turn changes the period of charging/discharging of the capacitor.

$$T_c = R_{FG-PFET} \; C \times \frac{\Delta V_c}{V_1} \qquad (5)$$

However, the period of the output clock is two times of this period (Tc). Therefore the output square wave generated can be tuned by just varying the resistance of the floating-gate PFET.

2.5 Programming Methodology

Using floating gate transistor synapse as shown in figure 3 we have implemented the indirect programming of FG-pFET (M3 in figure 6). Injection requires > 1.5V drain-to-source voltage across the injection transistor (M_p in figure 3) while tunneling requires > 8V across the tunneling terminal for 0.35µm CMOS process.
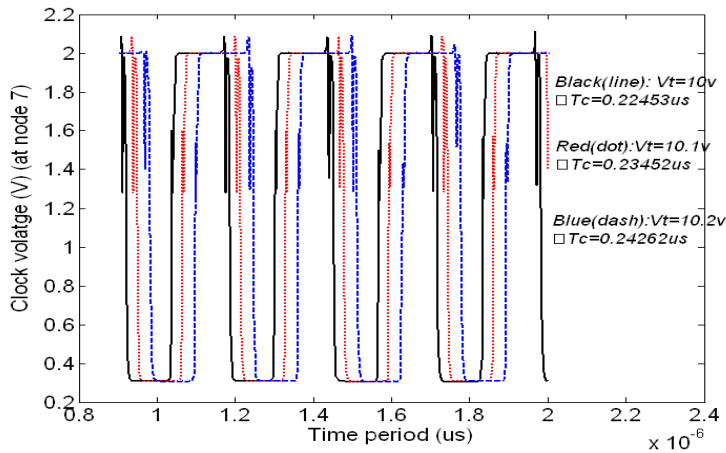

Figure 7: Variation in output clock with respect to tunneling voltage ($V_t=V_{tun}$)

The following two graphs will represent the change in output clock with change in tunneling voltage and with change in drain to source voltage in programmable PFET i.e. changes due to tunneling and injection respectively.

With increasing tunneling voltage, threshold voltage of floating-gate pFET (M_a in figure 3) increases and thus the resistance, this sequentially increases the time period of the output clock (as shown in figure 7). Whereas when the drain-to-source voltage of programmable PFET decreases, i.e. injection decreasing, threshold voltage increases and hence the period of the output clock (as shown in figure 8).
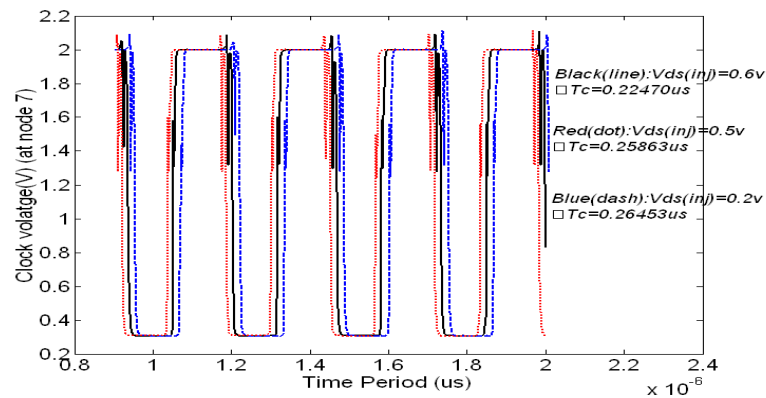
Figure 8: Variation in output clock with respect to injection voltage (Vds (inj) = $V_{d\_prog} - V_{s\_prog}$)

2.6 Simulated Results

Figure 9 first wave shows the voltage across the capacitor (V4) (node 4 in figure 6). It shows the charging and discharging of the capacitor using NMOS switch. Fig8 middle wave shows the invertors output (V6) (node 6). The input D of the flip flop is shorted with its complemented output. Thus, Figure 9 last wave showing the output square wave (output clock) obtained from the D flip-flop (V7) (node 7).

The square wave generated has been kept at low frequencies by adjusting the W&Ls of transistor used and by keeping high capacitor(C) value (250fF). As at high frequency like 20MHz very high distortion in the clock has been observed. While at low frequency 1 to 8 MHz clear and better clock is generated as shown in figure 9.
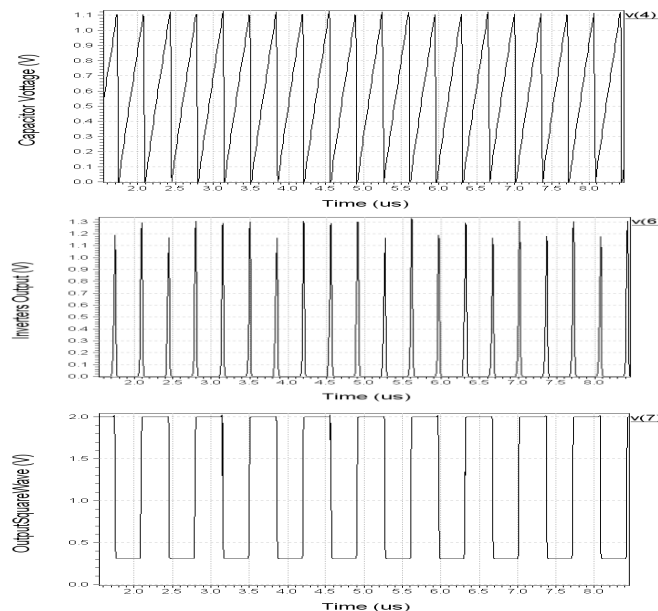

Figure 9: The simulated output waveforms (capacitor C output, inverters output and the D flip-flop output sequentially represented) obtained from proposed simulation model on T-spice 0.35um CMOSS process.

3. COMPARATIVE TRIMMING RESULTS

Table 1. Digitally trimmed resistor array RC oscillator inspired from [5]

Switching	Resistance (K)	Time Period (us)	Frequency (MHz)
1111111	47.8	0.15	6.67
0111111	75.9	0.18	5.55
0011111	99.98	0.2	5
0001111	120.4	0.22	4.76
0000111	137.89	0.26	3.33
0000011	154.26	0.3	2.63
0000001	167.83	0.38	2.63
0000000	175.3	0.45	2.22
1000000	151.02	0.3	3.33
1100000	125.35	0.25	4
1110000	105.35	0.2	5
1111000	88.62	0.19	5.124
1111100	70.34	0.18	5.55
111110	57.98	0.16	6.25

The simulation model of the previous work by [4] is approximated in T-spice under 0.35μm CMOS process. There is seven resistors array and each resistor switches ON/OFF using seven nmos switches. The 32k, 30k, 25k, 22k, 20k, 18k, 14k, 10k resistors are used and the corresponding impedance of the nmos switches are approximately 3.2k, 3.0k, 2.5k, 2k, 1.8k, 1.4k, 1k, respectively. The operating supply voltage is 2V. The equivalent resistance of the array changes with the switching of the nmos switches. At different switching conditions (almost 2^7 cases of switching is possible as shown in table 1) specific range of resistance occur which in turn generate specific ranged periodic clocks. Thus, clock generated has discrete range of frequencies as shown in figure10.

Whereas proposed Analog Field Programmable RC oscillator circuit using FG-pFET generates a continuous and finely tuned frequency ranged clock. With every change (decrease/increase) in floating gate voltage, resistance increase/decrease respectively as tabulated in table 2.

Table 2: Proposed clock generator using tunable FG-pFET resistor

FG Volt. (V)	Resistance (K)	Time Period (us)	Frequency (MHz)
-0.31762	53.37	0.2	5
-0.26421	61.17	0.21	4.7619
-0.17629	75.65	0.22	4.5454
-0.14521	85.92	0.231	4.3290
-0.08863	108.44	0.245	4.0816
-0.0606	118.94	0.25	4
-0.04759	127.45	0.258	3.8759
-0.00543	142.88	0.28	3.6363
0.02732	154.87	0.3	3.3333

0.03106	176.99	0.32	3.125
0.032451	182.76	0.33	3.0303
0.033759	184.35	0.34	2.9411
0.036823	186.12	0.35	2.8571
0.038071	190.45	0.38	2.6315

The frequency range is small (0.97MHz-4.04MHz) or (1.63MHz-5.5MHz) because FG-pFET resistor can vary to a certain limit. The floating gate voltage changes from -0.25V to 0.0027V at low range of resistances (45K to 130K) and FG voltage is -0.31 to 0.03 at high R (63.37kto180.45k). At low resistance the characteristics are linear as compared to at high resistances. Due to body effect and mobility degradation non linearity occurs when MOS transistor operates in triode region.
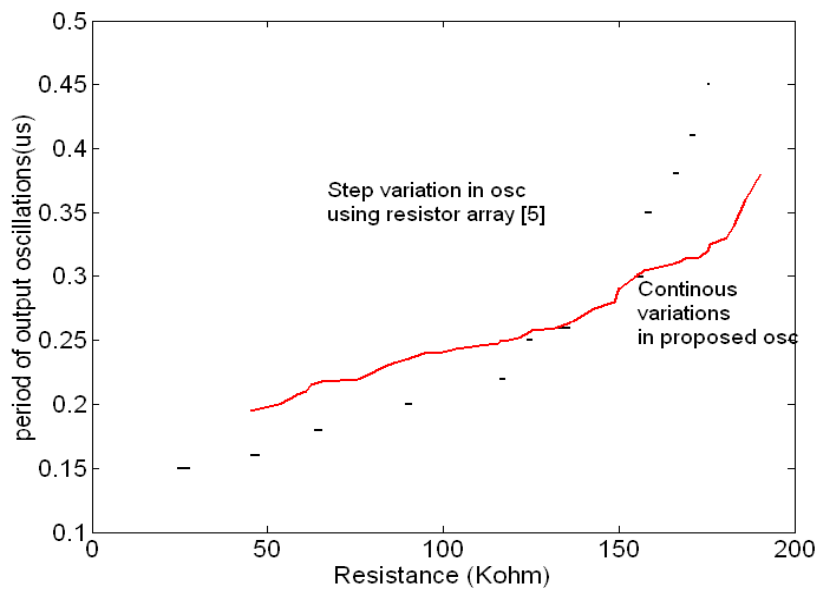

Figure 10: Period variation clock generated in digitally trimmed RC oscillator design inspired from [5] & continuous and finely tuned clock generated in proposed clock generator.

However, it gives very high resolution. Least possible change in floating gate voltage which can affect the output clock =.0003V. The resolution limit of programmability can be extended to 13-bit as mentioned in paper [1]. Thus, the number of changes in resistance value or trimming can be extended till (2^13=8192 cases). Hence, more accurate and fine-tuning of clock can be performed using proposed oscillator design.

4. THEORETICAL APPROXIMATION OF EFFECTIVE CHIP AREA

The chip area of the simulated model inspired from [5] is estimated. The transistor Effective Area= min poly-silicon width + 2*(min poly to contact spacing) + 2*(min contact size) +2*(min spacing from contact to active area edge). It can be approximated as poly-silicon gate area + 20% of this area. Thus, effective area of an nmos switch (for say 25k resistor w=2.7um, l=1um) = 2.7um*1um + 0.54um=3.24sq.um. However, in the paper [5] the impedance of the nmos switches is about 0.15ohm, i.e., (high w/l) nmos was considered (hence larger effective area). In

addition, the resistor (25k) will consume approximately 35.75um*35.75um chip area in 0.35um CMOS technology [18]. Thus, the effective area consumed by the resistors array comes out to be approximately 10224.5sq.um. Hence, the effective chip area consumed by the switching resistor array is 10259.48sq.um.

However, in the proposed RC oscillator circuit design two layers of poly-silicon are used. The effective area of the floating gate PFET synapse [19] is approximately 110um*93um when the floating gate PFET synapse is generated in 0.5um CMOS process technology. The area occupied by the capacitor (double poly layer) affect the total area of the circuit design. In addition, this Floating gate PFET synapse will implement in 0.35um CMOS technology. Therefore, the chip area occupied by the floating gate PFET will reduce further.

5. ON-CHIP PROGRAMMABILITY

The period of the output clock depends on floating-gate voltage, as shown in figure11. With fixed W and L specifications of floating-gate pFET, the circuit can be trimmed by just varying floating gate voltage of the floating gate pFET (by varying charge at the floating-gate) fabricated as a part of proposed design of clock generator. Thus, the generation of finely tuned frequency clock can be field programmable by simple tweaking charge at gate voltage of transistors.
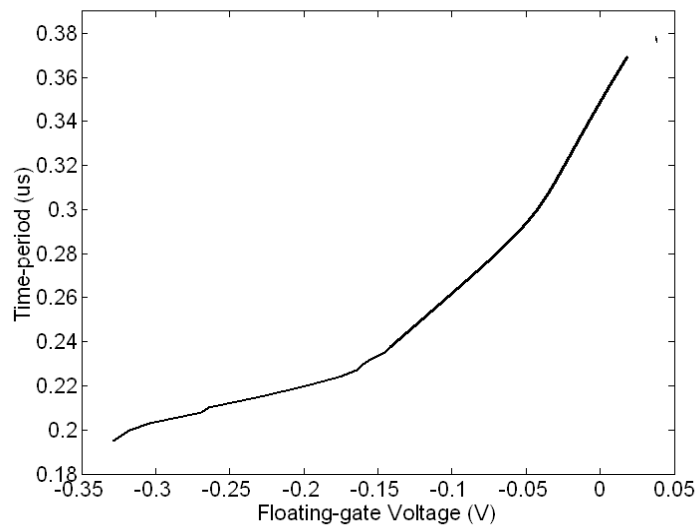

Figure 11: Variations in Clock period with change in floating gate voltage of tunable FG-pFET resistor in the proposed circuit.

6. TOPOLOGY TO WIDEN THE CLOCK RANGE

The proposed circuit generates very highly precise and continuous ranged clock as mentioned in last sections. However the range in which clock period can be programmed is small because floating gate voltage of FG-pFET resistor can vary to a certain limit. Thus, to increase this range place transistors with different W/L values in parallel with FG-pFET in the proposed circuit (figure 4.) with the common floating gate. For example, two transistor with w/l (2/1) and (2/0.8) are used independently then, range of resistances obtained respectively are (45K to 130K) and

(63.37kto180.45k); and hence clock obtained are (0.97MHz-4.04MHz) and (1.63MHz-5.5MHz) respectively. When placed parallel with common floating gate, the clock can be generated with frequency variation in the range between 0.97MHz-5.5MHz. As shown in Figure 12 the range of clock can be increased further by increasing more number of transistors at common floating gate.
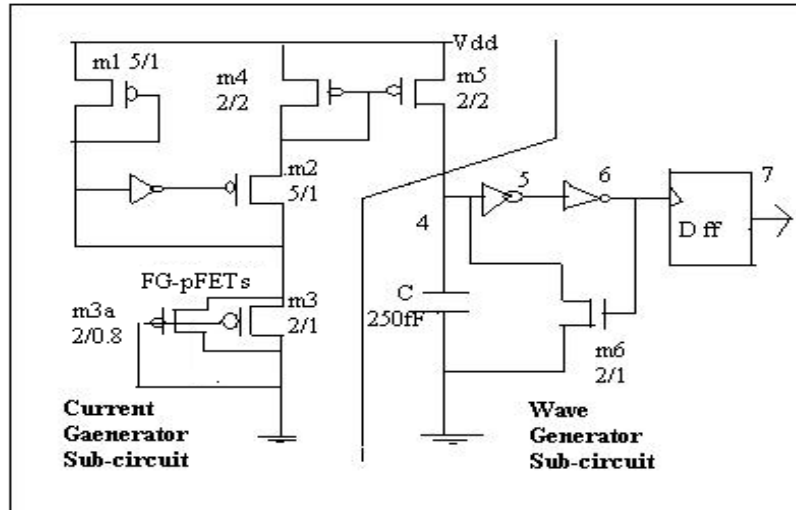

Figure 12: Circuit Diagram showing Topology to extend the frequency range of output clock

7. TEMPERATURE STABILITY

TABLE 3: Variations with Temperature

Temperature(°C)	Time period(us)	Frequency(MHz)
0	0.280982	3.56
10	0.279235	3.58
23	0.268301	3.73
25	0.265236	3.77
27	0.264132	3.78
30	0.259952	3.84
60	0.250887	3.98
80	0.240421	4.16

In proposed design the variation of FG-pFET resistor values varies with temperature as shown in figure 13. In addition, the frequency and time period change with temperature variation from 0 °C to 80 °C is shown in Table 3. The period varies at rate of 0.507ns/°C.
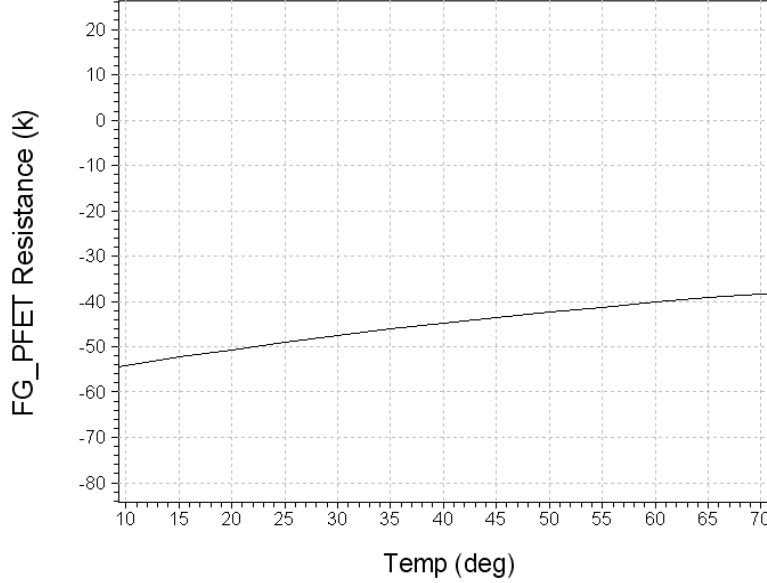

Figure 13: Plot representing FG-pFET resistance variation with change in temperature (about 0.1875K/°C)

The temperature dependence of the FG-pFET can be obtained using equation 4 and 5:

$$R_{FG\_PFET} = \frac{L}{\mu C_{ox} W (V_{gs} - V_{th})} \tag{6}$$

The temperature dependence of μ and V_T can expressed as $\mu = \mu_{no}(T/T_o)^{-m}$ and $V_T = V_{To} - \alpha_{VT}(T-T_o)$, where T_o is the reference temperature, and m is the positive constant that ranges from 1.5 to 2, and μ_{no} & V_{T0} are the temperature independent parameters. Also α_{VT} is in the range of 0.5 to 4 mV/°C[15]. Hence, the temperature coefficient of the FG-pFET can be expressed as

$$\frac{1}{R}\frac{\delta R}{\delta Y} = -\frac{1}{\mu}\frac{\delta \mu_{no}}{\delta T} + \frac{1}{V_g - V_T}\frac{\delta V_T}{\delta T} = \frac{m}{T} - \frac{\alpha_{VT}}{V_g - V_T} \tag{7}$$

where, $\frac{1}{\mu}\frac{\delta \mu_{no}}{\delta T} = -\frac{1}{m}$ & $\frac{\delta V_T}{\delta T} = -\alpha_{VT}$. As a result, the temperature coefficient of the FGPFET can be tuned by altering the effect of α_{VT} through the use of V_g. For desired temperature, T_d, and $V_g = \frac{\alpha_{VT}}{V_g - V_T}T_d + V_T$ the temperature coefficient of the FG-pFET can be set to zero at T_d. Hence, at specific temperature by adjusting the floating gate voltage temperature coefficient of the FG-pFET can be tuned to zero

8. CONCLUSION

The floating gate transistor using T-Spice, 0.35µm CMOS process, was successfully implemented as an efficient and accurate RC Oscillator circuit. FG-pFET resistors easily achieve high and precise (13bit) resistance values. FG-pFET resistor used in the circuit generates continuous and linear frequency range (1.63-5.5MHz at FG-pFET's R=110-500K or 0.95-4.04MHz at FG-pFET's R=63.87-183.84K).By switching multiple FG-pFET (with different W/Ls) at common floating gate, frequency range can be increased. With tweaking charges at the floating gate of FG-pFET, the frequency of the square wave can be finely and accurately tuned. The 13 bit of programming resolution can be obtained. It can also be operated at 1v supply voltage.

The circuit is adaptive to the change in temperature. By programming the FG-pFET the temperature coefficient can be tuned to zero value at any specific temperature. The size of the proposed circuit was relatively reduced when compared to other on-chip discrete trimming circuits. The proposed clock generator produces analog, highly precise and widely tuned square waveform which can find its application in wired or wireless network equipment which requires clock for highly accurate and high speed data transmission.

Table 4:Comparative Analysis of latest clock generators (RC oscillators)

Parameters	Proposed osc	S.Yu, et.al[5]	C.Ghidini, et.al.[6]	J.H Choi[7]	S.K.Kim, et.al [8]
Technique	FG-PFET	On-chip resistors array	5&3 bit C&R arrays	4-bit weighted-capacitors	OTFT transistors
Technology	0.35um	0.5um	0.25um	0.28um	Not mentioned
Min supply Voltage	1.8v	4.5v	2v	1.8v	-40v
Frequency Range	5.5MHz-1.63MHz	2.22MHz-6.67MHz[2]	30MHz-36MHz	1.6MHz-2.4MHz	140KHz
Oscillations behaviour	Continous	Discrete	Discrete	Discrete	Discerte
Frequency variation	0.507ns/°C	0.015ns/°C (0.5%)	2%	Not mentioned	Not mentioned
Temperature range	0°C -80°C	0°C-80°C	0°C-80°C	Not mentioned	Not mentioned
On-chip size	(110um×93um)[3]	130um×145um	444um×280um	240um×130um	Not mentioned
Programming resolution	13-bit (2^13=8192)[13]	7 bit (2^7=128)	8-bit	4-bit	Not mentioned

[1] simulated results

[2] from simulated model on 0.35um CMOS process

[3] Theoretically estimate

The proposed clock generator is being compared with the latest clock generators (RC oscillators) and noted in table IV. The proposed clock generator provides continuous and finely tuned (13bit resolution) clock. Comparable frequency range which can be extendable using

topology as explained before. Comparable clock period variation with temperature change which too can be compensated.

ACKNOWLEDGMENT

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