Design and Analysis of Multi V_t and Variable V_t based Pipelined Adder for Low Power applications

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ABSTRACT

Majority of Digital Signal Processing (DSP) applications require arithmetic blocks such as multipliers and adders for hardware realization of complex algorithms. Power consumption of arithmetic blocks need to be minimized by use of low power techniques. In this paper, an experimental setup is developed to identify the sources of power dissipation and remedies that can be adopted to minimize power dissipation in arithmetic blocks. Use of low power techniques such as Multi V_t, variable V_t, pipelining, geometry scaling and use of appropriate load capacitance have been used to reduce power dissipation. A 4-bit pipelined adder is designed and the power dissipation is reduced to 4.17μW from 9.6μW. The designed pipelined adder can be used for DSP applications.

KEYWORD

DSP, MAC, CMOS, Pipeline, Static and Dynamic

1.INTRODUCTION

With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that are required to be integrated on a single chip and total power consumption are increasing rapidly. Over the last two decades, low-power circuit design has become an important concern in digital VLSI design, especially for portable and high performance systems such as cellular phones, personal digital assistants (PDA), and military equipments. To further improve the performance of the circuits and to integrate more functions on a single chip, the feature size have to shrink. As a result, the power consumption per unit area grows. Another important reason for low-power circuit design is its reliability. The following sections discusses low power analysis of full adders, circuits to measure power in CMOS circuits & design of N-stage pipelined adder circuit for the MAC architecture. Analysis of power consumption in a sequential 4-bit adder of N-stage is presented by considering the power consumed by CMOS inverter and Full-Adder circuits. Technology variations and its impact on power are also discussed. There are various types of adders as reported in the literature.

Leighton [1] constructed N-bit adder (Carry-Ripple Adder) by cascading N full adders and the carry-out of bit i, C_i, is the carry-in to bit i+1. The delay of the adder is set by the time for the carries to ripple through the N stages, so the $T_{C->Cout}$ delay should be minimized. Killburn [2] constructed Manchester Carry Chain Adder, by switch logic to compute using propagate, generate and kill signals. The majority gate can be replaced with a switch network. Weinberger [3] proposed Carry Look Ahead Adder. It is similar to the carry-skip adder, but computes group generate signals as well as group propagate signals to avoid waiting for a ripple to determine if the first group generates a carry. It reduces the delay of the N-bit additions by computing in parallel. Tyagi [4] proposed a logic that reduces the size by factoring out the common logic and simplifying the multiplexer to a gray cell. This is sometimes called a carry-increment adder [5].

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The critical path delay is about the same as that of a carry-select adder because a multiplexer and XOR are comparable, but the area is smaller. Weinberger proposed Tree Adders, the delay of carry-look ahead adder becomes dominated by the delay of passing the carry through the look ahead stages. A multilevel tree of look ahead could be constructed to achieve delay that grows with log N. There are many ways to build the look ahead tree that offer trade-offs among the number of stages of logic gates, the maximum fan-out on each gate, and the amount of wiring between the stages. Here, 3 fundamental trees, the Brent-Kung, Sklansky and Kooge-Stone architectures are examined in the valency-2. Despite these costs, the Kooge-Stone tree is widely used in high performance 32-bit and 64-bit addresses. In summary, the basic three architectures represent cases that approach the ideal, but each differs in one respect. Brent-Kung has too many logic levels, Sklansky has too much fan-out and Kooge-Stone has too many wires. In this work, various types of adders are analysed for its power, delay and area. A pipelined 4-bit adder is designed using variable V_t and Multi V_t library. Experimental set up computing power is proposed and is modeled for analysis of adders. Section 2 discusses sources of power consumption in CMOS logic. Section 3 discusses 4-bit adder design and comparison of various adders. Section 5 discusses experimental set up for computing power dissipation in CMOS circuits and use of multi V_t and variable V_t cells for circuit design. Section 5 discusses design and analysis of pipelined adder and conclusion is presented in section 6.

2.SOURCES OF POWER CONSUMPTION IN CMOS

To measure the power consumption in CMOS circuits, the sources of power consumption should be known. Figure 1 presents the sources of power consumed in a CMOS circuit. As mentioned in Figure 1, the major part of the power consumption is Active and Standby powers. The active power consists of two components, Capacitive or Dynamic power and Short Circuit power.

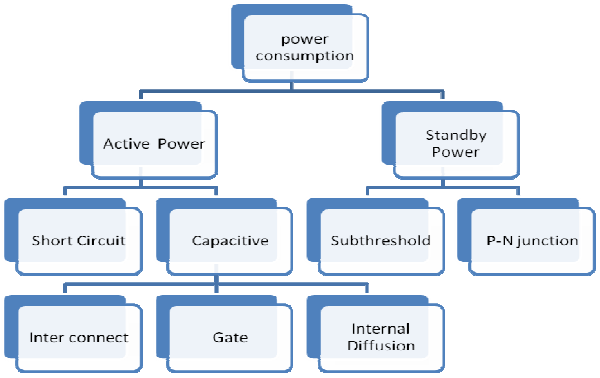

Figure 1: Sources of Power Consumption in CMOS [6]

A detailed discussion of sources of power consumption is discussed in [7], leakage power is one of the dominating factor at nanometer geometries. Efforts to reduce power are discussed in [8]. This paper addresses design and analysis of low power adders. Simulators such as H-Spice or Cadence tools are used to analyze CMOS circuits, simulators give average power alone. In order to estimate Switching power, short circuit power and leakage power, an experimental setup is required. Hence, in the next section, experimental setup for power analysis is carried out.

3.FOUR-BIT ADDER

An adder is the most commonly used arithmetic block in the Central Processing Unit (CPU) of a microprocessor, a Digital Signal Processor (DSP), and even in a variety of ASICs. In a DWT processor, adder is one of the important building blocks, required to compute the DWT coefficients of input signal. Multiplier used in a DWT processor also requires adder to add the partial products. Hence, design and analysis of adder is considered in this section. Speed and optimization of power of an adder is significant, to improve the overall performance of the system. But an adder also experiences the power-delay trade off. That is, its power dissipation increases with reduction in delay and vice versa. There are various architectures for adder design. 4-bit adders can be of different types. Some of those are Carry look Ahead Adder, Ripple Carry Adder, Carry Save Adder, Carry Select Adder. There are different ways to realize a full adder and are mentioned in Table 1. From the table 1, it is very clear that the Mux based full adder implementation consumes very less power and also has minimum delay. The Mux based full adder has a delay of 0.0012ns. This implies that, when the input is applied, it takes 0.0012ns to produce the output. Figure 2 shows the power consumption of all the seven adders. From the results obtained, mux based adder is the best in terms of low power. Thus, MUX based adder is used for low power applications.

Table 1: Full Adder Design Comparisons [15]

Full adder using	No. of transistors	Area (μm^2)	Power (µw)	Delay(µs)
Only NAND	36	507.592	0.01293	0.00987
Only mux	22	324.225	0.0001459	0.0012
Ex-OR,AND,OR	30	408.127	3.58	0.0065
Conventional CMOS logic	28	387.548	0.0328	0.01055
Quasi domino	23	375.124	0.01645	0.00767
Static and dynamic	22	367.721	46.65	0.0109
Ex-OR & AND	30	413.402	3.58	0.0065

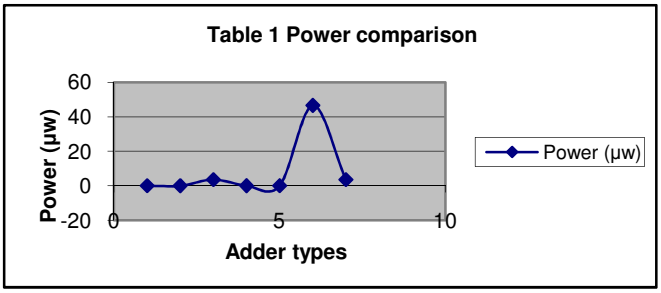

Figure 2: Power consumed by the adders

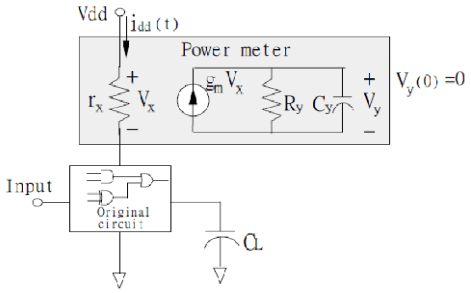

Figure 3: Power meter and Original circuit [12]

4. EXPERIMENT SETUPS FOR P_{SC}, P_{SWITCH} AND P_{LEAK} OF AN INVERTER

Figure 2 shows the experimental setup for power analysis. Device under test is applied with input and the output is captured across a load capacitor. V_{dd} and Gnd are the power sources to which the original circuit is connected. In order to measure power, a power meter circuit is introduced between V_{dd} and original circuit. This power meter circuit is used to analyze power dissipation of original circuit.

4.1. Calculation of P_{sc}

The short circuit power dissipation occurs when the output state is changing i.e., when both transistors are ON at the same time. P_{short} *is* defined as

$$\int_0^T V_{dd} * i_{dd(short)}(t)dt \quad (1)$$

where $i_{dd\ (short)}(t)$ is the instantaneous short circuit current at time *t,* the short circuit time *T* is defined as the duration of presence with a path from V_{dd} to ground. With a proper choice of the g_m, the voltage $V_y(t)$ *across* the capacitor C_y will read the average power consumption P_{avg}. So, the short circuit power dissipation $P_{short}= P_{avg} – P_{load}$ by assuming P_{static} is equal to zero. The table 2 represents values of P_{sc} for different widths and lengths of PMOS and NMOS. From the table, it is found that as the geometries of the transistors are varied, short circuit power also varies. Short circuit current is maximum for smaller geometries of transistors. From the values shown, it is observed that as length decreases, power increases, and as width decreases power decreases.

Table 2: P_{sc} for Varying width and length

V_{dd}(V)	f(MHz)	Length(µm)		Width (µm)		P_{sc} (µW)
		NMOS	PMOS	NMOS	PMOS	
3.3	100	0.18	0.18	0.36	0.72	3.7
3.3	100	0.14	0.18	0.36	0.72	4.5
3.3	100	0.18	0.16	0.36	0.72	3.96
3.3	100	0.18	0.18	0.33	0.72	3.5

Table 3: P_{leak} for various widths and lengths of NMOS and PMOS

V_{dd} (V)	f(MHz)	Length(µm)		Width (µm)		P_{leak} (Watt)
		NMOS	PMOS	NMOS	PMOS	
3.3V	100	0.18	0.18	0.36	0.72	6.40E-20
3.3V	100	0.14	0.18	0.36	0.72	6.90E-20
3.3V	100	0.18	0.16	0.36	0.72	6.75E-20
3.3V	100	0.18	0.18	0.33	0.72	6.60E-20

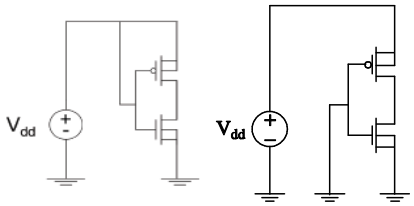

Figure 3: Setup for Static power when i/p is high and low

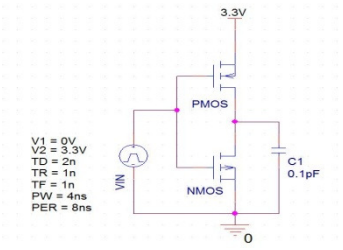

Figure 4: Setup for calculating Pswitch

Figure 3 represents the setups for calculating the leakage power in a CMOS inverter [13]. According to the setup, the P_{leak} can be calculated by taking the integrals of I(PMOS) and I(NMOS) in the intervals of half of the total time period, taking their average and multiplying with $V_{dd.}$ assuming C_L=0.01pf.

4.2 Calculation of P_{leak}

Table 3 represents values of P_{leak} for various widths and lengths of both the transistors. We observe that, as the length decreases, power increases and as width decreases, power decreases.

4.3 Calculation for P_{switch}

The setup for calculating the switching power for an inverter is shown in the Figure 4. To calculate the switching power, the current across the PMOS transistor is taken and integrated along the interval of half of total time period of the input signal. This current $I_{switching}$ is multiplied with the V_{dd} to get the power $P_{switch.}$.

Table 4: P_{switch} for various frequencies

V_{dd}(V)	f(MHz)	Length (µm)		Width (µm)		P_{switch}(Watt)
		NMOS	PMOS	NMOS	PMOS	
3.3V	100	0.18	0.18	0.36	0.72	2.15E-15
3.3V	150	0.18	0.18	0.36	0.72	3.18E-15
3.3V	33	0.18	0.18	0.36	0.72	3.18E-16
3.3V	25	0.18	0.18	0.36	0.72	3.14E-16
3.3V	20	0.18	0.18	0.36	0.72	3.12E-16

Table 5: P_{switch} for various C_{load}

V_{dd}(V)	f (MHz)	C_{load} (pF)	Length (µm)		Width (µm)		P_{switch} (Watt)
			NMOS	PMOS	NMOS	PMOS	
3.3V	100	0.01	0.18	0.18	0.36	0.72	2.00E-15
3.3V	100	0.1	0.18	0.18	0.36	0.72	1.06E-15
3.3V	100	100	0.18	0.18	0.36	0.72	3.60E-14
3.3V	100	10	0.18	0.18	0.36	0.72	3.06E-14
3.3V	100	0.0001	0.18	0.18	0.36	0.72	2.58E-14

Tables 4 and 5 represents the values of P_{switch} for various switching frequencies and capacitive loads for NMOS and PMOS transistors respectively. From the tables 4 and 5, it is observed that there is increase in power with increase in frequency and $C_{load,}$ and this proves the theoretical observation. Based on the analysis carried out, two low power techniques have been selected to reduce power dissipation. Discussions on these techniques are presented in the next section.

4.4. Calculation for Multi-V_t and Variable-V_t

As the switching activity poses more amount of power consumption, it is quadratically proportional to supply voltage. These transistor switching speeds require downscaling of the transistor threshold voltage, with the supply voltage reduction. Threshold voltage scaling leads to leakage power dissipation due to increase in the sub-threshold leakage current. There are three main sources for leakage current:

- Source/drain junction leakage current
- Gate direct tunnelling leakage
- Sub-threshold leakage through the channel of an OFF transistor

The common methods used to reduce the threshold leakage are:

- Leakage reduction through input vector control
- Leakage reduction by increasing threshold voltage
- Leakage reduction by gating the supply voltage

The concept of multi-V_t and variable V_t comes under the power reduction method using threshold voltage technique.

4.4.1 Multi V_t results

The table 6 represents the P_{leak} for various geometries of transistors in CMOS inverter (low V_t), assuming C_{load}=0.01pf. The table 7 represents the P_{leak} for various C_{load} and table 8 for various V_{dd}.

4.4.2 Variable-Threshold CMOS (VTCMOS) circuits

This technique usually requires twin-well or triple-well CMOS technology in order to apply different substrate bias voltages to different parts of the chip. The tables 9 and 10 represent the power consumed by the circuit for various frequencies and various V_{dd} respectively. Based on the analysis carried out in this section, low power adder circuits are designed and analyzed for its performances. Next section discusses full adder design and analysis.

Table 6: P_{leak} values for various geometries

V_{dd} (V)	f (MHz)	PMOS		NMOS		P_{leak} (Watts)
		Length (µm)	Width (µm)	Length (µm)	Width (µm)	
3.3	100	0.18	0.72	0.18	0.36	8.09E-18
3.3	100	0.14	0.72	0.14	0.72	1.16E-16
3.3	100	0.15	0.72	0.15	0.72	9.40E-17
3.3	100	0.18	0.72	0.18	0.5	1.64E-16
3.3	100	0.18	0.72	0.18	1.5	4.12E-16

Table 7: P_{leak} values for various C_{load}

V_{dd} (V)	C_{load} (pF)	f (MHz)	PMOS		NMOS		P_{leak} (Watts)
			Length (µm)	Width (µm)	Length (µm)	Width (µm)	
3.3	10	100	0.18	0.72	0.18	0.36	3.09E-17
3.3	0.001	100	0.18	0.72	0.18	0.36	2.18E-18

Table 8: P_{leak} values for various V_{dd}

V_{dd} (V)	f (MHz)	PMOS		NMOS		P_{leak} (Watts)
		Length (µm)	Width (µm)	Length (µm)	Width (µm)	
1.8	100	0.18	0.72	0.18	0.36	2.75E-18
5	100	0.18	0.72	0.18	0.36	8.18E-18

Table 9: Power consumed by VTCMOS for various frequencies

V_{dd}(V)	f(MHz)	PMOS		NMOS		P_{avg}(Watts)
		Length(µm)	Width(µm)	Length(µm)	Width(µm)	
3.3	100	0.18	0.72	0.18	0..72	2.15E-003
3.3	166	0.18	0.72	0.18	0.72	2.36E-03
3.3	200	0.18	0.72	0.18	0.72	4.12E-03

Table 10: Power consumed by VTCMOS for various V_{dd}

V_{dd} (V)	f (MHz)	PMOS		NMOS		P_{avg}(Watts)
		Length (µm)	Width (µm)	Length (µm)	Width (µm)	
3.3	100	0.18	0.72	0.18	0.36	6.09E-04
1.8	100	0.18	0.72	0.18	0.36	1.18E-03

Table 11: Comparison of power dissipation for various full adders

One-bit Full adder	Number of transistors	Power dissipated in PMOS transistors (pWatts)	Average power dissipation (µ Watts)
2-mux hybrid	14	154.1124	8.0606
Majority gate	28	99.9256	3.5590
6-mux	32	303.8668	70.5690
Mirror adder	28	110.4568	63.0500

Table 12: Comparison of delays for various full adders

One-bit Full adder	Number of transistors	Sum delay (p seconds)	Carry delay (p seconds)
2-mux hybrid	14	52.3160	88.8560
Majority gate	28	195.0000	117.1400
6-mux	32	69.9850	74.2320
Mirror adder	28	202.2000	115.2800

Table 13: Dynamic power dissipation for full adder by varying W_n/W_p ratio

W_n/W_p	Power dissipated in PMOS(p Watts)	Total power dissipation due to PMOS & NMOS (p Watts)	Average power dissipation (µ Watts)
0.5	-93.623	154.1124	20.348
1.0	-106.2179	179.3005	21.269
2.0	-112.1156	189.1309	1.8683

Table 14: Short circuit power dissipation for full adder by varying W_n/W_p ratio

W_n/W_p	$I(C_{load})$ amps	$I(V_{dd})$ amps	Short-circuit current(amps)	Short circuit power dissipation(Watts)
0.5	131.31f	140.36f	9.05f	16.29f
1.0	129.31f	169.80f	40.49f	72.882f
2.0	134.99f	165.39f	30.40f	54.72f

Table 15: Leakage power dissipation for full adder by varying W_n/W_p ratio

W_n/W_p	Input a (volts)	Input b (volts)	Input c_{in} (volts)	Number of transistors in cutoff	Leakage current (n amps)	Leakage power consumption (n Watts)
0.5	0	0	0	12	1.463	2.6334
1.0	0	0	0	12	0.555	0.999

4.5. Analysis of Sources of Power Dissipation in a Full Adder

The table 11 and table 12 shows comparison of four basic full adder circuits. The initial values are C_{load}=0.075pf, V_{dd}=1.8V, t_d=0.1ns, t_r=0.2ns, t_f=0.2ns, PW=10ns, T=20ns.

In this section, power analysis for full adder is carried out based on variations in device geometries, operating frequency and reference voltage. Table 13 to Table 18 presents the results carried out for power analysis. Width of PMOS and NMOS transistors are varied by keeping length constant.

5. PIPELINED ADDER FOR LOW POWER

Adders play a vital role in many complex logic circuits where performance and power are of main concerns. The MAC architecture used in DWT use the N-bit addition operation, in particular, 4-bit for the present problem. Given, a sequential 4 bit adder stages, it should be modified to a pipelined 4-bit adder stages by appropriate design and simulation.

5.1. Pipelined 4-bit adder Architecture

The Figure 5 represents the logic function of input vector and output vector. Both the input and the output vectors are sampled through register arrays, driven by a clock signal. The maximum input-to-output propagation delay t_{pmax} of this block is equal to or less than $T_{clk}=1/f_{clk.}$ Let C_{load} be the total capacitance switched every clock cycle. C_{total} consists of the capacitance switched in the input register array, Capacitance switched to implement the logic function and Capacitance switched in the output register array.

The power consumption of this structure can be found as $P_{reference}= C_{total} * V_{dd}^2 * f_{clk}$ (2)

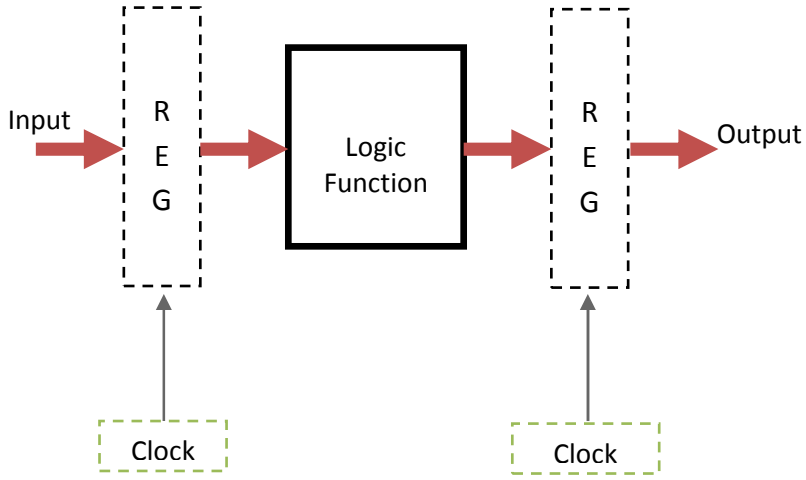

Figure 5: Single stage implementation of logic function

The N-stage pipelined structure for implementing the same logic function will be partitioned into N successive stages, and N-1 stages have been introduced apart from initial registers to create the pipeline. The delay of partitioned stages is given in equation 3.

T_p(pipelined stage) = $t_{p,max}$(input-to-output)/N = T_{clk} (3)

The dynamic power consumption of N-stage pipelined structure with the same functional throughput as single-stage structure is approximated by equation 4.

$$P_{pipeline} = [C_{total} + (N-1)C_{reg}] * V_{dd}^{2}{}_{,new} * f_{clk} \quad (4)$$

where C_{reg} represents the capacitance switched by each pipeline register. The pipeline reduction factor achieved in an N-stage pipeline structure is given in equation 5.

$$\frac{P_{\text{pieline}}}{P_{\text{reference}}} = [C_{\text{total}} + (N-1)C_{\text{ref}}] * V_{dd,new}^2 * \frac{f_{clk}}{[C_{\text{total}} * V_{dd}^2 * f_{clk}]} = \left[1 + \left((N-1) * \frac{C_{\text{ref}}}{C_{\text{total}}}\right)\right] * \frac{V_{dd,new}^2}{V_{dd}^2} \quad (5)$$

If the logic function block is replaced with 4 stages of pipeline structure, running at the clock frequency of 20MHz, the delay of each stage is increased by a factor 4 without losing the data. Assuming C_{ref}/C_{total}=0.1, power reduction factor is found as 0.2. Thus, by inclusion of the stages at the same clock frequency, and by reducing the supply voltage from 5V to 2V, the pipelining concept saved 80% of power. The theoretical values of power consumption by varying V_{dd}, C_{load}, number of stages are tabulated in the table 20. It is observed that the power is reduced to 36% when V_{dd} is reduced from 5V to 4V, and power reduced by 64%, when V_{dd} is reduced from 5V to 3V.

Table 16: Power consumption of Pipelined structure for varying V_{dd}

V_{dd} (Input supply voltage) (V)	V_{dd}^2 (V)	C_{ref} (Assumption)	C_{total} (Total capacitance)	No. of stages	f_{Clk}	Total power dissipation(µW)	Power reduction %
5	25	0.2	2	4	20	1300	0
4	16	0.2	2	4	20	832	-36
3	9	0.2	2	4	20	468	-64

Table 17: Power consumption of Pipelined structure for varying C_{load} (C_{total})

V_{dd} (Input supply Voltage) (V)	V_{dd}^2 (V)	C_{ref} (Assumption)	C_{total} (Total Capacitance)	No of Stages	f_{clk} (MHz)	Total Power Dissipation (µW)	Power Reduction %
5	25	0.2	2	2	20	1100	-15.38462
5	25	0.2	4	2	20	2100	61.538462
5	25	0.2	6	2	20	3100	138.46154

Table 18: Power consumption of Pipelined structure for varying number of stages

V_{dd} (Input supply voltage)	V_{dd}^2	C_{ref} (Assumption)	C_{total} (Total capacitance)	No. of stages	f_{Clk} (MHz)	Total power dissipation (µW)	Power reduction %
5	25	0.2	2	3	20	1200	-7.69231
5	25	0.2	2	4	20	1300	0
5	25	0.2	2	5	20	1400	7.692308

Table 19: Power consumption of Pipelined structure for V_{dd} =1.8V and V_{dd}=2.5V

V_{dd} (Input supply voltage)	V_{dd}^2	C_{ref}(µf) (Assumption)	C_{total} (Total capacitance)	No. of stages	f_{Clk} (MHz)	Total power dissipation(µW)
2.5	6.25	0.1	1	4	62.5	507.8125
1.8	3.24	0.1	1	3	62.5	243

The table 21 represents the calculation of power for various C_{load} and it is observed that the power is reduced to 15% when C_{load} is 2pf and power increased to 61.5%, when C_{load} is increased to 4pf and power increased to 138.5%, when C_{load} is increased to 6pf. The table 22 represents the calculation of power for varying number of stages and the observation is that, as the number of stages increases, the power consumed by the circuit also increases. From the theoretical calculations, the pipelined adder can be designed for V_{dd} = 1.8V and 2.5V and load as 0.1µf.

5.2. THREE STAGE PIPELINED ADDER SEQUENCE

Figure 6 represents the three stage pipelined adder, that is considered for the practical simulations and results are compared with theoretical values.

In this work, three stage pipeline adders are considered for analysis purpose alone. This analysis will help in understanding the importance of pipelined architecture and its impact in power reduction. As shown in the figure, there are three adders cascaded, three registers are introduced in between the adders to make the design pipelined. Inputs that are applied from the left are added with inputs provided from the top registers and are taken to the next stage. Simulation results are presented and discussed in detail.

The ripple carry adder is constructed by cascading Full Adder (FA) blocks in series as in Figure 7. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage

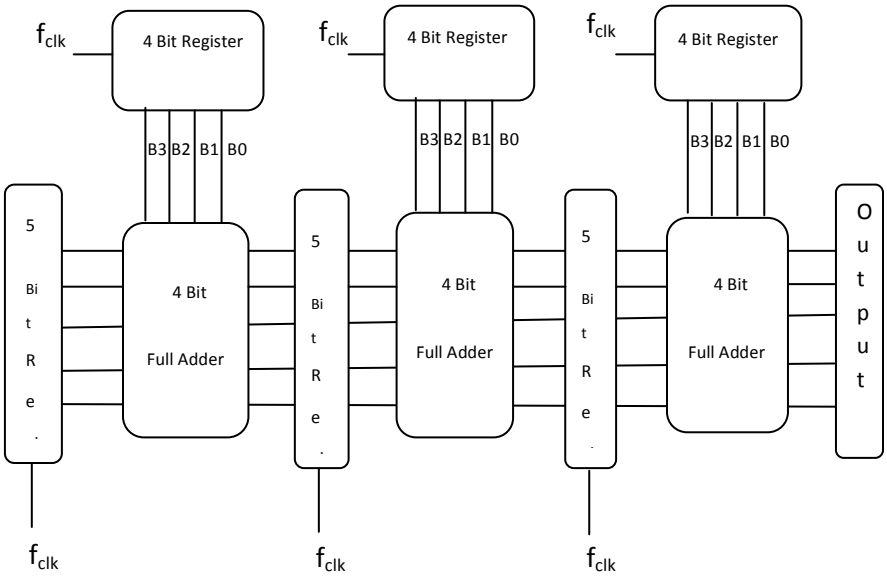

Figure 6: Three-stage pipelined adder

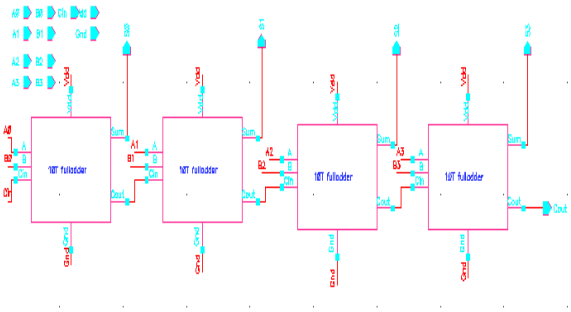

Fig 7 Four Bit Ripple Carry Adder

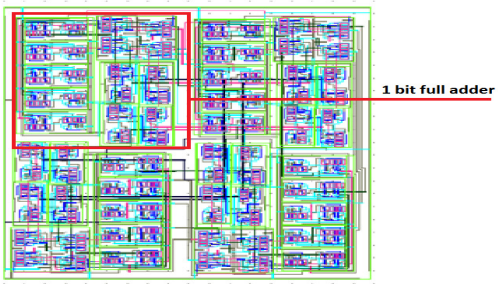

Fig 8 Layout of 4-Bit Adder

Four bit ripple carry adder is used as the building block for the pipelined adder. The Figure 8 shows the layout diagram of such a four bit full adder. The pipelined 4- bit adder circuit consists of registers made of D-flip-flops and three stages of 4-bit adders made of full adders.. From the

table 20, it is observed that the power dissipation for C_{ref} = 0.1µf is 465.75µW, and the practical value of the power dissipation through simulation is 341µW. From Table 21, it is observed that the power dissipation for C_{ref} = 0.2µf is 627.75 µW.

Table 20: Power dissipation for three stage pipelined adder for C_{ref} =0.1µf

V_{dd} (Input supply voltage)	V_{dd}^2	C_{ref} (Assumption) µf	C_{total} (Total capacitance)	No. of stages	f_{Clk} MHz	Total power dissipation (µW)
1.8	3.24	0.10	2.10	3.00	62.50	465.75

Table 21: Power dissipation for three stage pipelined adder for C_{ref} =0.2µf

V_{dd} (Input supply voltage)	V_{dd}^2	C_{ref} (Assumption)	C_{total} (Total capacitance)	No. of stages	f_{Clk}	Total power dissipation (µW)
1.8	3.24	0.20	2.70	3.00	62.50	627.75

Table 22: Power, Area and Delay of 1-bit, 4-bit full adder and 4 bit Pipelined adder

PARAMETERS	1 bit adder	4bit adder	4 bit pipelined adder
POWER (in watts)	8.1951E-9	9.633E-6	4.172 E-6
AREA (in μm^2)	82	334.4	9345
DELAY (in sec)	1.234E-10	7.8267E-12	5.248E-9

Table 22 presents the comparison of 4-bit adder and pipelined 4-bit adder. Pipelined 4-bit adder consumes less power and also has very less delay compared with 4-bit adder, but the area is affected.

6. CONCLUSION

An experimental setup is developed and modeled using Cadence Virtuoso to analyze the three sources of power dissipation. Inverters, NAND, NOR, 2:1 MUX and full adder circuits are analyzed for power dissipation. Various full adder circuits have been designed, modeled and analyzed for its power dissipation. 2-Mux circuit requires 14 transistors and occupies less area as compared with other full adder circuits. Majority gate based full adder requires 28 transistors and consumes less power. For low power applications, Majority gate based full adder can be used. A three stage pipelined adder is designed with C_{load} of 2pf. The pipelined adder power dissipation is reduced by 15% compared to adder without pipeline (7.8ns). The designed pipelined adder can be used to realize multipliers.

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