OPTIMIZATION TECHNIQUES FOR SOURCE FOLLOWER BASED TRACK-AND-HOLD CIRCUIT FOR HIGH SPEED WIRELESS COMMUNICATION

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ABSTRACT

Since *the current demand for high-resolution and fast analog to digital converters (ADC) is driving the need for track and hold amplifiers (T&H) operating at RF frequencies. A very fast and linear T&H circuit is the key element in any modern wideband data acquisition system. Applications like a cable-TV or a broad variety of different radio standards require high processing speeds with high resolution. The track-and-hold (T&H) circuit is a fundamental block for analog-to digital (A/D) converters. Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Having a wideband and precise acquisition system is a prerequisite for today's trend towards multi-standard flexible radios, with as much signal processing as possible in digital domain. This work investigates effect of various design schemes and circuit topology for track-and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise.*

KEYWORDS

Track and Hold Circuit, Low Power Consumption, Slew Rate, Peak Power, Sampling Switch, Flash Analog to Digital Converter

1. INTRODUCTION

Track and hold circuit is the fundamental block for analog to digital (A/D) converters. Track and hold circuit is inserted in front of a comparator array of a flash A/D converter to keep comparator's input voltages constant while the comparators are settling their output voltage levels. Track and hold architecture can be classified into two classes (fig.1): open-loop and closed-loop architecture [1]-[5].

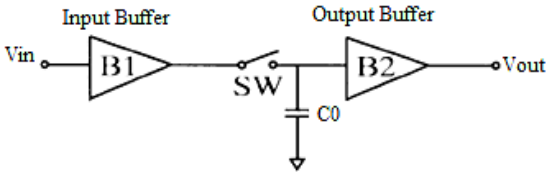

Figure 1a. Open-loop T/H

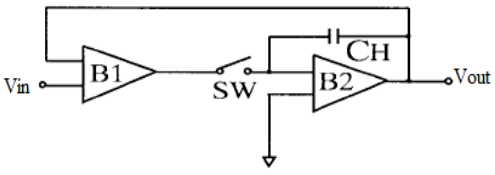

Figure 1b. Closed-loop T/H

The open loop T/H circuit is suitable for high precision but not for high speed. Most CMOS T/H circuits proposed/implemented so far employ closed-loop architecture to obtain better than 8 bit accuracy. However closed loop architectures suffer from relatively lower sampling frequency and higher power consumption as compared to open-loop architecture [6]. Open-

loop architectures tend to consume lower power and work at high sampling frequencies than closed-loop ones. Open-loop architectures have been used in high-speed ADCs [3][4].

Source-follower-based T/H circuit has been optimized with respect to linearity, noise, and speed and power consumption.This paper investigates effect of various design schemes and circuit topology for track-and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise. Superior speed & acceptable linearity of source-followers makes it promising candidate for the purpose of this work.

2. SAMPLING SWITCHES FOR T/H

The sampling network consists of a sampling switch (M_{sw}) and a hold capacitor (C_s) to store the value of sampled signal during the hold mode. During the tracking phase, the combination of the switch and the capacitor forms a first-order RC network, the time-constant of which sets the maximum achievable sampling frequency. The speed of sampling network appears not to be a serious limitation in this work because as will be seen the chosen operating frequency is far less than the time-constant of the switch network and is basically limited by other parts of the circuit [15].

The noise contribution due to the sampling network is dependent on the sampling capacitance value and the width of the switching transistor. In addition to the noise added by the switch, the non-linearity due to the signal-dependent behaviour of the switch can degrade the overall linearity of the T/H circuit.

2.1. Single MOS Switch

The maximum output voltage that an NMOS transistor can deliver is approximately equal to V_{dd}-$V_{th.}$

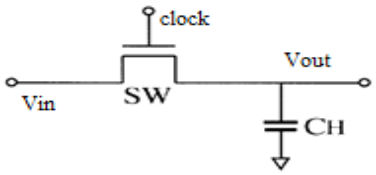

Figure 2. Single MOS sampling switch

The on-resistance of a long-channel MOS device operating in the linear (triode) regions is given by:

$$R_{ON} = \frac{1}{\mu C_{OX} \frac{W}{L}(V_{gs} - V_{th})} \qquad (1)$$

From the above expression it is clear that the resistance of NMOS switch is non-linear that is approaches infinity when Vin approaches Vdd-Vth,which is the upper limit of the NMOS transistor [10].

2.2. Transmission-Gate Switch

To circumvent the above problem with a varying switch resistance the benefit of NMOS for low input voltages and the PMOS for high input voltages can be Utilized.it is done simply by connecting them in parallel and thereby forming a transmission gate.

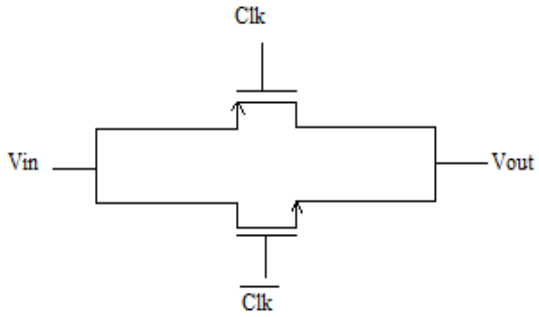

Figure 3. Transmission gate sampling switch

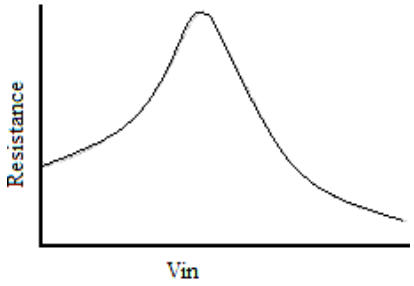

Figure 4. On-resistance of the transmission gate

NMOS transistor shows the non-linear characterisitcs for high voltages. This is why NMOS transistor works poorly for high voltages. A PMOS transistor on the other hand , is known to work poorly for low voltages and rather for high voltages.

The transmission-gate-switch (NMOS-and-PMOS transistor connected in parallel) might be the solution to the problem faced by single NMOS and PMOS switches. As seen in figure, the resistance for the transmission-gate-switch is much linear that is why transmission-gate-switches can be wise choice to get acceptable linearty and large output gain [18].

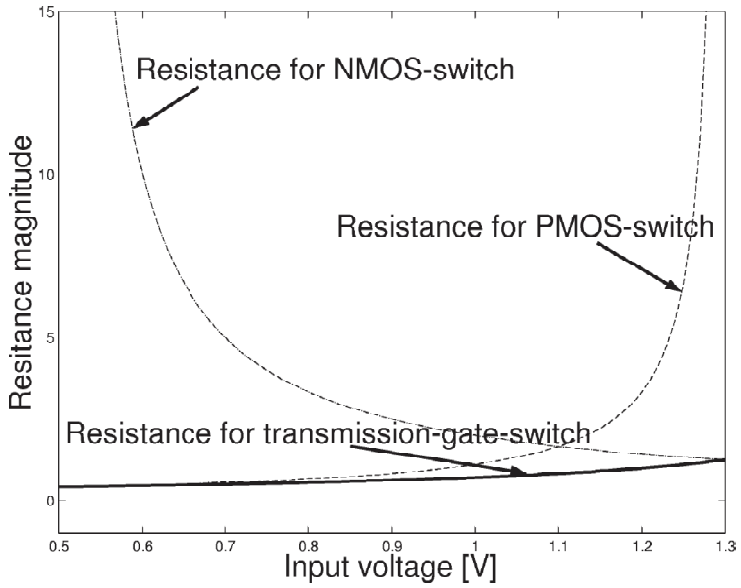

Figure 5. Resistance magnitude of sampling switches

3. CONVENTIONAL T/H USING SOURCE FOLLOWER

Source follower was used in this work to drive the load capacitance of the T/H stage. The active devices in the source-follower contribute to the noise in both the track and hold modes of

operation. The noise of these devices mainly due consists of channel thermal noise and gate flicker noise.

3.1. Analysis of T/H Circuit Using NMOS Sampling Switch

A conventional source follower T/H circuit basically consists of input, output buffers, a switch and a sampling capacitor. An output buffer is usually used to charge and discharge the input capacitances of following comparators.

A T/H circuit has two operation phases named “track phase” and “hold phase”. During a track phase the switch is shorted and V_{out} becomes equal to V_{in}. On the other hand, during a hold phase the switch is opened and the T/H circuit keeps its output voltage equal to the value at end of track phase. A required hold time of a T/H circuit is usually decided by a settling time of the following comparators since the comparators must settle their output voltage during a hold time [9].

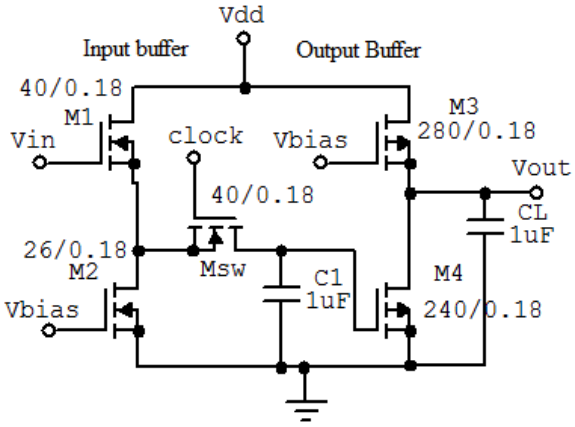

Figure 6. Single ended conventional T/H

Table 1. Design specification of T/H

Power supply voltage	1.8 v
Maximum input signal frequency	500 MHz
Sampling frequency	1GHz
Maximum output voltage swing (Ain)	1 Vp-p
Resolution	6 bit
Load capacitance (C_L)	10pf
Input offset	0.8 v
CMOS technology	0.18µm

An input voltage represented by

$$V_{in} = A_{in} \sin(\omega_{in} + \varphi_{in}) \qquad (2)$$

Where A_{in} is equal to the maximum input voltage given by the specifications and ω_{in} is set to 2π ($f_s/2$). f_s means its sampling frequency.

3.2. Analytical Modeling of Conventional T/H Circuit

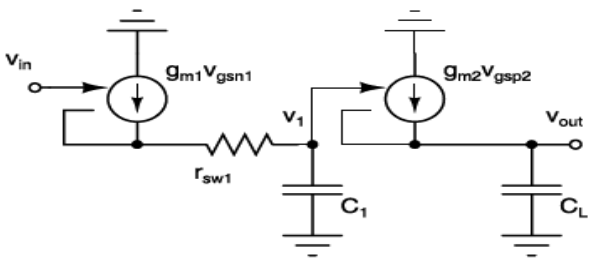

Figure 7. Small signal model of conventional T/H

A Transfer functions from V_{in} to V_1 , and from V_1 to V_{out} is represented by

$$T_1(s) = \frac{v_1}{v_{in}} = \frac{1}{1 + sC_1\left(\frac{1}{g_{m1}} + r_{sw1}\right)} = \frac{1}{1 + s\tau_1} \quad (3)$$

$$T_2(s) = \frac{v_{out}}{v_1} = \frac{1}{1 + sC_L\left(\frac{1}{g_{m2}}\right)} = \frac{1}{1 + s\tau_2} \quad (4)$$

Respectively, where τ_1 and τ_2 is time constant which is defined by

$$\tau_1 = C_1\left(\frac{1}{g_{m1}} + r_{sw1}\right) \quad , \qquad \tau_2 = \frac{C_L}{g_{m_2}} \quad (5)$$

$$g_{m_2} = \frac{C_L}{\tau_2} \quad , \quad \frac{1}{g_{m1}} = \frac{\sqrt{\alpha_n}}{\sqrt{\alpha_n} + \sqrt{\beta_n}} \frac{\tau_1}{C_1} \quad , \qquad r_{sw1} = \frac{\sqrt{\beta_n}}{\sqrt{\alpha_n} + \sqrt{\beta_n}} \frac{\tau_1}{C_1} \quad (6)$$

Whereα_n, β_n is defined as follows

$$\alpha_n = \frac{(V_{gs} - V_{T_n})g_{m1}}{2} \quad , \qquad \beta_n = \frac{L_{sw1}^2 f_s V_{dd}}{\mu_n(V_{gs} - V_{tn})} \frac{1}{r_{sw1}} \quad (7)$$

On the assumption that an acceptable gain error at the input buffer of the T/H circuit is e_1 an optimum τ_1 must satisfy

$$|T_1(j\omega_{max})| = \frac{1}{\sqrt{1 + \omega_{max}^2 \tau_1 2}} = 1 - e_1 \quad (8) \qquad \text{and } v_{out}(t) = L^{-1}\left[\frac{1}{1 + s\tau_2}.V_1(s)\right] \quad (9)$$

Where $V_1(s)$ is the output of the input buffer of conventional T/H circuit.

Table 2. Hspice smulation of conventional T/H circuit

Vout	1.46 v
Average power consumption	76.94 mw
peak power over a cycle	89.08 mw
Slew rate	89.64 mv/ns
Track time	0.92 ns
Hold time	0.76 ns

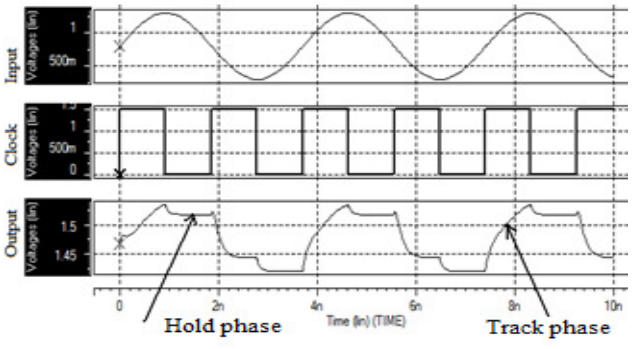

Figure 8. Output waveform for conventional T/H

3.2.1 Noise Analysis of Conventional T/H Circuit

Table 2. Noise results of conventional T/H

Total output noise voltage	6.945e-01 Sq V/Hz=833.37p V/Rt(Hz)
Transfer function value (Vout/Vin)	1.64882n
Equivalent input noise at Vin	505.43604m
Total equivalent input noise voltage	1.14265K V

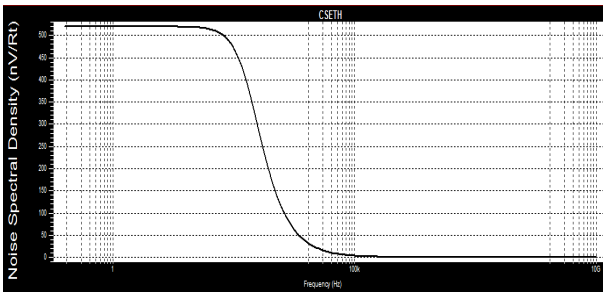

Figure 9. Output noise of conventional T/H

3.3. Analysis of T/H Circuit using Transmission-Gate Sampling Switch

Here NMOS sampling switch is replaced with Transmission-gate sampling switch. As discussed earlier that On-resistance of Transmission-gate shows the linear characteristics hence linearity in output waveform is expected this is confirmed by the HSPICE simulation result. It improves the linearity but at the cost of area overhead. We require one more clock to use transmission-gate sampling switch

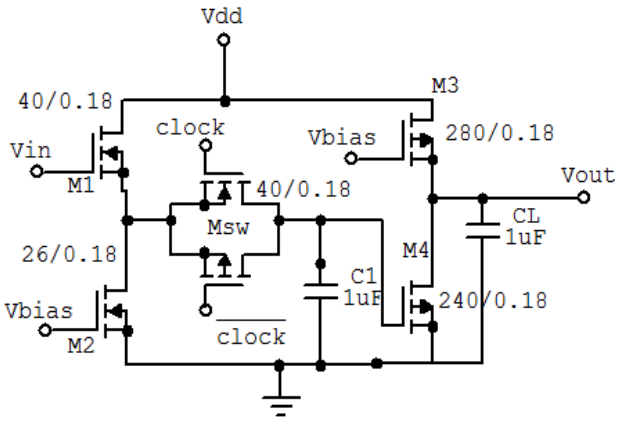

Figure 10. Conventional T/H using Transmission-gate sampling switch

Table 3. Hspice simulation results for conventional Track-and-Hold using Transmission-Gate

V_{out}	1.57v
Average power consumption	78.33 mw
Peak power over a cycle	90.91 mw
Slew rate	110.48 mv/ns
Track time	0.92 ns
Hold time	0.81 ns

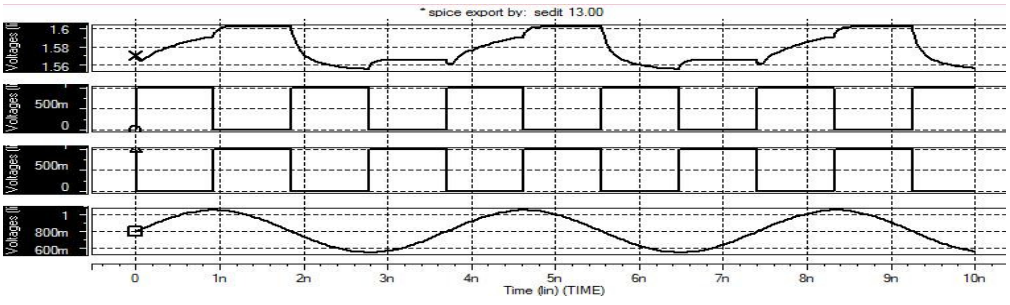

Figure 11. Output waveform for T/H using Transmission-gate sampling switch

From the output waveform it is clear that V_{out} is linear in behaviour.

3.3.1 Noise Analysis of Conventional T/H Circuit using Transmission-Gate

Table 4. Noise results of conventional T/H using Transmission-Gate

Total output noise voltage	4.473e-019 Sq V/Hz = 668.83807p V/Rt(Hz)
Transfer function value (Vout/Vin)	1.06742n
Equivalent input noise at Vin	626.59340m
Total equivalent input noise voltage	1.43876K V

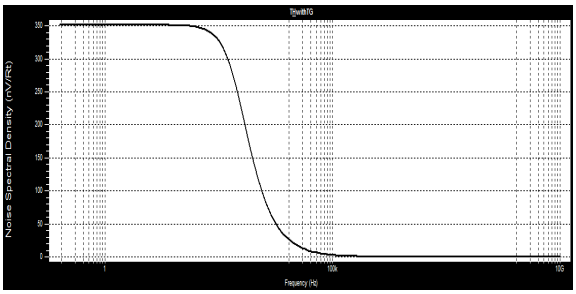

Figure 12. Output noise of conventional T/H using Transmission-Gate

3.4. Analysis of Pseudo-differential T/H circuit

The T/H circuit is implemented in a pseudo-differential fashion to suppress even–order nonlinearities as well as offset and common-mode noise. The biasing branch of the source-follower is, however, shared between the two half circuits to cancel the noise contribution of biasing devices.

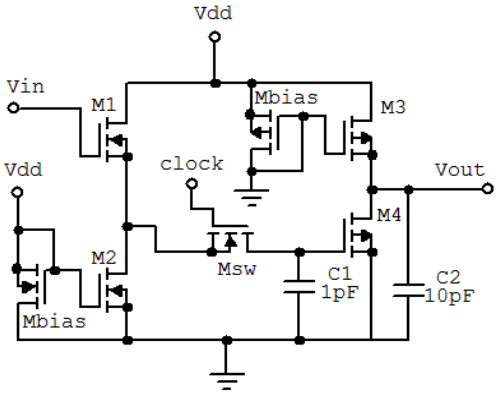

Figure 13. Pseudo-deferential T/H

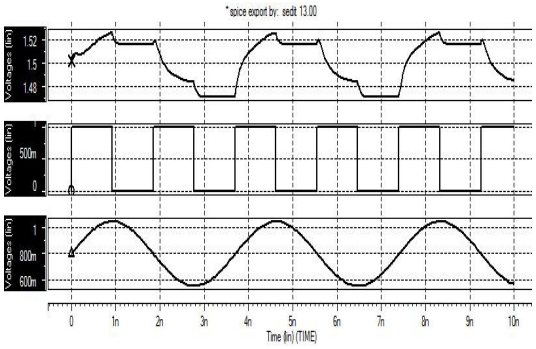

Figure 14. Output waveform for pseudo-deferential T/H

Table 5. Hspice Simulation Result of Pseudo-Differential T/H

Vout	1.50 v
Average power consumption	93.64 mw
Peak power over a cycle	103.5 mw
Slew rate	135mv/ns
Track time	0.88 ns
Hold time	0.77 ns

3.4.1 Noise Analysis of Pseudo-differential T/H circuit

Table 6. Noise results of conventional T/H using Transmission-Gate

Total output noise voltage	5.674e-019 Sq V/Hz =753.29254p V/Rt(Hz)
Transfer function value (Vout/Vin)	1.04183n
Equivalent input noise at Vin	723.05050m
Total equivalent input noise voltage	1.63118K V

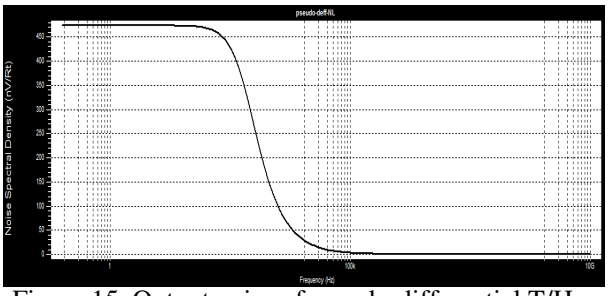

Figure 15. Output noise of pseudo-differential T/H

3.5. Analysis of fully-differential T/H circuit

Figure 16. shows that input and output buffers of conventional Track-and-Hold circuit are modified in differential manner so that common mode noise could be suppressed. This architecture suppress the noise upto 60-70% as compared to conventional one but at the cost of power consumption and area overhead.

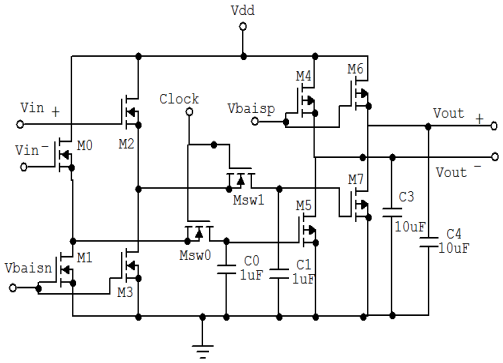

Figure 16. Fully-deferential T/H

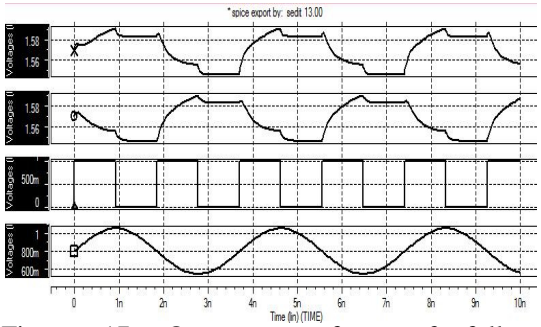

Figure 17. Output waveform of fully-deferential T/H

Table 7. Hspice simulation results of fully-differential T/H

Vout	1.56 v
Average power consumption	162 mw
Peak power over a cycle	182 mw
Slew rate	181 mv/ns
Track time	0.92 ns
Hold time	0.81 ns

3.5.1 Noise Analysis of fully-differential T/H circuit

Table 8. Noise results of fully differential T/H circuit

Total output noise voltage	2.981e-019 Sq V/Hz = 546.01522 p V/Rt(Hz)
Transfer function value (Vout/Vin)	0
Equivalent input noise at Vin	0
Total equivalent input noise voltage	0 V

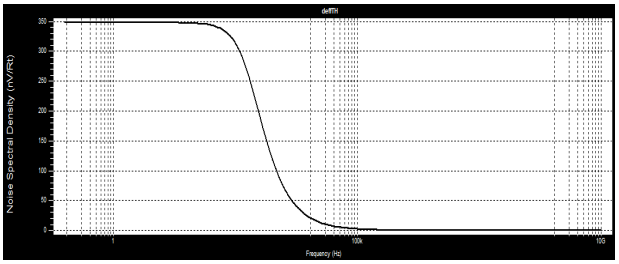

Figure 18. O/P Noise of fully-differential T/H

3.5. Analysis of Two-Stage T/H using Conventional T/H Circuit

In two-stage T/H circuit, two conventional T/H circuits are connected in cascade. The output of the first T/H serves as the input to the next T/H. If the input voltage of a T/H circuit is kept constant during its track phase, only one of charging or discharging is occurred in a track phase. In this case the output voltage of the T/H circuit settles monotonously into the constant voltage from the beginning of the track phase and its hold time must be as long as possible. This reduction of the tracking time results in a low power consumption. In order to apply such a constant voltage to the T/H circuit an additional small T/H circuit is inserted in front of the original T/H circuit as shown in Figure 19. Inverting and non-inverting clocks are applied to the two switches, Msw0 and Msw1, respectively so that the two T/H circuits act reciprocally.

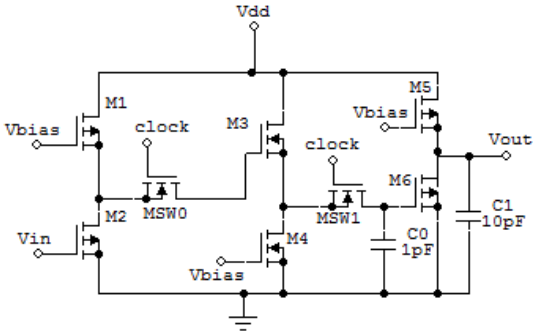

Figure 19. Two stage T/H circuit

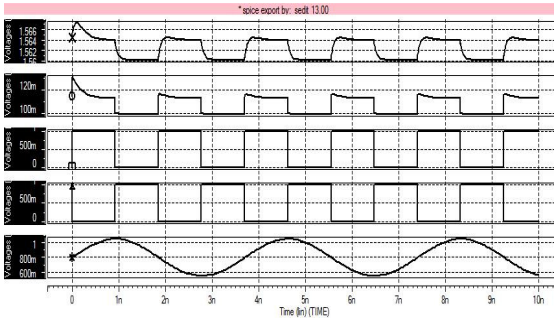

Figure 20. Output waveform of two stage T/H circuit

When the second T/H circuit is in a track phase the first T/H circuit is always in a hold phase whose output voltage is constant. The first T/H circuit also charges and discharges its load capacitance during a track phase, however, it can operate very fast because its load capacitance is much smaller than that of the conventional T/H circuit. The first T/H circuit consumes very low power when the first T/H circuit and the conventional one have the same operation speed. The output voltage of the first stage is applied to the second T/H circuit. When the second T/H circuit is in the track phase, its input voltage is always constant because the first T/H circuit is already in the hold phase. Therefore, its output voltage approaches to the final value directly and it's settling time decreases drastically [8].

Table 9. Hspice simulation results of two-stage T/H

Vout	1.59 v
Average power consumption	64.30 mw
Peak power over a cycle	69.80 mw
Slew rate	37 mv/ns
Track time	.16 ns
Hold time	0.62 ns

HSpice simulation result (fig.20) shows that track-time in output waveform for two stages T/H circuit is reduced drastically while the hold time in output waveform is increased.

3.5.1 Noise Analysis of two-stage T/H circuit

Table 10. Noise results of two-stage T/H

Total output noise voltage	7.473e-020 Sq V/Hz =273.36864p V/Rt(Hz)
Transfer function value (Vout/Vin)	115.94659f
Equivalent input noise at Vin	2.35771K
Total equivalent input noise voltage	734.89198K V

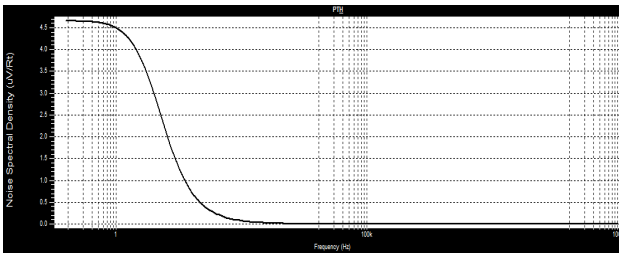

Figure 21. Output noise of two-stage T/H

3.6 SLEW RATE LIMITATION OF SOURCE FOLLOWER T/H CIRCUIT

When input signal is such that it demands an o/p response is faster than the specified value of slew rate (SR), non linear distortion will occur due to slew rate limitation.

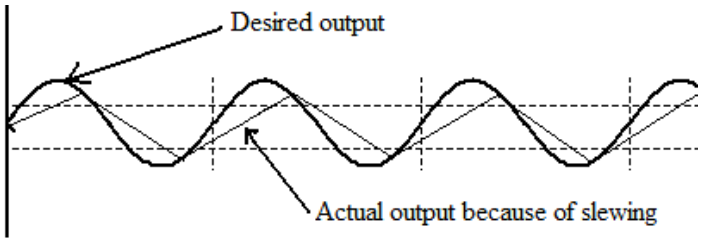

Figure 22. Slew rate distortion due to slewing

Slew rate limitation cause non linear distortion when I/P is sinusoidal

$$V_{in} = A_{in}\sin(\omega_{in}t+\Phi)$$

$$(dV_{in}/dt)_{max} = A_{in}\omega_{in} \qquad (10)$$

Thus the maximum occurs at zero crossing of I/P sinusoidal. If $A_{in}\omega_{in}$ exceeds the slew rate of the input buffer the output waveform will be distorted. Output cannot keep up with this large rate of change of the input sinusoidal at its zero crossing & hence source follower slews [7].
There is a specific frequency f_M called the full-power bandwidth at which output voltage of the source follower begins to show distortion due to slew-rate limitation

$$A_{in}\omega_{in} = \text{SR (slew rate)} \qquad F_M = SR/2\,\pi A_{in} \qquad (11)$$

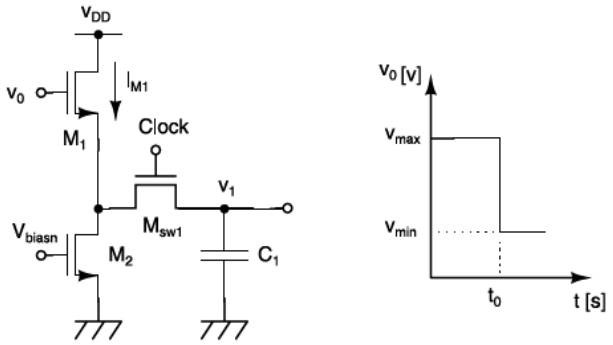

Figure 23. Single stage of source follower T/H

When the step voltage whose amplitude is larger than (Vgs – V_T) is applied to the single stage of source follower T/H circuit, M_1 goes into the cut-off region at t = t_0. When M1 is cut off, its load capacitor is discharged by a constant current I_{M2}. The slew rate is limited to I_{M2}/C_1.
The output voltage during the slewing can be represented by

$$V_1 = V_{max} - V_{gs1} - \frac{I_{M2}}{C_1} \qquad (12)$$

Where V_{gs1} is the gate-to-source bias voltage of M_1 On the assumption that an on-resistance of M_{sw1} is adequately small, this slewing continues as

$$t_{slew} = \frac{C_1}{I_{M2}}(V_{max} - V_{min} - V_{gs1} + V_T) \qquad (13)$$

3.7 COMPARISON OF POWER

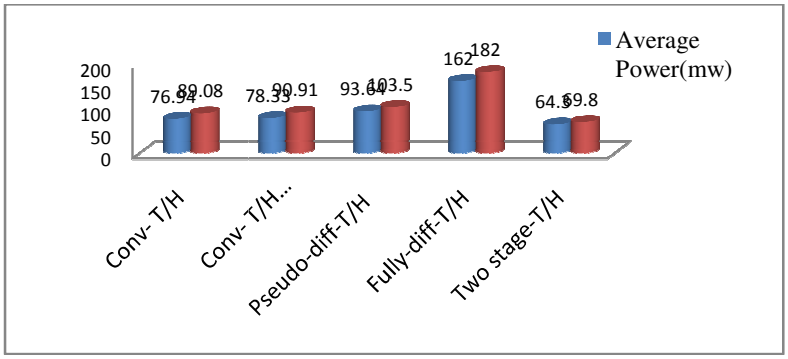

Figure 24. Comparison of power consumption

Figure 24. Shows that average power consumed by two stage Track-and-Hold circuit is minimum.

3.8 COMPARISON OF O/P NOISE

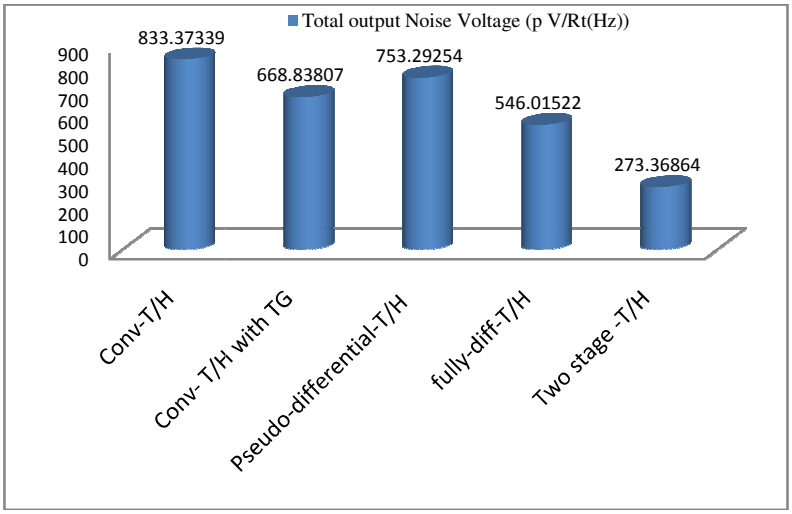

Figure 25. Comparison of O/P noise voltage

Graph shows that the o/p noise voltage of two stage Track-and-Hold circuit is minimum.

3.9 COMPARISON OF SLEW RATE

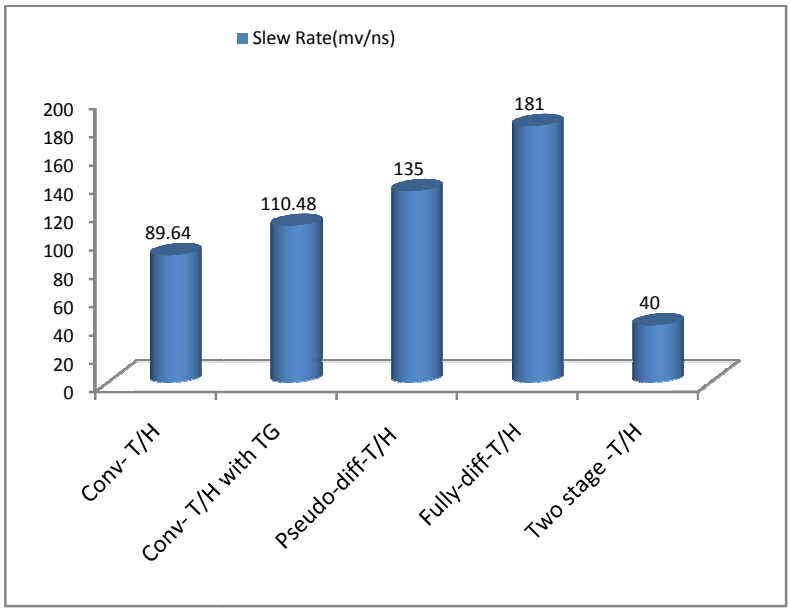

Figure 26. Comparison of Slew Rate

From figure 26. It is observeed that the slew rate of the fully-differential Track-and-Hold circuit is maximum.

3. CONCLUSIONS

It is found that the on-resistance of transmission-gate-switch (NMOS and MOS-transistor connected in parallel) is much more linear. Later on, NMOS switches are replaced with transmission-gate-switch.

Two stage Track-and-Hold circuit shows 16.42% decrease in power consumption as compared to conventional Track-and-Hold circuit. Further, track time of two-stage T/H circuit is found to be .16(ns) which is minimum among all Track-and-Hold circuits. Hence two-stage structure is fastest among all designs. Fully differential Track-and-Hold circuit shows the highest slew rate (181 mv/ns) while two-stage T/H shows minimum slew (40 mv/ns). There is an 8.90% increase in V_{out} of two stage Track-and-hold circuit as compared to conventional Track-and-Hold circuit. Two-stage T/H circuit shows 67.19% reduction in output noise voltage as compared to conventional Track-and-Hold circuit. Two Stage T/H Circuit based on source follower buffers mitigates the problem of power consumption, large track time and noise but at the cost of small value of slew rate. A unity-gain buffer is capable to achieve high slew rates in both positive and negative directions. By sensing the drain current of the common-drain device in an NMOS source follower, the extent of slewing could be achieved. So the future work of this dissertation would be implementation of high slew rate Track-and-Hold circuit by using an enhanced slew rate source follower buffers [7].

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