# IMPACT OF STRAIN AND CHANNEL THICKNESS ON PERFORMANCE OF BIAXIAL STRAINED SILICON MOSFETs

Neha Sharan[#1], Ashwani K.Rana [*2]

[#] Department of Electronics and Communication, National Institute of Technology, Hamirpur
Hamirpur (H.P)-177005, India

[1]nehasharan11@yahoo.com
[2]ashwani_paper@gmail.com

***ABSTRACT***

*In this paper the impact of strain and channel thickness on the performance of biaxial strained silicon MOSFET with 40 nm channel length has been analyzed by simulation in TCAD Sentaurus Simulator. With the increase in the mole fraction of germanium at the interface of the channel region, the strain in the silicon channel increases and with it the mobility of the carriers increases and thus the drain current increases. The mole fraction in this paper is varied from 0 to 0.3. Other than mobility, the increase in strain also shows improvement in other performance parameters. The impact of variation in channel thickness on the functionality parameters of the MOSFET has also been analyzed. The channel thickness cannot be increased more than the critical thickness and therefore, in this paper the thickness is varied from 2nm to 20 nm. It is observed that beyond 10nm the performance improvement gets saturated and therefore the critical thickness for the channel of this structure is 10nm..*

***KEYWORDS***

*Biaxial Strained, Channel Thickness, Drain current, Mobility & Mole Fraction.*

## 1. INTRODUCTION

Strain Engineering is the most recent technology adopted to improve the performance of the device significantly. Application of strain results in alteration of the energy band of the device [1]. Strain results in increase in curvature of the hole bands and splitting of the electron bands [2]. These factors results in increase in mobility of the device thus, improving the functioning of the device. Introduction of strain in the channel region also improves the drain current, subthreshold swing and DIBL (drain induced barrier lowering), electron velocity and transconductance of the device overall improving the functionality of the device. Though scaling which is the present trend adopted to improve performance also results in increase in drain current but the drawback with scaling is that with decrease in device dimensions, threshold voltage also decreases and results in increase in subthreshold swing and DIBL. Scaling leads to introduction of short channel effects in the channel. Therefore, strain technology is considered as a viable option to improve performance of the device.

There are various methodology adopted to induce strain in the channel of the MOSFET. Depending on the methodology adopted different types of strain get induced that can be either

compressive strain or tensile strain. Compressive strain results in increase in just hole mobility but tensile strain results in increase in both electron and hole mobility [3]. Therefore tensile strain is preferred over compressive strain. Moreover depending on the strained lattice direction in the channel Uniaxial or Biaxial strain gets induced.

In this paper Biaxial tensile Strained Silicon MOSFET of 40nm channel length and 2nm oxide thickness has been taken and the impact of strain and channel thickness on the performance of the device in terms of mobility, subthreshold swing, DIBL and drain current has been observed. Strain is varied with variation in mole fraction of the germanium at the channel interface. The mole-fraction in this paper is varied from 0.05 to 0.3. Channel thickness is also a factor which varies the strain induced in the channel. If the channel thickness is increased to a greater extent then the performance of the device gets saturated. The performance of the device is observed for a channel thickness varying from 2nm to 20nm. Analysis is being done in Sentaurus TCAD tool.

In this paper Section 2 describes the device structure and design, Section 3 describes the simulation set-up used to simulate this structure, Section 4 deals with structure modelling, and Section 5 describes the results obtained and its discussion. Finally, Section 6 presents the conclusion.

## 2. DEVICE DESIGN

Figure 1. depicts the structure of Biaxial Strained Silicon MOSFET.

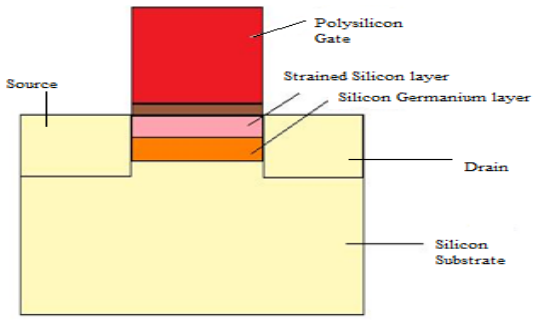


Figure 1. Biaxial Strained Silicon MOSFET

The MOSFET structure is made in Sentaurus device editor. A Silicon Substrate is taken and in the channel region this Silicon layer is replaced with a relaxed Silicon Germanium layer of 10nm thickness on which Strained Silicon layer of 10 nm thickness has been placed. The oxide layer is taken of thickness 2nm on which poly gate of 40nm is placed. The source drain region is implanted to a junction depth of 25 nm.

## 3. SIMULATION SETUP

Figure 2. shows the sentaurus simulator schematic of the MOSFET with doping profile.

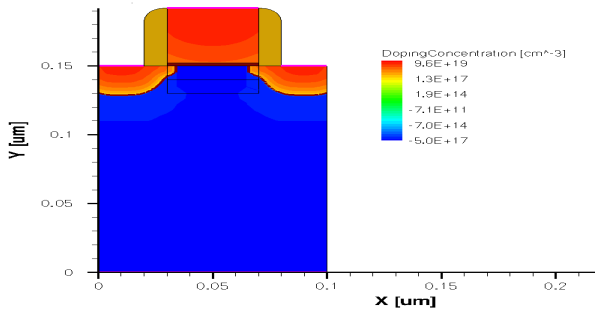


Fig. 2. Schematic cross-section of Strained MOSFET with doping concentration

The doping concentration in silicon S/D region is assumed to be graded due to diffusion phenomenon with a peak value of $1x10^{19}$ $cm^{-3}$ and $1x10^{17}$ $cm^{-3}$. The doping of the silicon S/D region is assumed to be very high for negligible silicon resistance near the channel. The body region is doped with boron concentration of $1e+17cm^{-3}$ The poly-silicon doping has been taken to be $1x10^{20}$ $cm^{-3}$ at the top and $1x10^{20}$ $cm^{-3}$ at bottom of the poly-silicon gate i.e. interface of oxide and silicon.

The strain is induced in the structure by varying the mole fraction of Silicon Germanium layer as well as channel thickness. The mole fraction in this structure is varied from 0.05 to 0.3 and the thickness of the strained silicon channel is varied from 2nm to 20nm. The MOSFET parameters are taken to have a threshold voltage of 0.101 V.

The simulation of the device is performed by using Sentaurus design suite [4], with drift-diffusion, density gradient quantum correction and advanced physical model being turned on. The SRH and Auger model are used to capture the recombination of carriers in device. SRH model is adopted to account for the generation and recombination of the carriers which also play a role in drive current. The strain induced mobility models are used during simulation of the structure in order to capture the influence of strain on carrier transport. Piezoresistance model and mole fraction variation is adopted to realise effects of varying strain and channel thickness in the MOSFET.

## 4. THEORETICAL STRUCTURE MODELLING

Figure 3. shows the lattice mismatch phenomenon between Silicon and Silicon-Germanium layer resulting in strain generation in channel region.

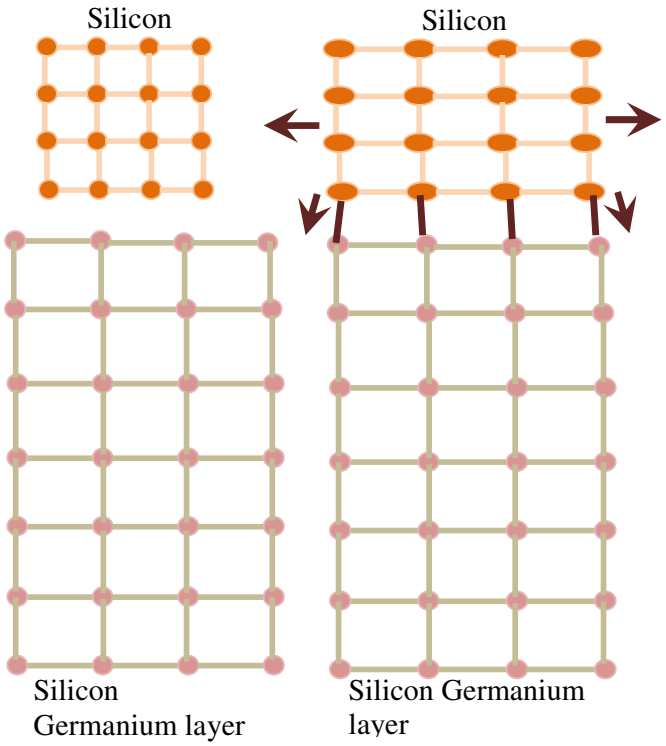


Figure 3. Strain Generation through lattice mismatch in Silicon Lattice

It is depicted in the figure that the lattice constant of silicon germanium is greater than silicon and therefore when silicon is placed over it, in order to get aligned, the silicon layer gets strained. The increase in mole fraction at the interface of channel region results in increase in strain in the channel. In order to maintain strain in the channel region we require a relaxed $Si_{1-x}Ge_x$ layer and therefore, the mole-fraction should not be increased beyond 0.5. Increase in mole-fraction beyond 0.5 results in the Silicon Germanium lying underneath silicon channel to get strained and therefore the strain in the channel get relaxed. Moreover, in order to maintain strain in the channel the thickness of the Strained Silicon layer should be less than the critical thickness as above this misfit dislocations get incurred at channel interface which traps the charges and therefore, the performance of the MOSFET gets saturated. The strain induced by this structure is along both x-y axis, therefore, the strain induced is biaxial in nature.

## 5. RESULTS AND DISCUSSION

The simulation of the device is carried out with sentaurus simulator and the results obtained are described as follows.

Figure 4. shows the plot between mobility and germanium mole-fraction. It is shown in the plot that both hole mobility and electron mobility increases with increase in germanium mole-fraction i.e. strain. Hole mobility range is much less than electron mobility range because holes have less effective mass than electrons. Electron mobility increases to a great extent at lower germanium content and the increase saturates at higher germanium content. This is because at higher germanium content vertical electric field increases and electrons being

majority carrier shows higher scattering coefficient and therefore, the factor of electron mobility increase gets lessen. Since holes occupy valence band and being minority carriers gets less affected by electric field and therefore, the increase factor remains same for higher germanium content as well. With the increase in strain the six energy valleys in the conduction band of silicon splits into two-fold degenerate and four-fold degenerate. These two split valleys have energy difference of 0.67x. This difference in the energy levels causes repopulation of the electrons at lower energy level, thereby reducing their net effective mass. This difference in energy level also results in increase in distance between these valleys thereby decreasing the intervalley scattering rate. The relation of mobility to these two factors is:

$$\mu = q\tau/m \tag{1}$$

Therefore, decrease in effective mass and scattering rate ($1/\tau$) results in increase in mobility of the charge carriers.

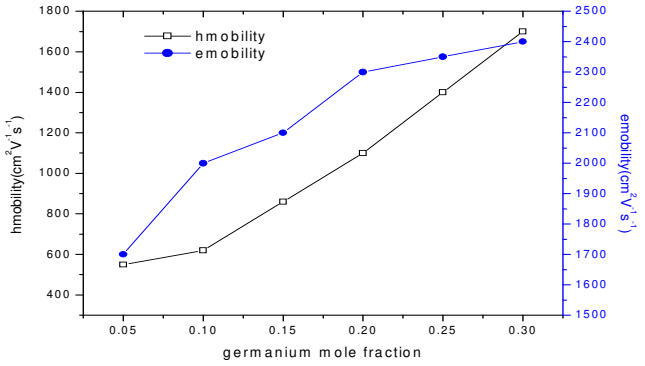


Figure 4. Mobility profile with variation of mole-fraction.

Figure 5. shows the plot between drain current and germanium mole fraction. It is clear from the plot that with increase in mole-fraction, the drain current also increases. This is due to the fact that drain current is directly proportional to the mobility of the carriers according to the drain current equation of MOSFET [8].

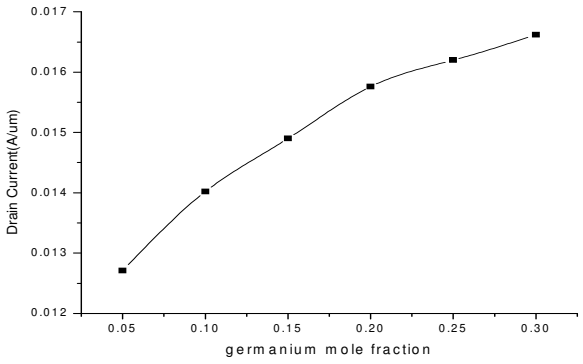


Figure 5. Drain Current variation with variation in mole-fraction

Figure 6. shows the graph between subthreshold swing and DIBL vs. germanium mole-fraction. It is observed from the graph that with increase in mole-fraction subthreshold swing and DIBL decreases. DIBL decreases because the lateral electric field induced in the channel due to strain prevents the drain barrier to gets lowered. Since, the carriers in the channel shows profound increase in mobility, the generation-recombination rate of the carriers also gets increased and therefore, there is no diffusion current which is the main source of subthreshold current. Therefore, increase in strain results in decrease of subthreshold current . Subthreshold swing parameter, which is defined as the inverse of the slope of the $\log_{10}(I_{DS})$ versus VGS characteristic and since with increase of strain drain current increases and therefore subthreshold swing decreases with increase of strain (increase of mole-fraction).

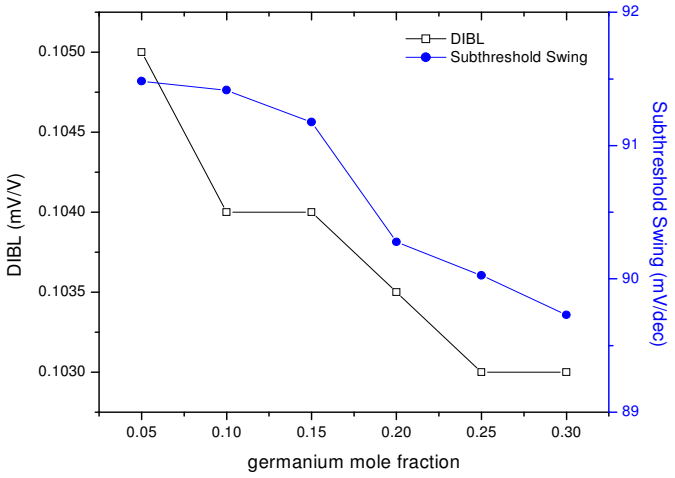


Figure 6. DIBL and Subthreshold Swing variation with variation in mole-fraction

Figure 7. shows the plot between electron velocity and transconductance vs. germanium mole-fraction. It is shown that with increase in mole-fraction both electron velocity and transconductance increases. With increase in mobility the electron velocity increases as depicted in following equation:

$$v = \mu E \tag{2}$$

Similarly, since drain current increases with strain the transconductance of the device also increases as it is directly proportional to drain current. Increase in transconductance depicts decrease in resistance of the device. With increase in electron velocity and transconductance, the switching factor of the device increases and therefore, the device operates faster.

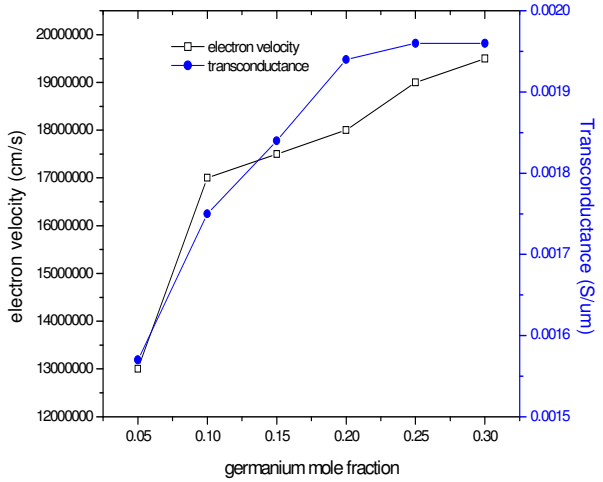


Figure 7. Electron velocity and transconductance variation with mole-fraction

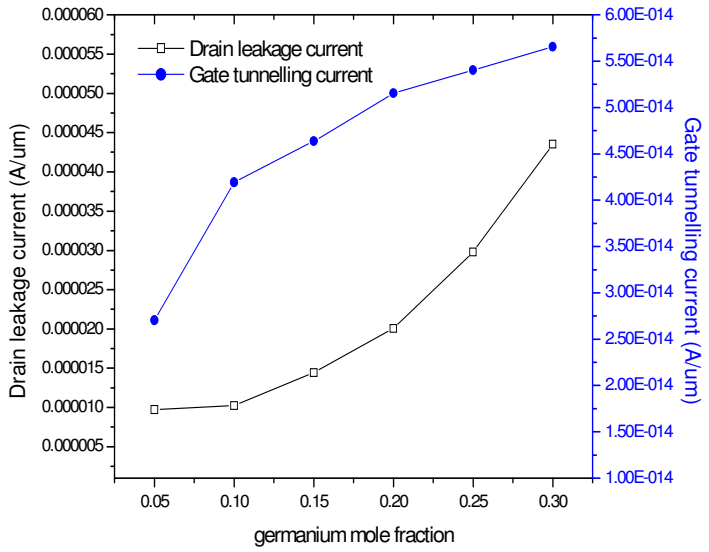


Figure 8. Leakage current with variation in mole fraction

Figure 8. shows the graph between static leakage current and germanium mole-fraction. It is observed that with increase in mole-fraction the leakage current also increases. This is due to the combined effect of lateral electric field, backscattering rate and increase in conduction band four-fold energy level, the leakage current at drain increases. Also the gate tunnelling current increases with increase in strain because the conduction band energy level increases and therefore the electrons can easily traverse from the gate to the strained silicon channel. Though

the magnitude of leakage current is very small but still due to the increase in leakage current with strain, the strain in the channel region cannot be increased to a great extent.

Figure 9. shows the graph between mobility and channel thickness. It is observed from the graph that with increase in channel thickness both the electron and hole mobility increases till 10 nm and beyond 10 nm the mobility gets saturate. As the channel thickness is increased the inversion region increases and the carriers get large space to move about thereby resulting in decrease in scattering of the carriers and thus mobility increases. But beyond a certain thickness the increase does not affects the mobility as misfit dislocations gets incurred in the channel region which acts as a trap for the carriers.

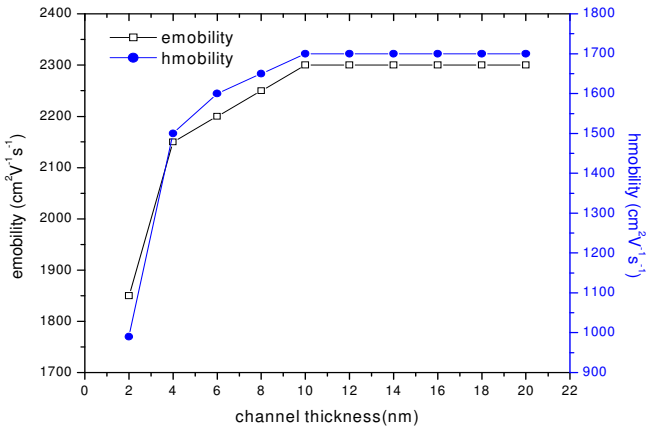


Figure 9. Mobility profile with channel thickness

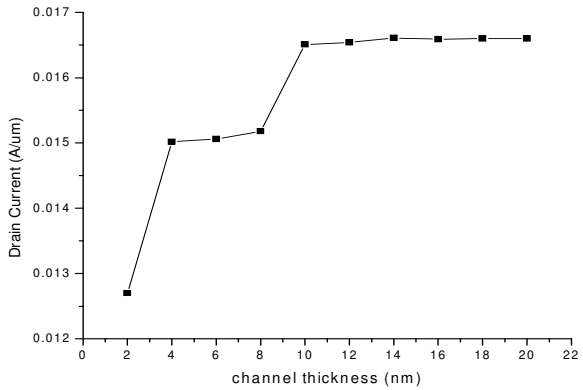


Figure 10. Drain Current variation with channel thickness

Figure 10. shows the plot between drain current and channel thickness. It is clear from the plot that the drain current increases till 10nm with increase in channel thickness. Increase in drain current is due to the increase in mobility of the carriers. As the mobility gets saturated after 10nm, likewise the current also gets saturated at 0.0166A/um beyond 10 nm.

Figure 11. shows the plot between leakage current and channel thickness. It is shown in the plot that drain leakage current increases with channel thickness in the initial stage and gets saturated later on because of the increase in lateral electric field and mobility in the channel at initial stage. The gate leakage current does not vary much with channel thickness because it depends on the applied potential and normal electric field which has no direct dependence on channel thickness.

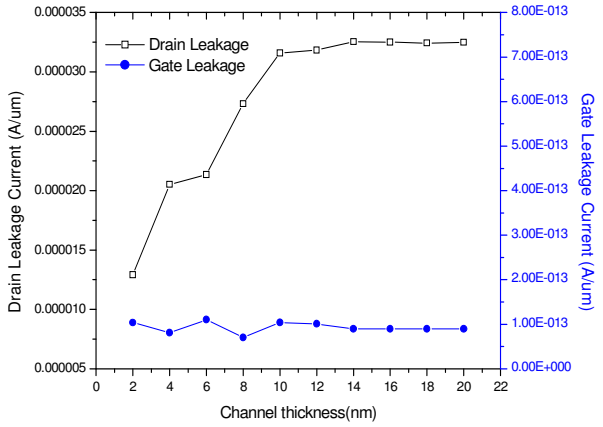


Figure 11. Leakage current variation with channel thickness

Other performance parameters like subthreshold Swing, transconductance, DIBL etc has no direct dependence on the channel thickness as they are dependent on many other factors which vary in random fashion with channel thickness. Therefore, these parameters variation cannot be categorised with variation in channel thickness.

# 5. CONCLUSION

In this work it is concluded that with increase in strain in the channel, the performance of the MOSFET is enhanced. Foremost, the mobility of the carrier increases with strain and thus, other performance parameters like drain current, DIBL, subthreshold swing, electron velocity, and transconductance also gets improved. Though the amount of leakage current in Strained Silicon MOSFET is very small but the leakage current also increases with strain and therefore the trade-off should be taken care of. With increase in channel thickness, the carrier mobility, drain current also increases initially and saturates later on due to introduction of misfit dislocations. Thus, MOSFET with strained channel provides much better performance than Bulk MOSFET with certain trade-off which can be taken care off. Therefore, due to improved functionality, Strained Silicon MOSFET should be incorporated in modern day VLSI applications.

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## REFERENCES


[1] Jakub Walczak and Bogdan Majkusiak, "Electron mobility and Drain Current in strained-Si MOSFET", *Journal of Telecommunications and information Technology*, pp. 84-87, 3/2007.

[2] Athanasios Dimoulas, Evgeni Gusev, Paul C.McIntyre and Marc Heyns, "Advanced Gate Stacks for High-Mobility Semiconductors" *Springer Series in Advanced Microelectronics*, 2007.

[3] Y. Lin, Report on "Advanced Gate Stacks for Strained Silicon Devices", 2005.

[4] ISE TCAD: Synopsys Santaurus Device simulator.

[5] S. I. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors", *Journal of Applied Physics*, vol. 80, pp. 1567-1577, 1996.

[6] Wong Yah Jin, Ismail Saad and Razali Ismail, "Characterization of strained silicon MOSFET using semiconductor TCAD Tools", *IEEE Trans, ICSE2006* Proc, pp. 924-928,2009.

[7] Weiying Gu, Renrong Liang, Mei Zhao, Jun Xu, "Strained Silicon Dynamic Threshold Voltage MOSFETs for low voltage and ultra high speed CMOS circuits, *IEEE Transactions*, 2008.

[8] S. Kang and Y.Leblebici, "CMOS Digital Integrated Circuits" Tata McGrawHill.

[9] P. vander Meer et al., "Ultra-low standby-currents for deep sub-micron VLSI CMOS circuits: smart series switch," *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 4, pp. 1-4, 2000.

[10] J. R. Hauser, "Extraction of experimental mobility data for MOS devices," *IEEE Transactions on Electron Devices*, vol. 43, pp. 1981-1988, 1996.

[11] James G. Fiorenza, Ji-Soo Park and Anthony Lochtefeld, "Detailed Simulation Study of a Reverse Embedded-SiGe Strained-Silicon MOSFET", *IEEE Transactions on Electron Devices*, Vol. 55 No. 2, February 2008.

[12] J.L.Hoyt, H.M.Nayfeh, S.Eguchi, L.Alberg, G.Xia, T.Drake, E.A.Fitzgerald and D.A.Antoniadis "Strained Silicon MOSFET Technology", *IEEE,* IEDM 2.1.1-2.1.4, 2002.

[13] Tejas Krishnamohan, Christoph Jungemann, Donghyun Kim, Enzo Ungersboeck and Siegfried Selberherr, " Theoretical Investigation of performance in Uniaxially and Biaxially-Strained Si, SiGe and Ge Double-Gate p-MOSFETs", *IEEE,* 2007.

[14] Kern (Ken) Rim, Judy L.Hoyt and James F.Gibbons, " Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's", *IEEE Transactions on Electron Devices,* vol. 47, No. 7, July 2000.

[15] Y. Taur and T. H. Ning, Fundamentals of modern VLSI devices, *NY: Cambridge University Press,* 1998.

[16] K. Rim, et al., "Strained Si NMOSFETs for high performance CMOS technology," *Symp. on VLSI Tech.*, , pp. 59-60, 2001.

[17] Muhammad Nawaz and Mikael Ostling, "A Design Evaluation of Strained Si-SiGe on Insulator (SSOI) Based Sub-50 nm nMOSFETs", *Journal of Semiconductor Technology and Science,* Vol. 5, No.2, June 2005.

[18] Stefan Flachowsky, Andy Wei, Ralf Illgen, Tom Herrmann, Jan hontschel, Manfred Horstmann, Wilfried Klix and Roland Stenzel, "Understanding Strain-Induced Drive Current Enhancement in Strained-Silicon n-MOSFET and p-MOSFET", *IEEE Transactions on Electron Devices,*vol. 57, No.6, June 2010.

## Authors

**Neha Sharan** received her B.Tech. Degree in Electronics & Communication Engineering in 2009from B.H.S.B.I.E.T, Lehragaga, Punjab, India.She is pursuing her M.Tech. Degree in VLSI Design Automation and Techniques from Department of E&CE, National Institute of Technology, Hamirpur HP India. Her area of interest is Semiconductor devices modelling and VLSI.

**Ashwani K. Rana** received his B.Tech degree in Electronics and Communication Engineering NIT Hamirpur, India in 1998 M.Tech degree in VLSI Technology from Indian Institute of Technology, Roorkee, India in 2006. He is currently pursuing the Ph.D degree in nano devices from National Institute of Technology, Hamirpur, India. Presently he is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India, as an Assistant Professor. His research interest include modelling of semiconductor devices, low power high performance VLSI circuit design and emerging integrated circuittechnologies. He has more than 10 publications in International/National Journal & conferences and guided more than 10 M.Tech students in these areas. He is member of ISTE.