# A NOVEL APPROACH FOR LOWER POWER DESIGN IN TURBO CODING SYSTEM

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***Abstract****: Low Power is an extremely important issue for future mobile communication systems; The focus of this paper is to implementat turbo codes for low power solutions. The effect on performance due to variation in parameters like frame length, number of iterations, type of encoding scheme and type of the interleave in the presence of additive white Gaussian noise is studied with the floating point model. In order to obtain the effect of quantization and word length variation, a fixed point model of the application is also developed.. The application performance measure, namely bit-error rate (BER) is used as a design constraint while optimizing for power and area coverage. Low power Optimization is Performed on Implementation levels by the use of Voltage scaling. With those Techniques we can reduced the power 98.5%and Area(LUT) is 57% and speed grade is Increased .This type of Power maneger is proposed and implemented based on the timing details of the turbo decoder in the VHDL model.*

***Keywords:*** *low power consumption, Turbo Encoder, Turbo Decoder, Power Ooptimization, AreaOptimization.*

## I INTRODUCTION

Application specific design is a process of alternative design evaluations and refined implementations at various abstraction levels to provide efficient and cost effective solutions. Turbo codes were presented in 1993, by Berrou et al. [20] and since then these codes have received a lot of interest from the research community as they offer better performance thanany of the other codes at very low signal to noise ratio. Turbo codes achieve near Shannonlimit error correction performance with relatively simple component codes.

Efficient methodology for the application specific design reduces the time and effort spentduring design space exploration. The turbo code application from the area of wirelesscommunications is chosen as the key application for which an application specific designmethodology is developed. The

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functionality and specific characteristics of the applicationare needed to carry out the design space exploration. The application characteristics studiedare, the impact on the performance of the turbo codes with variation in the size of the inputmessage (frame-length), type of the interleaver and the number of decoding iterations.Turbo coding is a forward error correction (FEC) scheme.

Iterative decoding is the key feature of turbo codes. [1-15] Turbo codes consist of concatenation of two convolution codes. Turbo codes give better performance at low SNRs (signal to noise ratio) .Interestingly, the name Turbo was given to this codes because of the cyclic feedback mechanism (as in Turbo machines) to the decoders in an iterative manner. The algorithmic specifications and the performance characterization of the turbo codes. Form a pre-requisite study to develop a low power solution. Functional analysis of turbo decoder with simplified computation metric to save on power as well as the architectural features like bit-width are closely related to the application parameter like bit-error rate (BER).

# II SYSTEM LEVEL MODELING

System level modeling is the phase of design aimed at architecture exploration before theactual HDL implementation. The availability of system level modeling and implementation techniques helps us to ensure functional correctness as well as explore the design space.The memory access patterns in the application are studied. The data flowanalysis as well as synchronization requirement between the different modules form the basis for identifying parallelism in the algorithm. This drives the hardware solution of the turbo encoder and decoder design at system level in the design methodology. Identifying the access pattern of the computationally intensive routines, it is proposed to use FIFO/LIFO buffers to store the intermediate results in the four state turbo decoder.To test the implementation correctness, the turbo encoder and one four state turbo decoder is synthesized onto Xilinx ISE simulators.

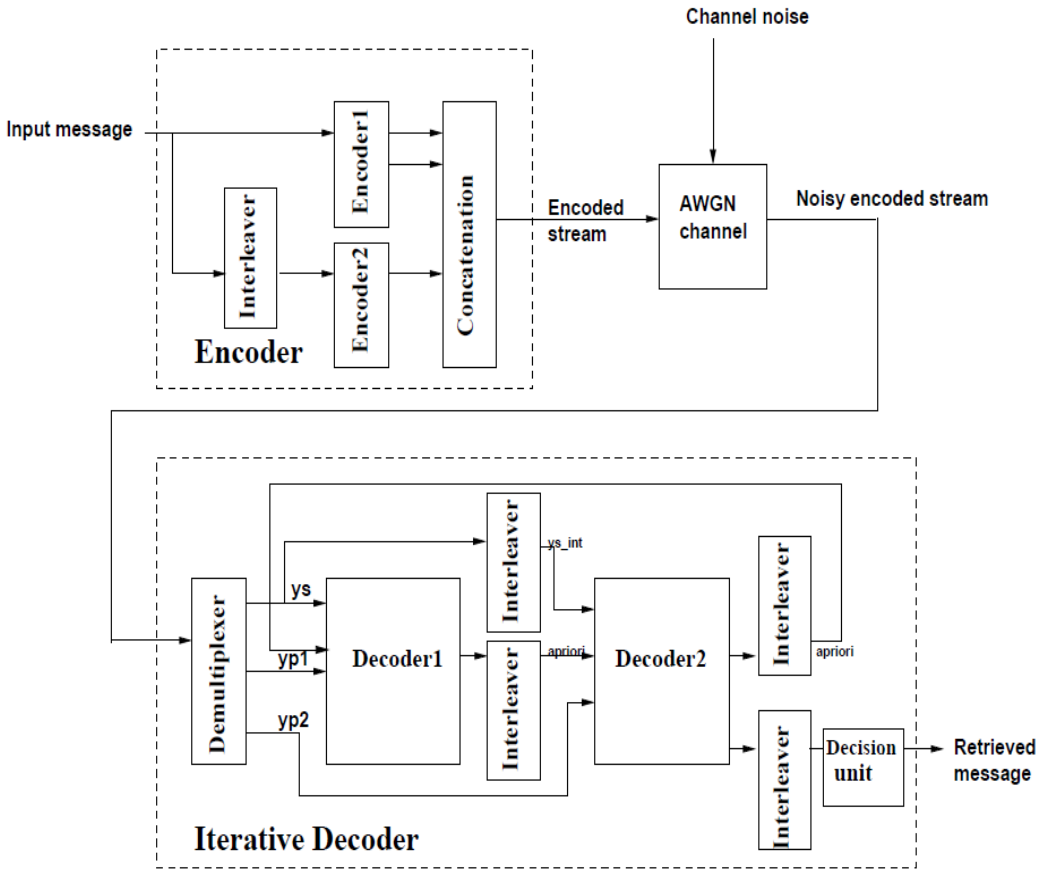



Figure 1: The turbo coding system

1.Generate the message to be transmitted through the channel, which is a binary data offrame size *N*. Generating this message to be transmitted through the AWGN channel is done using a random number generator.

2. The two encoders, depicted in figure 4.1 encode the message into a bit stream and transmit it through the channel. To the encoder1, the input is the message to be transmitted and to the second, it is the interleaved message using symmetric interleaver of size *N*. The encoded data is concatenated and mapped to the (1, 0) channel symbols onto an antipodal baseband signal (+1, -1), producing transmitted channel symbols.

3. Add AWGN noise to these transmitted channel symbols to obtain the noisy receiver input.

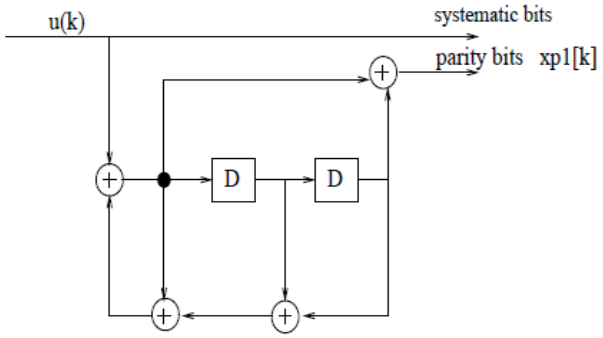
4. Perform MAP decoding for six iterations to retrieve the message that is transmitted. Bit error rate is computed to obtain the performance of the turbo decoder for varyingsignal-to-noise ratios.

## Turbo encoder

Turbo coding system consists of the turbo encoder and the turbo decoder. The description of the four state and eight state (3GPP).

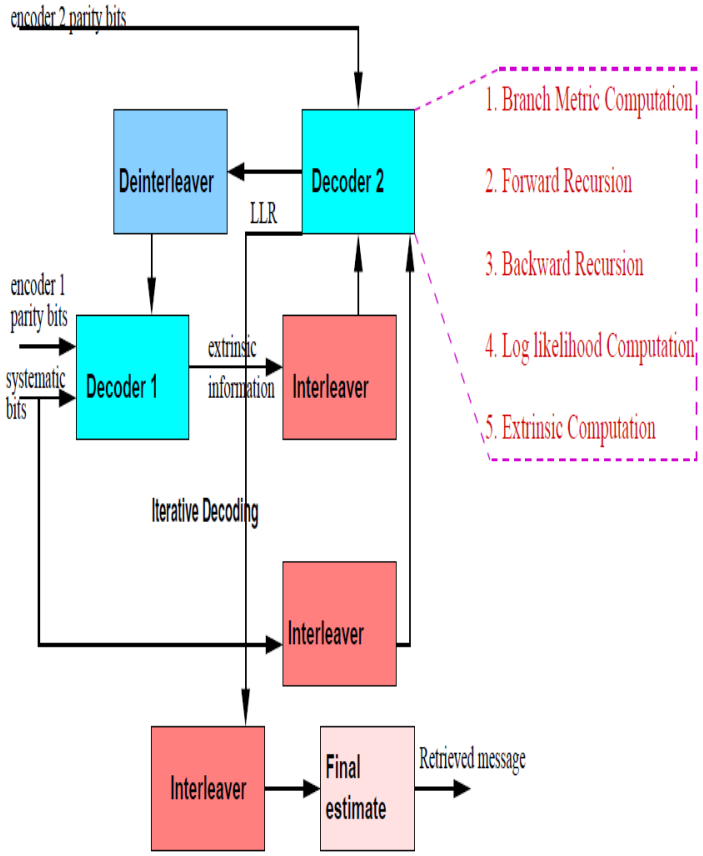
## Four state turbo encoder

The general structure of turbo encoder architecture consists of two Recursive SystematicConvolutional (RSC) encoders Encoder 1 and Encoder 2. The constituent codes are RSCsbecause they combine the properties of non-systematic codes and systematic codes.In the encoder architecture displayed in the two RSCs are identical. The *N* bitdata block is first encoded by Encoder 1. The same data block is also interleaved and encoded by Encoder 2. The main purpose of the interleaver is to randomize burst error patterns so that it can be correctly decoded. It also helps to increase the minimum distance of the turbo code . Input data blocks for a turbo encoder consist of the user data and possible extra data being appended to the user data before turbo encoding.The encoder consists of a shift register and adders . The structureof the RSC encoder is fixed for the design because enabling varying encoder structures would significantly increase the complexity of the decoder by requiring to adapt to the new trellis structure and computation of the different metrics in the individual decoders. The input bits are fed into the left end of the register and for each new input bit two output bits are transmitted over the channel. These bits depend not only on the present input bit, but also on the two previous input bits, stored in the shift register.




## Turbo Decoder

In turbo decoder the iterative decoding process of the turbo decoder is described. The maximum *a posteriori* algorithm (MAP) is used in the turbo decoder. There are three types of algorithms used in turbo decoder namely MAP, Max-Log-MAP and Log-MAP. The MAPalgorithm is a forward-backward recursion algorithm, which minimizes the probability of bit error, has a high computational complexity and numerical instability. The solution to these problems is to operate in the log-domain. One advantage of operating in log-domain is that multiplication becomes addition. Addition however is not straight forward. Addition is a maximization function plus a correction term in the log domain. The Max-Log- MAP algorithm approximates addition solely as maximization. Max-Log-MAP algorithm in turbo decoder is used in our work.




The block diagram of the turbo decoder is shown inabove Figure. There are two decoders corresponding to the two encoders. The inputs to the first decoder are the observed systematicbits, the parity bit stream from the first encoder and the de interleaved extrinsic information from the second decoder. The inputs to the second decoder are the interleaved systematic bit stream, the observed parity bit stream from the second RSC and the interleaved extrinsic information from the first decoder. The main task of the iterative decoding procedure, in each component decoder is an algorithm that computes the *a posteriori* probability (APP) of the information symbols which is the reliability value for each information symbol.

### 1) Branch metric computation

Turbo decoding the first computational block is the branch metriccomputation. The branch metrics is computed based on the knowledge of input and output associated with the branch during the transition from one state to another

$$\gamma[k] = x_s[k] \cdot z[k] + x_s[k] \cdot L_c \cdot y_s[k] + L_c \cdot x_p[k] \cdot y_p[k] \qquad \text{Eq. 1}$$

### 2) Forward metric computation

The forward metric is the next computation in the algorithm, which represents the probability of a state at time k, given the probabilities of states at previous time instance.

$$\alpha_s[k] = \sum_{s' \epsilon S} \alpha_{s'}[k-1]\gamma_{s',s}[k] \qquad \text{Eq. 2}$$

Where the summation is over all the state transitions, which is to be computed at each node at a time instance k in the forward direction traversing through the trellis and is computed for states 00, 01, 10 and 11.

### 3) Backward metric unit

The backward state probability being in each state of the trellis at each time k, given the knowledge of all the future received symbols, is recursively calculated and stored The backward metric is computed using equation 3 in the backward direction,

$$\beta_{s'}[k-1] = \sum_{s} \beta_s[k] \cdot \gamma_{s',s}[k] \qquad \text{Eq. 3}$$

Where the state transition is from s', β. is computed for states 00, 01, 10 and 11 in a 4 state decoder. In an 8 state decoder - 3GPP version is computed for states 000, 001,010, 011, 100, 101, 110 and 111.

### 4) Log likelihood ratio (lr)

Log likelihood ratio llr is the output of the turbo decoder. This output llr for each symbol at time k is calculated as

$$llr[k\text{-}1] = ln\frac{\sum_{u_k=1} \alpha_{s'}[k-1]\beta_{s'}[k]\gamma_{s',s}[k]}{\sum_{u_k=0} \alpha_{s'}[k-1]\beta_{s'}[k]\gamma_{s',s}[k]} \qquad \text{Eq. 4}$$

The sign of the number corresponds to the hard decision while the magnitude gives a reliability estimate

.

### 5) Extrinsic unit

Compute the extrinsic information that is to be fed to the next decoder in the iteration sequence. This is the llr minus the input probability estimate. Extrinsic information ext [k-1] is obtained from the log likelihood ratio llr [k-1] by subtracting the weighted channel systematic bits and the information fed from the other decoder.

# III. DESIGN MODULES

In application specific designs, impact of architectural parameters on the power consumption and area is significant. With increasing demand for low power battery driven electronic systems, power efficient design is presently an active research area. Batteries contribute a significant fraction of the total volume and weight of the portable system. Ap plications like digital cellular phones, modems and video compression are compute and memory intensive. The basic components in these are the input-output units, on-chip mem ory, off chip memory and the central processing unit.

Power dissipation is highly dependent on the switching activity, load capacitance, frequency of operation and supply voltage. Further design parameters like memory size and bit width influence the power consumption significantly.

The power dissipation of the application design needs to be lowered using suitable architectural optimizations. In this project work a digital design for log MAP coding for turbo encoding/decoding is developed for such portable devices.

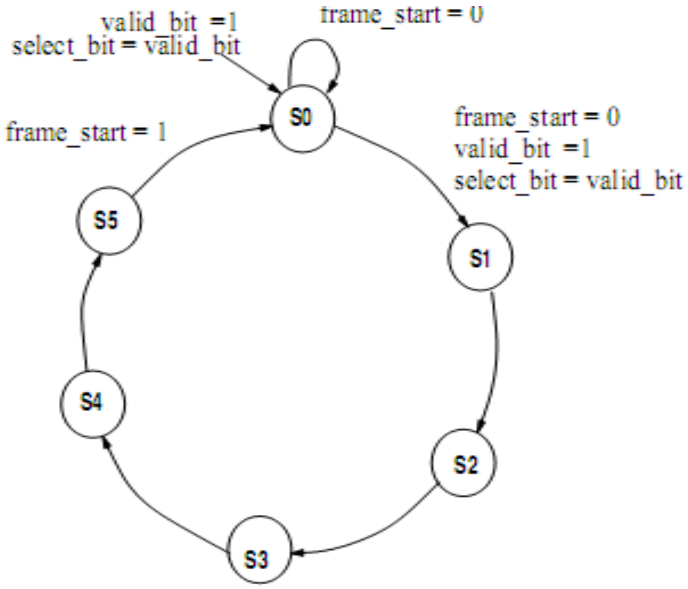
## C) FSM Controller Unit

The top-level controller, whose purpose is to activate the modules in proper order, manages the turbo decoding process. The turbo decoder which constitutes of the two decoders is iterative in nature. The simulations have to be performed for six iterations. Hence a top-level finite state machine (FSM) controller unit is essential. A FSM consists of a set of states, a start state and a transition signal to move from the current state to the next state (in turbo decoder from one iteration to the next iteration). The FSM design appears explicitly in the turbo decoder design system for the control and the sequencing of the iterations. At the data flow level, iteration control and the data computation of the decoder system are separated then the description of the FSM has a close correspondence to the typical behavior of the algorithm.

Frame start is the input bit from the FSM controller unit to the computation unit.

Valid bit is the input bit signal from the last module of the decoder2 to the controller unit

Select bit is the output bit signal from the FSM controller unit to the first module of the decoder1




## IV.SIMULATION RESULTS

The design is first modeled in VHDL and then synthesized using Leonardo tools. XPower brings an extra-level of design assurance to the low-power device analysis. Accurate power estimation during programmable design is done with XPower. XPower reads in either pre-routed or post-routed design data and provides accurate device power estimation either by net, or for the overall device. Results are provided either in report or graphic format. The VHDL designs were simulated and only synthesized. The estimates are for 0.18 m technology. The voltage that is used in our estimation is 2.5V. There is a facility to set the input capacitance and frequency of operation for whichthe design power estimation is to be done. There is a provision to give a specific switching activity for the design power estimation. The estimate for 20 and 50 activity factor is found.

XPower calculates the power as a summation of the power consumed by each component in the design. The power consumed is the product of capacitance, square of the voltage, activity factor and frequency of operation and is reported in mW.

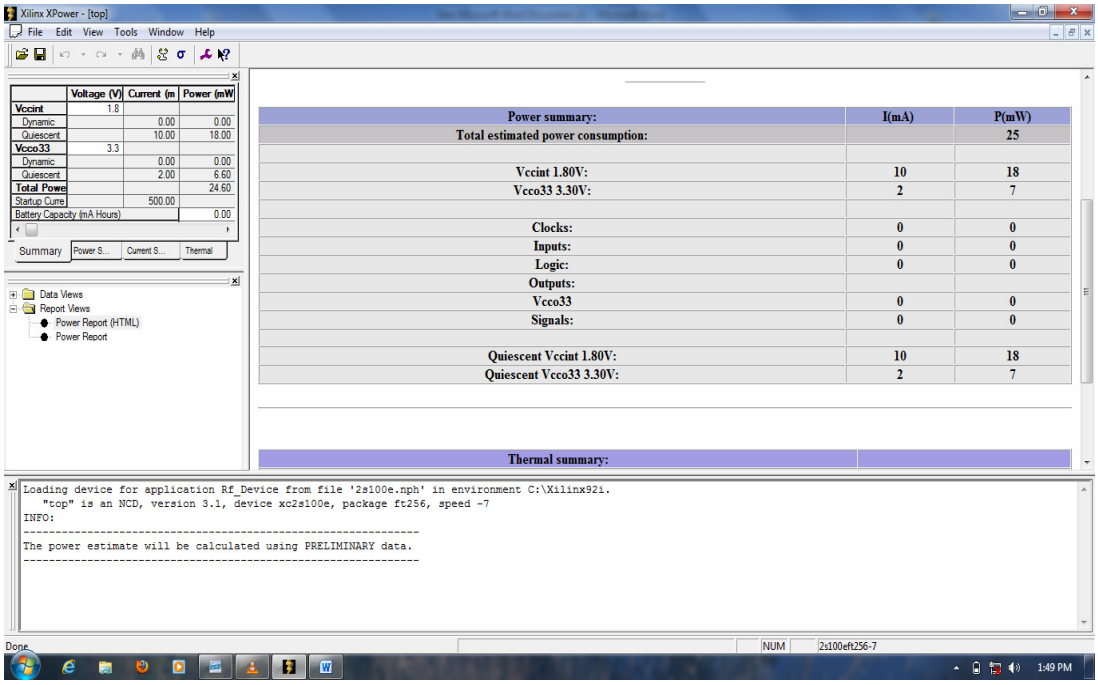



Figure:2 (A)Turbo encoder and Decoder Top module Power report

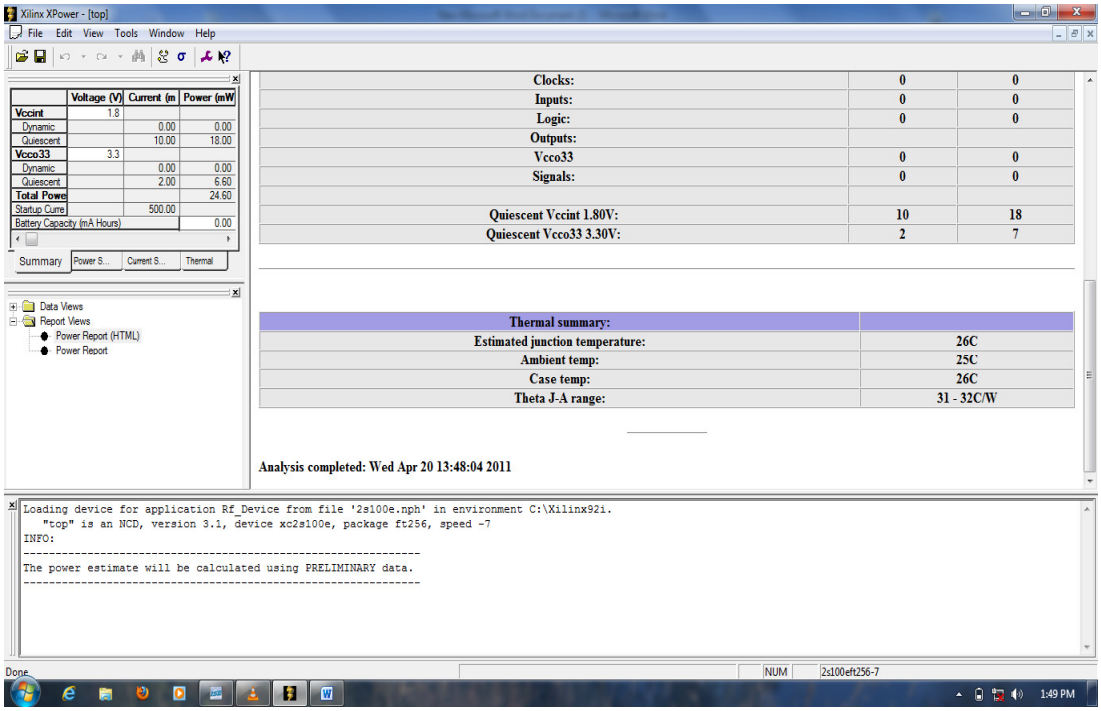



Figure:2 (B)Turbo encoder and Decoder Top module Power report with date

Figure:-2(A) and (B) Represented that the Turbo encoder and Decoder Top Module power report, Which is implemented by using XPower Tool this is repeat a gives the varies Parameter such as voltage output from the it observed that this approach achieve a power Consumption of 98.5% this is 25mV.there is > improvement is power consumption When it compared with a real Existing work made by references(1605mV),(1069mV).

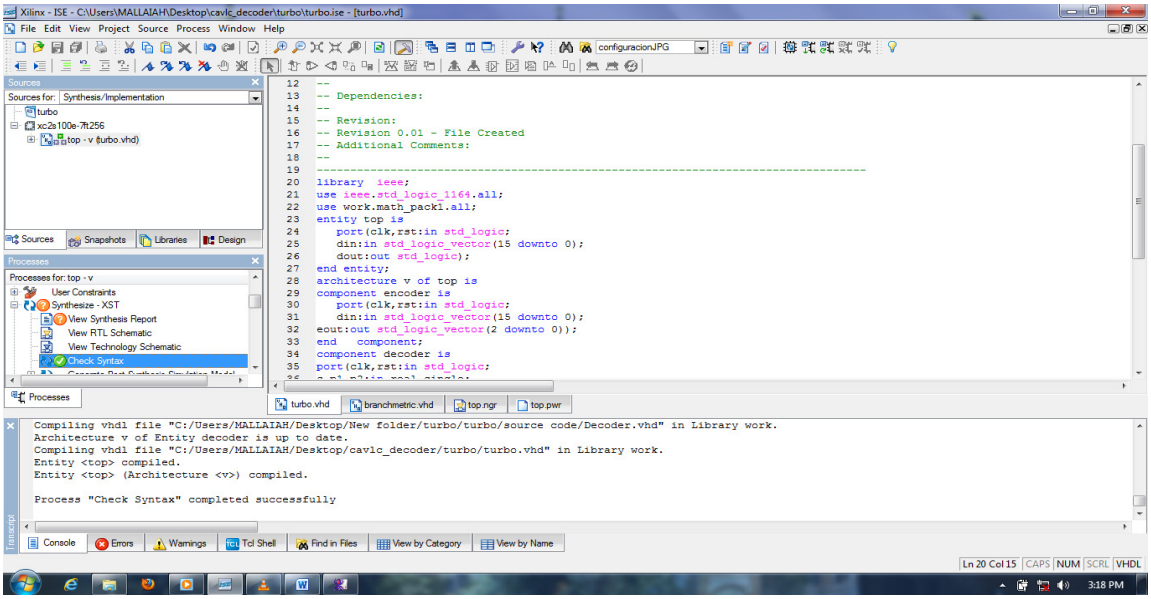



Figure:3 Turbo encoder and Decoder Top module check syntax report

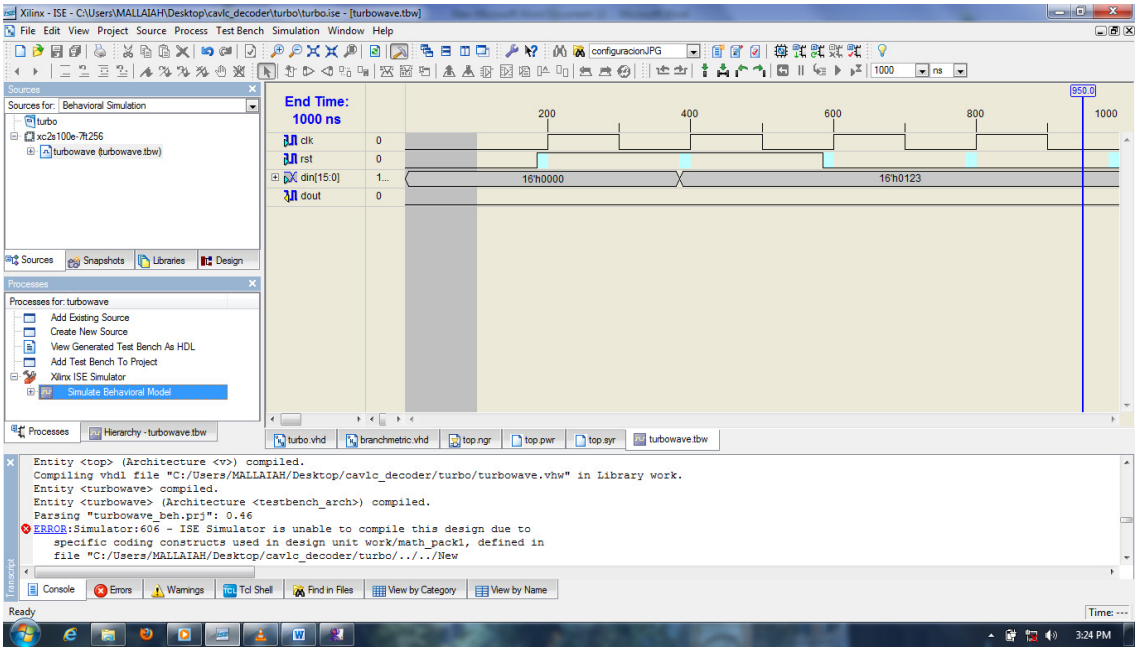



Figure 4: simulation observation illustrating timing result for the Turbo encoder and decoder

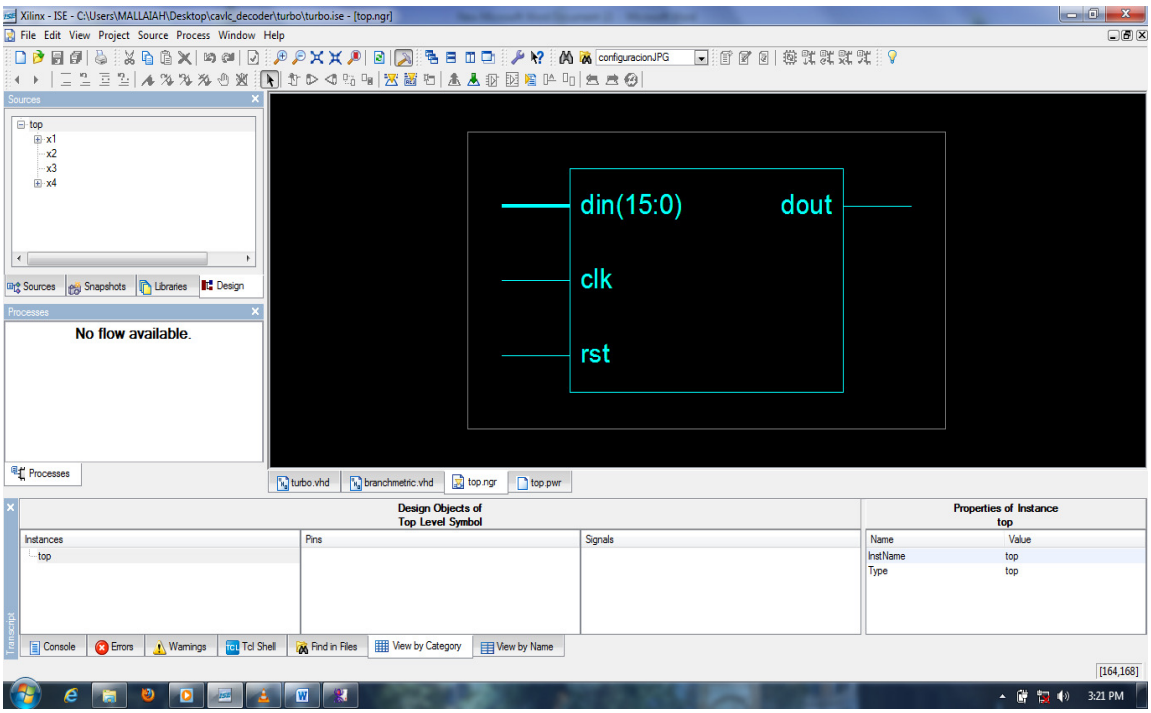



Figure: 5(A) RTL view of turbo Encoder and Decoder Top module

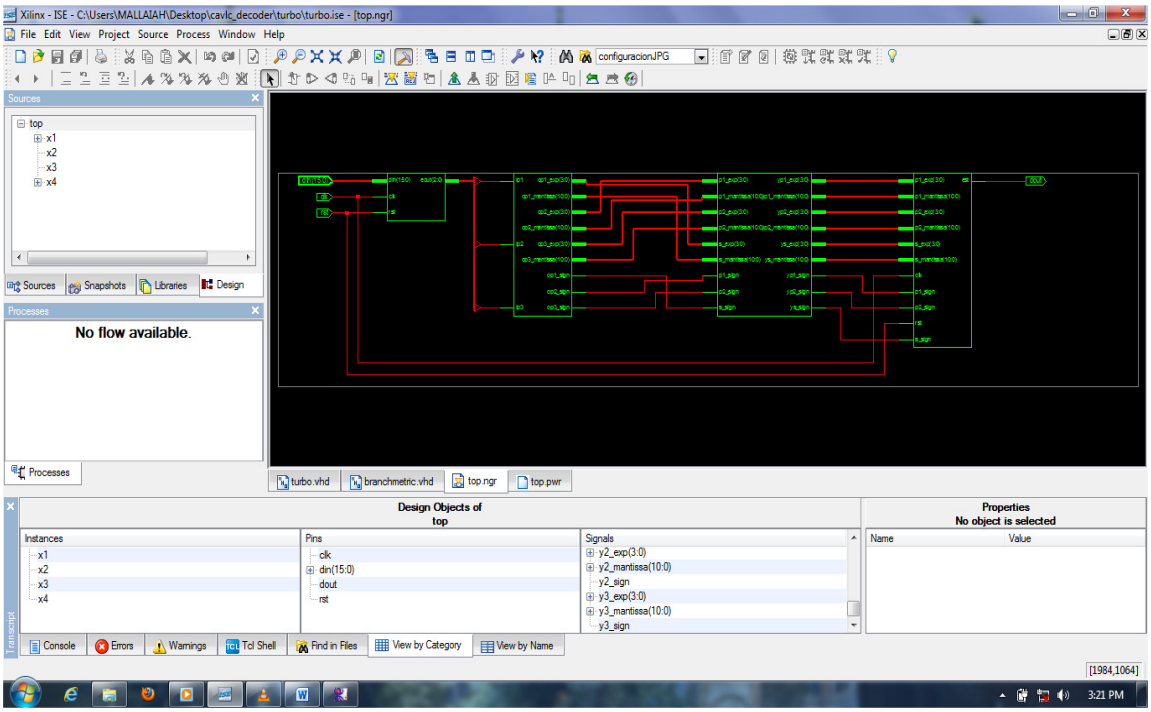



Figure: 5(B) RTL view of Internal Turbo Encoder and Decoder Top Module

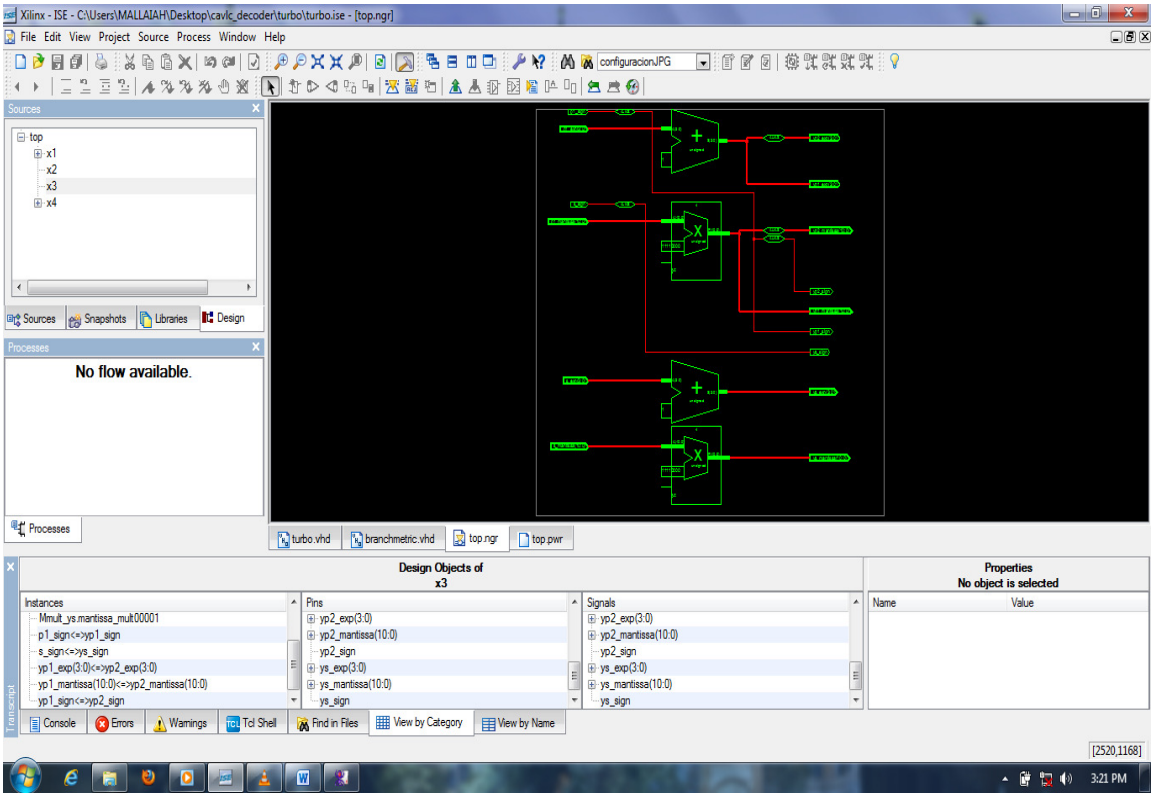



Figure: 5(C) RTL view of Internal turbo Encoder and Decoder Top Module

## PERFORMANCE EVALUATION CONSUMPTION OF EXISTING AND PROPOSED APPROACH

Table:1

| publication | 32 Bit design Previous work | Reference paper [21] Existing work | Present optimal design this paper work |
|---|---|---|---|
| Power(mv) | 1695mv | 1069mv | 25mv |
| Power consumed % | -------- | 63% | 1.5% |
| Power saved % | -------- | 36.92 % | 98.5% |
| Area 4 bit LUT | 5216 | 2816 | 2267 |
| Area(LUT) is accupied % | -------- | 53 % | 43% |

| | | | |
|---|---|---|---|
| Area(LUT) is saved % | --------- | 46% | 57% |
| Speed grade | ---------- | 5 | 7 |
| IOB | 19 | 19 | 19 |
| VCC | 1.8v | 1.8v | 1.8v |
| #BELS | ------- | 6549 | 3142 |
| No of Slices | ------- | 2701 | 1206 |
| No of slices FF | -------- | 119 | 71 |

# V. CONCLUSION

From this paper here the author proposed a novel approach for power consumption which is based on turbo coding details and it is implemented in vhdl based on Xilinx platform . From the results it is observed that a major improvement of power consumption that is 25mv has been achieved when it compare with other previous approaches a significant power saving that is 98.5%. and utilization of the power is 2.5%only

Not only this with respect area only 43% is occupied by the LUTS which gives an improvement of reduces sing area from 53% (previous) to 43% . Further in this work speed grade is increased and{ #BELS are reduced to 48% and No of Slices are reduced to 44.65% and No of slices FF are reduced to59.66%, compare to previous work (Reference paper:21)}

# VI. FUTURESCOPE:

The following are the some of the interesting extensions of the present work:

1.An interesting topic for future research is to perform more extensive performance comparisons between FFT based BTC – OFDM and DCT based BTC – OFDM systems under additional real-world channel impairments, such as multipath fading, time dispersion which leads to inter symbol interference (ISI).

2. The main problems with OFDM signal is very sensitive to carrier frequency offset, and its high Peak to Average Power Ratio (PAPR). So, BTC – OFDM systems can be tested for these problems.

3. The turbo code system which is going to be the *defecto*standard in 3G communication systems has been selected as the specific application.

4. Turbo Code Applications provides a vast coverage of those applications starting from data storage systems through wire-line and wireless communications. That includes the utilization in satellite communications, digital video broadcasting, space exploring systems, and the implementation technologies.

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