Design and test challenges in Nano-scale analog and mixed CMOS technology

Mouna Karmani, Chiraz Khedhiri and Belgacem Hamdi

Electronics & Microelectronics Laboratory, Monastir, Tunisia
mouna.karmani@yahoo.fr
chirazkhedhiri@yahoo.fr
belgacem.hamdi@gmail.com

Abstract

The continuous increase of integration densities in Complementary Metal–Oxide–Semiconductor (CMOS) technology has driven the rapid growth of very large scale integrated (VLSI) circuit for today's high-tech electronics industries from consumer products to telecommunications and computers. As CMOS technologies are scaled down into the nanometer range, analog and mixed integrated circuit (IC) design and testing have become a real challenge to ensure the functionality and quality of the product. The first part of the paper presents the CMOS technology scaling impact on design and reliability for consumer and critical applications. We then propose a discussion on the role and challenges of testing analog and mixed devices in the nano-scale era. Finally we present the I_{DDQ} testing technique used to detect the most likely defects of bridging type occurring in analog CMOS circuits during the manufacturing process and creating a resistive path between V_{DD} supply and the ground.
To prove the efficiency of the proposed technique we design a CMOS 90nm operational amplifier (Op amp) and a Built in Current Sensor (BICS) to validate the technique and correlate it with post layout simulation results.

Keywords

Nano-CMOS technology, Analog testing, operational amplifier (Op amp), short (bridging) defect, resistive path, I_{DDQ} Testing, BICS, 90nm technology

1. Introduction

During the early 1970s, both Mead [1] and Dennard [2] noted that the basic MOS transistor structure could be scaled to smaller physical dimensions [3]. Also Moore's Law stated that the number of transistors on integrated circuits doubles every two years [4]. Thereby, the constant advances in VLSI technology have led to design and manufacture very complex integrated circuit including digital, analog and mixed circuits in the same chip, this approach is known as system-on-a chip (SOC) which is the future of the IC technology [3,5].

So, with the rapid increase of chip complexity, testing of electronic components is a real challenge and an important part of the business to ensure the functionality and quality of a reliable product at a reasonable cost [3]. The traditional tests are the most expensive in terms of both test development costs and test implementation for analog and mixed signal circuits. In a SOC, up to 80% of the test costs are due to the analog and mixed signal functions that typically occupy only around 10% of the chip area [6].

The high analog test cost is due to many factors, such as expensive test equipment, long test development time, and long test production time. Test challenges for analog circuits are caused by accessibility problems and by lack of common test strategies and standards. Therefore, with the steady downscaling of CMOS technologies, developing a test methodology that reduces test cost

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and accelerates time-to-market without sacrificing IC quality is critical and very challenging [7]. For analog CMOS circuits, the continuous variations of parameters prevent the use of the fault concept as it is used in the digital domain. In fact, we are talking about catastrophic faults, which are directly responsible for a failure of the circuit (such as short circuits and open circuits) and parametric faults, which will cause degradation in performance of the circuit.

In this paper, we propose an I_{DDQ} current test methodology based on the use of a built in current sensor (BICS) that allows the detection of multiple bridging faults which create a resistive path between V_{DD} and the ground supply in analog and mixed circuits. To prove the efficiency of the proposed technique, a full custom CMOS operational amplifier is implemented in 90 nm technology and the most likely faults of bridging circuit type creating a resistive path between the V_{DD} and the GND supply are deliberately injected in the layout. Also, a CMOS BICS is designed and implemented in the same 90nm technology.

The paper is organised as follows. Section 2 presents the CMOS technology scaling: the design and testing challenges. The proposed test approach is presented in section 3. A case is studied in section 4. Finally, we conclude in section 5.

2. Complementary Metal-Oxide Semiconductors (CMOS) technology scaling

CMOS technology refers to the device technology for designing and fabricating integrated circuits that employ logic using both n- and p-channel MOSFET transistors. The complementary p-channel and n-channel transistor networks are used to connect the output of the device to either the VDD or VSS power supply rails. CMOS is currently the dominant fabrication technology due to its many advantages including low power requirements, high operating clock speed, density, cost, performance, and manufacturing designer experience [8].

A typical schematic structure of CMOS transistor is given in fig. 1. In conventional NMOS circuit, Figure 1 (a), the substrate is normally connected to ground or lowest potential in the circuit and in PMOS circuits, the substrate is connected to supply voltage or the highest potential in the circuit [9].

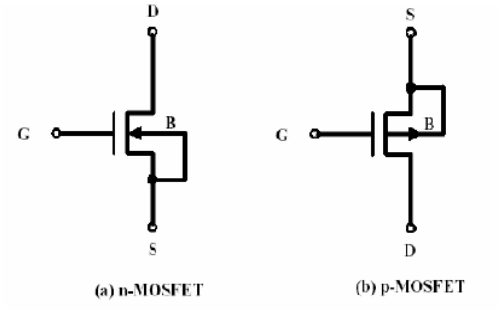

Figure 1: NMOS and PMOS transistors structure

Over the past decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a denser and faster integration [1-3-10]. The need for more performance and integration has accelerated the scaling trends in almost every device. The transistors manufactured today are twenty times faster and occupy less than 1% of the area of those built twenty 20 years ago [3].

2.1.NANO-SCALE CMOS Technology

The evolutionary trend in nano-scale CMOS technologies predicted by Moore's law has been fuelled by a huge demand for ever better performance and by fierce global competition over the past three decades [3]. Nano-scale CMOS technology is desirable for several reasons: firstly Smaller MOSFETs may allow more current to pass, due to their shorter length dimension. Also MOSFETs are like resistors in the on-state, and shorter resistors have less resistance. Secondly smaller MOSFETs have smaller gate areas, and thus lower gate capacitance. Finally the most important reason for MOSFET scaling is reduced area, leading to reduced cost because the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer which reduce the price per chip [11-12].

"Scaling MOS devices down below 100 nm has produced little improvement in device transconductance, has increased the dominance of wiring parasitics in predicting circuit gain bandwidth, and has brought into play a plethora of lithographic, stress, quantum, and process variability effects that make the problem of good analog device matching more difficult". Supply voltage scaling, power dissipation and variability are fast becoming major bottlenecks limiting the performance of nano-scale CMOS technologies [13].

2.2.The design challenge

With the introduction of nano-scale CMOS technologies, analog and mixed designers are faced with many new challenges at different phases of design. These challenges include severe degradation in device matching characteristics as a result of device and lithographic quantum limits [13]. "Unfortunately, in the nano-scale era analog CMOS design becomes more complex which causes nonidealities include hot carrier injection and time-dependent dielectric breakdown effects limiting supply voltage, stress and lithographic effects limiting matching accuracy, electromigration effects limiting conductor lifetime, leakage and mobility effects limiting device performance, and chip power dissipation limits driving individual circuits to be more energy-efficient" [13].

The lack of analog and mixed design and simulation tools available to address these problems has become the focus of a significant effort with the electronic design automation industry [13]. Consequently, semiconductor designers have begun to move design methodologies to higher levels of abstraction, in part to speed integration but also to ensure their designs are adaptable to changes in specifications or system design [14]. Also, adaptive solutions that can analyze and correct design specific yield issues are needed. Since yield levels are becoming design dependent, it is now becoming important to not only improve the yield level for each new design but to do so in an acceptable amount of time [15].

2.3.Most commonly observed physical defects in analog CMOS technology

In CMOS technology, the most commonly observed physical defects are permanent and parametric faults. Permanent faults are further classified into catastrophic faults (open and short (bridging)) and parametric faults (due to disturbance in the process parameters). When a catastrophic fault occurs, the topology of the circuit is changed. Due to parametric faults, the performance parameter of manufactured circuit deviates from the nominal one and therefore corresponds to a different point in each parameter space [7].

2.4. The testing challenge

If you design a product, fabricate and test it, and it fails the test, then there must be a cause for the failure. Either the test was wrong or the fabrication process was faulty, or the design was incorrect, or the specification had a problem [5]. The testing phase is one of the most important tasks in design and manufacturing of integrated circuits. The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong, and where the process needs to be altered. Therefore, correctness and effectiveness of testing is most important for quality products. If the test procedure is good and the product fails, then we suspect the fabrication process, the design, or the specification [5].

In many cases the failure analysis of a faulty circuit in the manufacturing test returns negative results, the primary cause for this result is that the test is incomplete because the defect coverage is too low, thus manufacturing test cannot identify the faulty parts. The adoption of Design for Test (DFT) methods such as scan test and Automatic Test Pattern Generators (ATPG) targeted at the stuck-at fault model was the solution to improve the defect coverage [16].
Another popular technique for detection of defects in CMOS VLSI circuits is the I_{DDQ} testing. This technique involves online monitoring of the power supply current. Usually Bridging faults induce an elevated I_{DDQ} current. Therefore these faults can be easily detected using a Built In Current sensor (BICS) [17-18].

3. The proposed test procedure

In this section, we present the I_{DDQ} test technique that serves to diagnose analog ICs, and distinguish a fault-free from a faulty circuit with respect to short defects. This technique is based on analysing the leakage current (I_{DDQ}) of the circuit under test using a Built In Current Sensor. In our investigation, we prove that at the nanometer range I_{DDQ} testing is still be used to detect multiple bridging defects which create a resistive path between V_{DD} supply and the ground.

I_{DDQ} test is based on measuring the current on supply lines (V_{DD}, GND) of the circuit under test (CUT). The defects which increase the I_{DDQ} current will be detected using a built in current sensor inserted between the circuit under test and the ground [16, 19, 18].

A short between two or more nodes in the circuit can induce an undetermined level creating a resistive path between V_{DD} and ground. The current created is higher than the quiescent current and can be easily detected using a BICS. Fig. 2 shows the Built In current Sensor inserted between the cmos circuit under test and the ground.

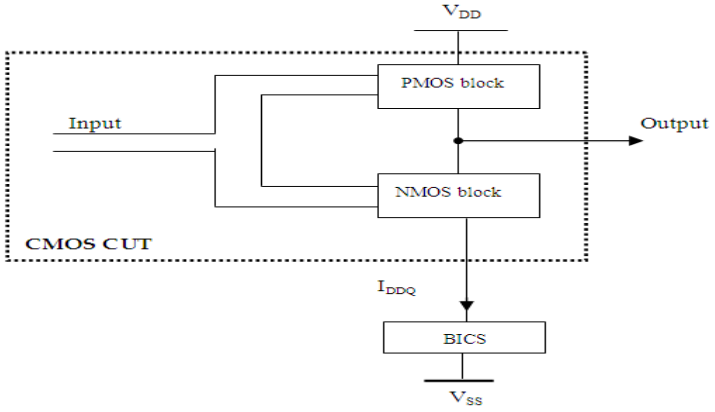

Figure 2: A built in current sensor measuring the I_{DDQ} current of the CMOS circuit under test

The detailed sensor design is shown in fig. 3 [21]. Using the BICS requires the estimation of the reference current I_{REF} which is the I_{DDQ} current value of the faulty free integrated circuit under test. Then, when testing the circuit if the I_{DDQ} current of the circuit under test is less than I_{REF} we suppose that the circuit is fault-free, otherwise, the increase in current beyond this value means that there is a failure in the circuit [20].

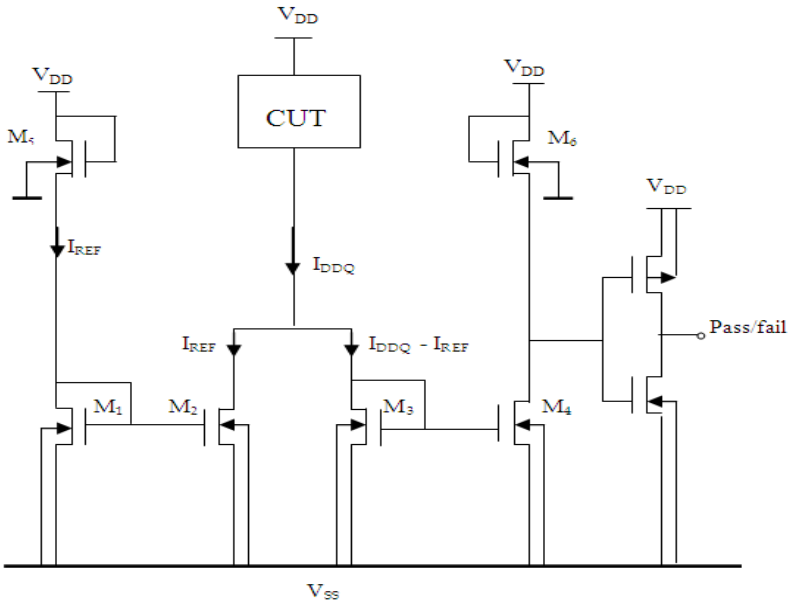

Figure 3: The detailed Built In Current Sensor CMOS design

4. Case Study

In order to evaluate the merit of the proposed test technique, we apply the above mentioned test procedure on a CMOS operational amplifier circuit (Op amp). The Op amp under test is a two stage amplifier, having a differential input amplifier and single-ended output stage. Fig. 4 shows the circuit typology of the CMOS Op amp.

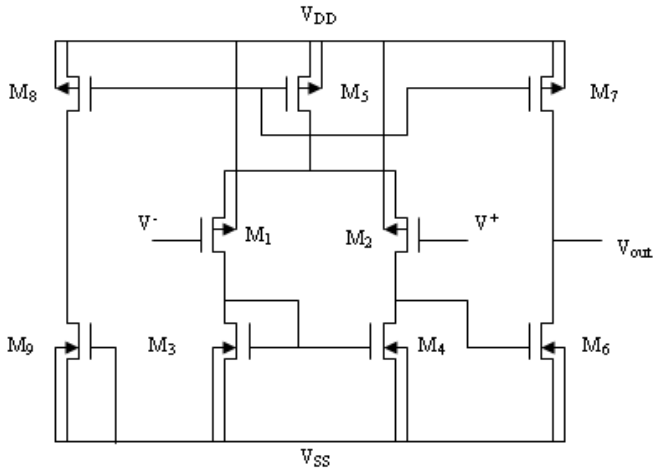

Figure 4: CMOS operational amplifier

The first floor of this CMOS amplifier includes a PMOS source coupled differential pair transistors M_1 and M_2, a current mirror with N-channel formed by the two transistors M_3 and M_4, a current mirror p-channel formed by two transistors M_8 and M_5 and active resistance composed by the N-channel transistor M_9. The second stage amplifier contains a common source N-channel formed by the transistor M_6 loaded by the current source formed by P-channel transistor M_7 [21]. The transistors are sized to have a bias current of 45µA intensity and an amplifier's quiescent current I_{DDQ} equal to 225µA. The operational amplifier is implemented in full-custom 90nm CMOS technology [22]. For this technology, the appropriate supply voltage V_{DD} is equal to 1.2V while V_{SS} is the ground (GND). SPICE simulations of the post-layout extracted operational amplifier are used to demonstrate that this amplifier has an acceptable electrical behaviour.

4.1. Simulation Results

The Spice simulation results of the CMOS operational amplifier are shown in next figures.

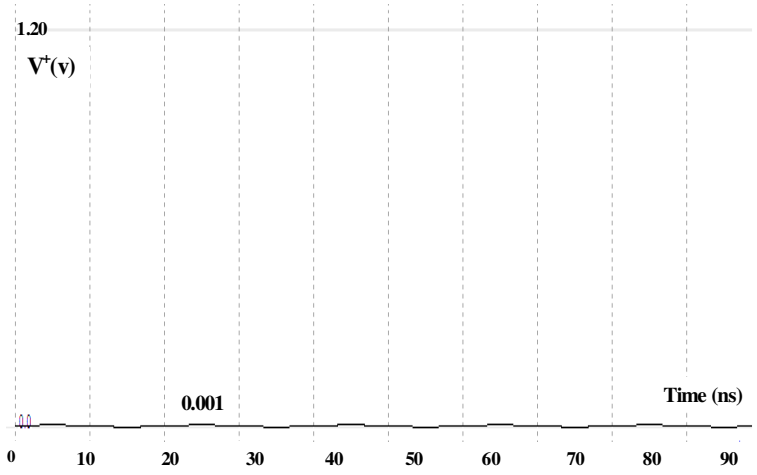

Figure 5: Input of the CMOS Operational Amplifier

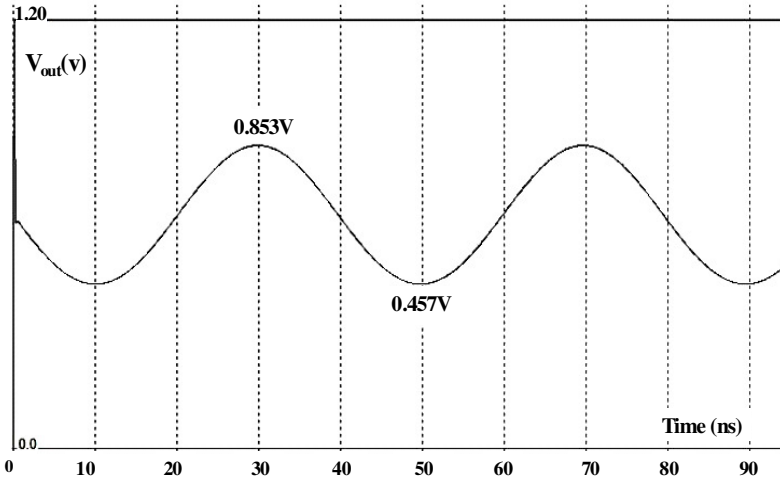

Figure 6: Output of the CMOS Operational Amplifier

Fig. 5 and fig.6 show respectively the input and the output waveforms of the Op amp. The operational amplifier input and the output are sinusoidal waveforms and its open loop gain is equal to 46 dB. The bias current waveform of the Op amp is given by fig. 7.

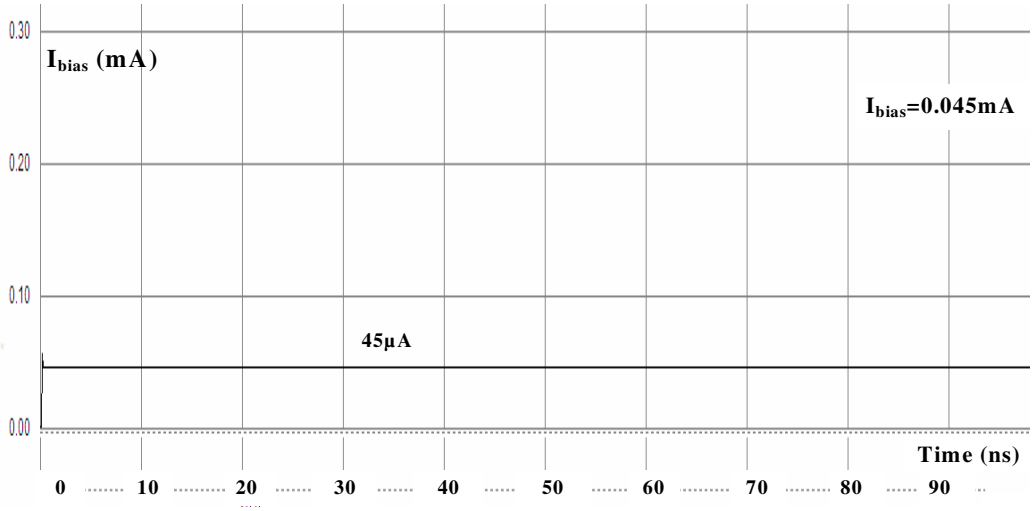

Figure 1: Bias current of the fault-free Operational Amplifier

Fig. 8 shows the I_{DDQ} current waveform of the Op amp.

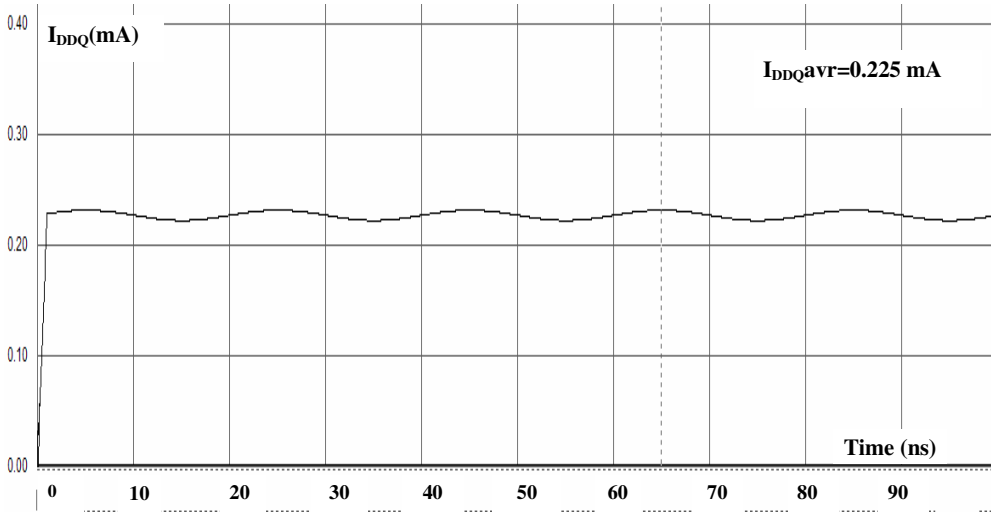

Figure 8: I_{DDQ} current of the fault free Op amp

Fig. 7 gives the I_{DDQ} current of the fault-free operational amplifier circuit. The average value of this current is equal to 0.225 mA as expected. Thus, when the value of the I_{DDQ} current is 0.225 mA we assume that there are no short-circuit defects.

Hence, we should note that the I_{DDO} value of the fault-free operational amplifier is the I_{REF} value of the built in current sensor (the BICS resolution). So, I_{REF}=0.225 mA. The layout of the CMOS

operational amplifier and the built in current sensor is given by fig. 9.

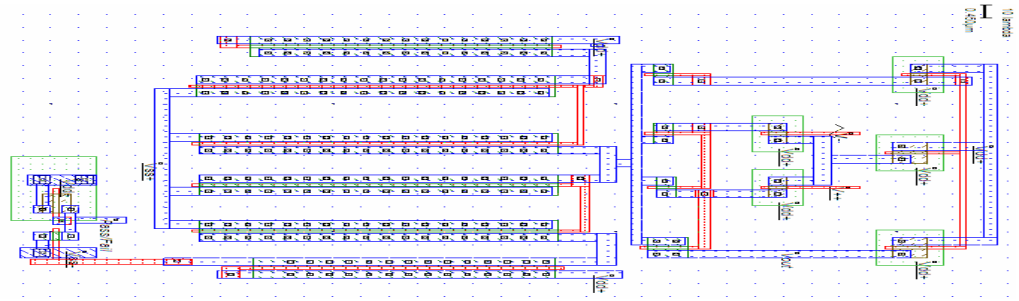

Figure 9: layout of the Built In Current Sensor inserted between the CMOS Op amp and the ground in the full-custom 90nm CMOS technology

The most likely resistive paths which can occur in the CMOS Op amp circuits during the manufacturing process are given by the next figure.

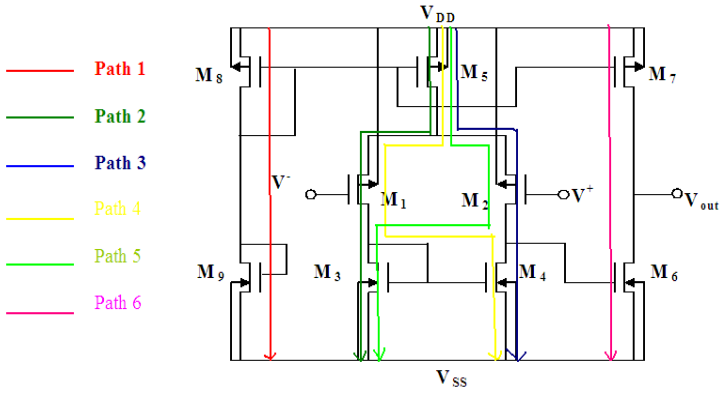

Figure 10: *Resistive paths which can occur in the CMOS Op amp circuits*

Each resistive path is injected at the layout level of the circuit under test using a Fault Injection NMOS Transistors (FIT). The FIT transistor is shown by fig. 11.

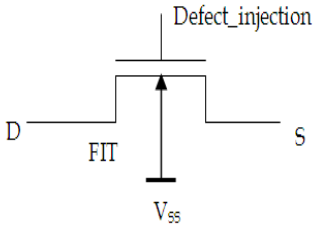

Figure 11: The NMOS Fault Injection Transistor

When the gate of the fault injection transistor is connected to V_{DD}, the FIT is activated and consequently the defect is injected. To prove the efficiency of the proposed testing approach some likelihood faults type multiple short defects which create a resistive path between V_{DD} and the ground are intentionally injected in the layout of the Op amp.

The first fault simulated is the resistive path (path1) created between V_{DD} and Vss supply. This fault consists of injecting two short defects at same time in the circuit under test to have the first resistive path. The first short defect is injected between the source and the gate of the PMOS M_8 transistor and the second is injected between the source and the gate of the NMOS M_9 transistor.

So to inject the resistive path 1 we must use two fault injection transistors (FIT_1 and FIT_2) as shown in fig. 12. V is the defect injection signal. When the gate of the fault injection transistor is connected to V_{DD} FIT_1 and FIT_1 are activated and consequently the resistive path (path1) is injected.

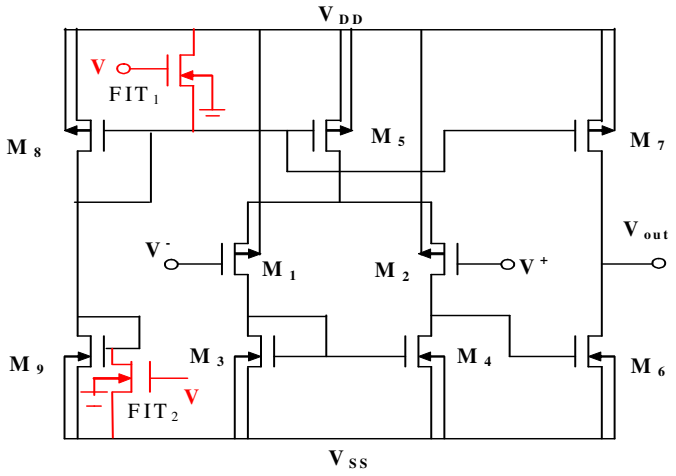

Figure 12: The resistive path 1 created using two fault injection transistors

Fig. 13 shows the simulation results obtained by injecting the resistive path1 at the layout level.

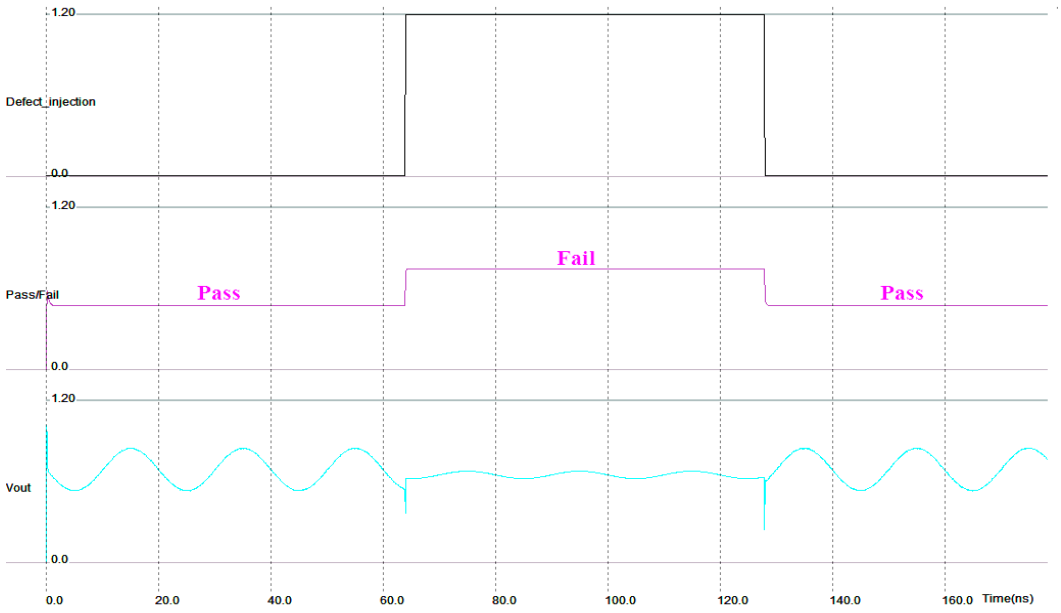

Figure 13: Simulation results obtained when the resistive path1 is injected at the layout level

From fig .13, we can notice that when the Op amp is fault free (Defect-injection=0) the output of the BICS is Pass, thus we are sure that the circuit under test does not contains a resistive path between V_{DD} and the ground. On the other side, the injection of the resistive path (Defect-injection=1) change the circuit under test output form that still sinusoidal but distorted. Also, the output of the BICS is Fail. So, surely the circuit under test contains a resistive path which increases the I_{DDQ} current beyond the resolution of the BICS (0.225 mA). In the same way, we can simulate all likelihood resistive paths that can occur in the operational amplifier under test.

5. CONCLUSIONS

As CMOS technologies are scaled down into the nanometer range, it is become very difficult to achieve a successful analog and mixed circuit design. Also, due to the dramatic increase in design complexity and the miniaturisation of transistors, test efficiency is the most important challenge facing the semiconductor industry.

In this paper we presented an I_{DDQ} testing methodology using a Built In Current Sensor to assure the detection of multiple bridging (short) circuit defects occurring in CMOS analog circuits which create a resistive path between the V_{DD} and GND supply. Finally we demonstrated that the I_{DDQ} testing technique can still be used in the nano-cmos scaled technology. This approach is able to distinguish a fault-free circuit from a faulty one with respect to multiple bridging fault model. Simulation results show that the technique is effective and can be easily implemented in the SOC environment.

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