Performance Comparison of RF CMOS Low Noise Amplifiers in 0.18-µm technology scale

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Abstract

This paper presents the design theory of conventional single-ended LNA and differential LNA based on CMOS technology. The design concepts give an useful indication to the design trade-offs associated with NF, gain and impedance matching. Four LNA's have been designed using technological design rules of TSMC 0.18-µm CMOS technology and this work mainly proposed for IEEE 802.11a applications. With 1.8V supply voltage, the proposed LNA's achieve a gain higher than 19dB, a noise figure less than 4dB and impedance matching less than -10dB at 5GHz frequency. The goal of this paper is to highlight the efficient LNA architecture for achieving simultaneous gain, noise and input matching at low supply voltage. The performance of all LNA's are analysed and compared using Agilent's Advanced Design System Electronic Design Automation tools.

Keywords: *CMOS, Low Noise Amplifier (LNA), RF design, Wireless application.*

1. Introduction

RF integrated circuits (RFIC's) are the basic building blocks of portable wireless communication devices. CMOS technology is one of the best technologies for realization of RF front-ends. This is possible because of the following features such as low cost, continuous device scaling and high integration. Due to an increasing demand on the consumer electronic services, the operating frequency is moving towards the 5GHz band. According to this, it is desirable to introduce innovative RF front-end designs. The simplified block diagram of RF front-end is shown in fig.1. Low Noise Amplifiers, Mixers and Oscillators are the basic building blocks of RF front-end.

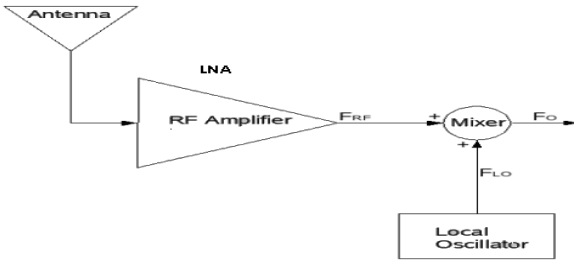

Figure.1. RF front-end

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In a typical design, LNA plays an important role because it is responsible for entire system sensitivity. Therefore, it should fulfill several requirements on the performance .These include providing a stable 50 ohms input impedance, minimizing the noise figure and supplying high gain to suppress the noise of other stages[1]. Several low-power, low-voltage single-ended and differential LNA designs have been reported [2-5]. All used simple cascode structure only in LNA schematic and also performance analysis done only at 2.4GHz. In [7], [8] & [10] , the following LNA objectives such as optimum gain, lowest noise figure and better impedance matching are not satisfied simultaneously in performance analysis. The aim of this work is to introduce an innovative LNA design structures for satisfying all design constraints and comparing their performances. The paper is organized as follows. The design theory of conventional single-ended and differential LNA discussed in Section 2.The proposed design structures and its importance presented in Section 3.Section 4 presents the simulation results of the LNA's ,which is followed by the conclusion.

2. Conventional LNA design

Fig.2. shows the block diagram of LNA. The topology may be single-ended or differential. It is composed of input matching, amplification and output matching blocks. The passive elements used for matching which plays an important role in the overall performance of the circuit in terms of gain and noise figure.

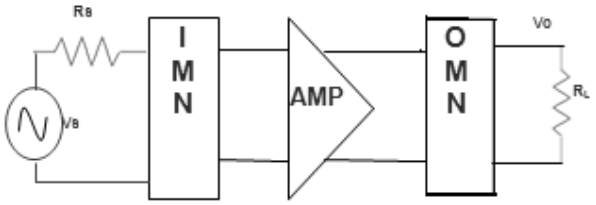

Figure2. Block diagram of LNA

2.1 Single-ended LNA

The conventional Single-ended LNA structure is shown in fig.3. It uses common source(CS) transistor M1 and common gate (CG) transistor M2. Lg and Ls are used for input matching. The small signal equivalent circuit is shiown in fig.4. used to evaluate the theoretical expression of input impedance.

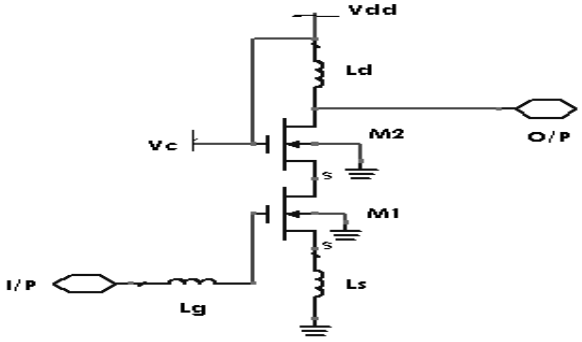

Figure3. Conventional Single-ended LNA topology

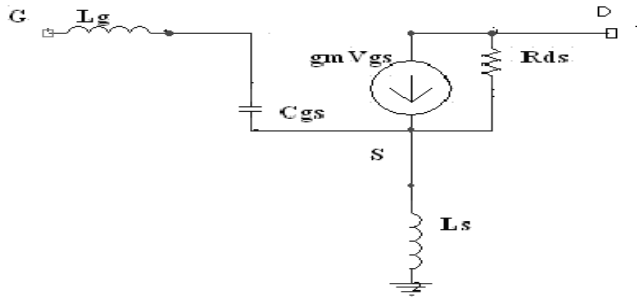

Figure4. Small Signal model at input stage LNA for impedance

The combination of the gate and source equivalent inductance cancels the reactance of the parasitic capacitance at the gate at resonance frequency ω_o. The expression for input impedance while looking at the gate of M1 is given in eqn.1

$$Z_{in} \cong j\omega_o L_s + \frac{1}{j\omega_o C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{1}$$

At resonance frequency, ω_o is evaluated as, $\omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}}$ (2)

The simplified expression of input impedance is given in eqn.3.

$$Z_{in} = \frac{g_m}{C_{gs}} L_s = 50\Omega \tag{3}$$

where g_m and C_{gs} represent the transconductance and gate-to-source capacitance of the M1 respectively. Rds is the drain-source impedance of MOSFET. To realize a gain of 20dB at 5GHz, L_S should be the source inductor in the order of 1 to 2nH. Fig.4. shows the small signal equivalent circuit for the noise analysis of the LNA.

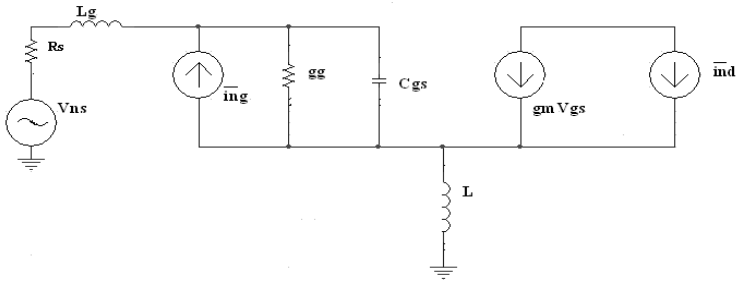

Figure5. Small Signal model at input stage LNA for noise

where g_g is the input admittance, mean-squared channel thermal noise current and gate induced noise current $i^2_{n_d}$ $i^2_{n_g}$ are shown in fig.5. The output noise power density due to the gate noise current (Sg) and drain noise current (Sd) derived first. Then the noise factor F is derived as the ratio between the sum (Sg +Sd) and output noise power density due to the source impedance(S_{Rs}).The simplified theoretical expression for achieving minimum noise figure (NF) is derived from equivalent circuit and shown below.

$$F_{\min} \cong 1 + \frac{2.4\gamma}{\alpha}[\frac{\omega_o}{\omega_T}] \quad (4)$$

where ω_o , ω_T are the resonance frequency and cut-off frequency and α ,γ are process dependent constants.

2.2 Differential LNA

Single-ended LNA design needs additional balun circuitry to convert single-ended output into differential output. Also, the second stage of receiver's are the mixers which require signal to be fed from a differential source. These are the limitations of single-ended LNA. In differential LNA, input/output signals can be realized in differential form. Fig.6. shows a schematic of conventional CMOS Differential LNA . It is constructed by using two single-stage cascode (CS-CG structure) LNA's. A cascade output buffer is also added with LNA for betterment of gain, noise figure and reverse isolation. In the first stage, input impedance required is confirmed by inductances L_g , L_s and gain is confirmed by transistor M1. The output block comprises the transistor M3 and the drain inductance $L_{d,}$ which are part of the output impedance network. The second stage comprises an input stage formed by another set of inductors L_g, Ls, and transistor M2.The equivalent circuit of conventional CMOS differential LNA is same as that of single-ended LNA. The LNA topology component values such as Q of an inductor, Gate inductance, Drain inductance and width of the transistors are evaluated using suitable design formulas given below. The Quality factor (Q) of an inductor lies between 6 and 10 for 0.18-µm technology scale. The value of L_g and L_d determined by using Eqn.(5) and Eqn.(6) and lies between 10 and 12 nH.

$$L_g = \frac{QR_s}{\omega_o} \quad (5)$$

$$L_d = \frac{1}{\omega_o \sqrt{C_{out}}} \quad (6)$$

where $\omega o = 2\pi f_o$ and f_o is the RF frequency and equal to 5GHz. The optimized width of the transistors evaluated by using these two factors C_{gs} and C_{ox} , and it is shown in simplified eqn.(7). The transistors width used for all the designs lies between 50 and 100-µm.

$$W = \frac{4LC_{gs}}{3C_{ox}} \quad (7)$$

where C_{ox} is the oxide specific capacitance, L is the channel length ,equal to 0.18-µm.

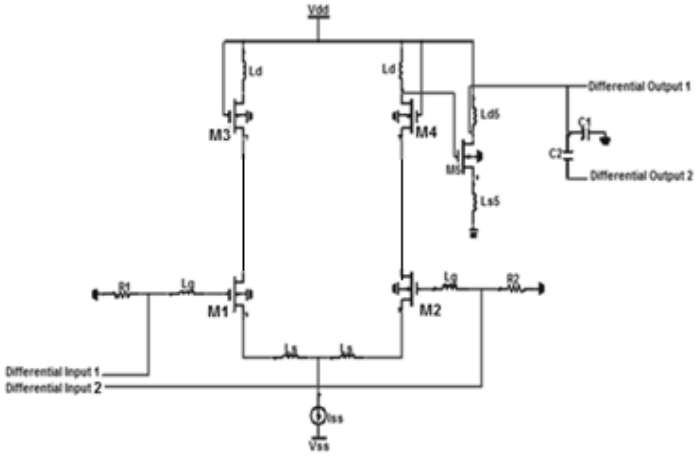

Figure6. Conventional Differential LNA topology

3. Proposed LNA's design

There are four design structures proposed for 5GHz LNA. The component values are calculated as per design theoretical expressions. The performance factors such as gain, noise figure and impedance matching design calculations are analysed by perspective understanding of CMOS based LNA designs. The simplified schematics of all structures shown in figs.7, 8,9,10. The following are the circuits, named as,

(i) Single-ended, inter-stage matched, inductively degenerated LNA
(ii) Single-ended, dual-CS cascode LNA
(iii) Inter-stage matched Differential LNA
(iv) Dual-CS Differential LNA

Inductor L is used as inter-stage matching inductor and represented in Fig.7 and Fig.9.The value lies between 2 to 3nH. It is introduced here in all designs, for improving the impedance matching and gain. Each common source (CS) stage of cascode structure is revised by using two parallel transistors instead of one , and renamed as dual CS stage. This change applied in Fig.8 &Fig.10 designs. Fig.10. shows a two-stage fully differential CMOS LNA.

It comprises an input stage formed by inductors L_g and L_s , two inter-stage inductors (L_{is}), four common source transistors(M1-M4), two common gate transistors(M5-M6), two drain inductors L_D and cascaded output stage transistor M7. The theoretical component calculations done with the help of revised equivalent circuits, shown in Fig.11& Fig.12.

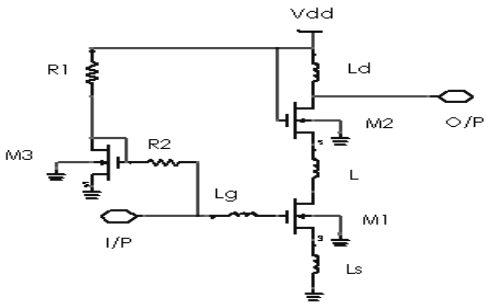

Figure7. Single-ended, inter-stage matched, inductively degenerated LNA

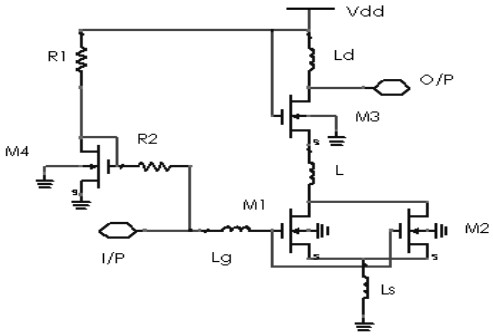

Figure8. Single-ended, dual-CS Cascode LNA

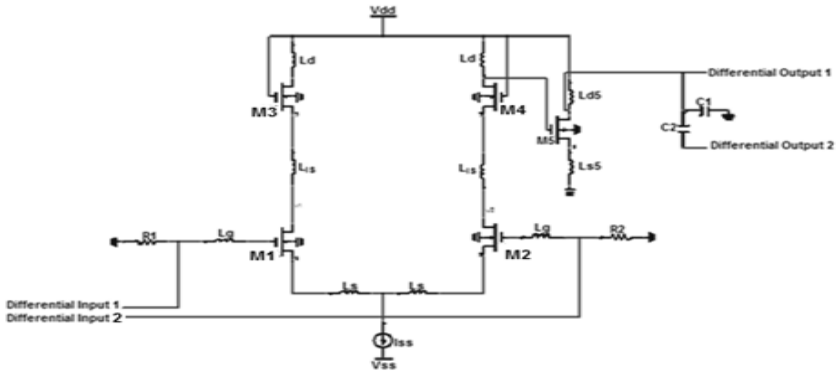

Figure9. Inter-stage Matched Differential LNA

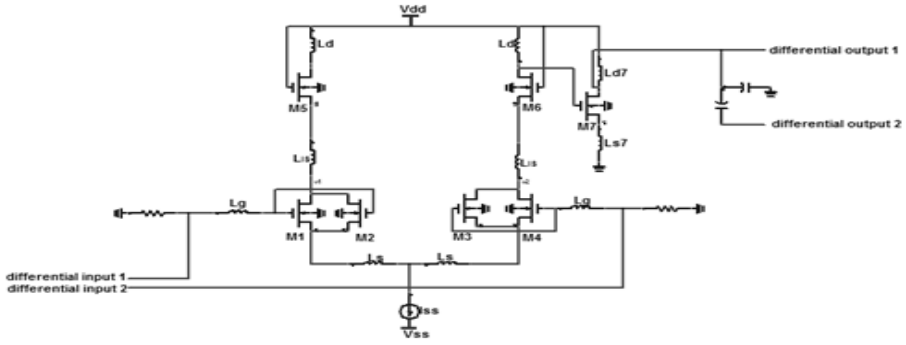

Figure10. Dual - CS Differential LNA

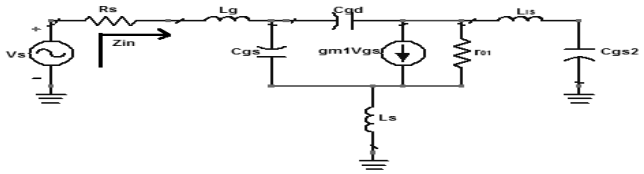

Figure11. Equivalent circuit with Matching Inductor L_{is}

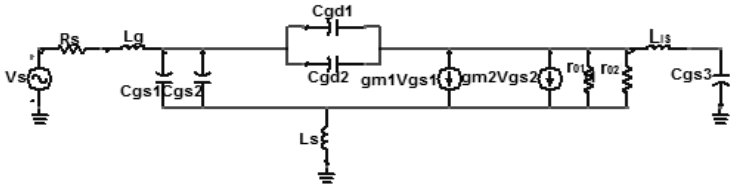

Figure12. Equivalent circuit for Dual CS stage with Matching Inductor L_{is}

4. Simulation Results

The proposed designs are simulated in a TSMC 0.18-µm CMOS process by Agilent's Advanced Design System EDA tools. The results are shown below. Fig. 13(a,b,c,d,e,f,g,h) shows simulated power gain S21, input matching S11 measured with respect to RF frequency in GHz. The noise figure is quite close to the theoretical value and demonstrates the noise performance of proposed design methodology. The simulated noise figure values are shown in Fig.14 (a, b, c, d) and markers are used to indicate the corresponding values. The performance comparison done between the four designs by bar graph and highlighted the efficiency of best LNA design. Fig.15, 16, 17 represents the bar graphs of gain, noise figure and input impedance matching.

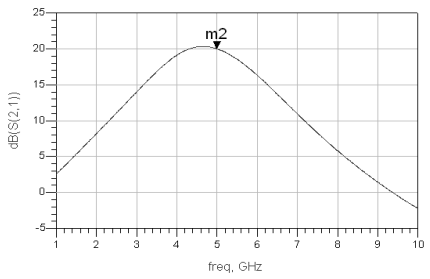

Figure13.(a)

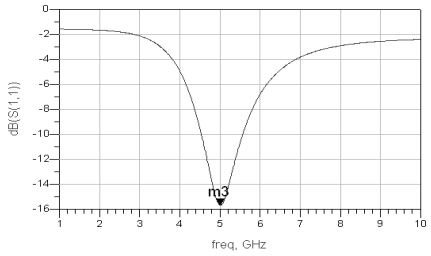

Figure13.(b)

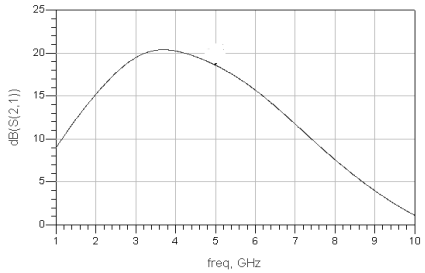

Figure13.(c)

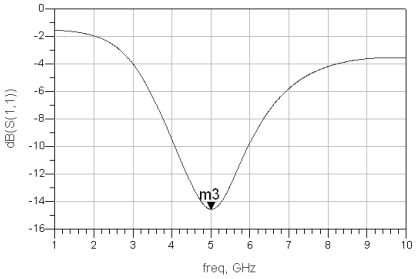

Figure13.(d)

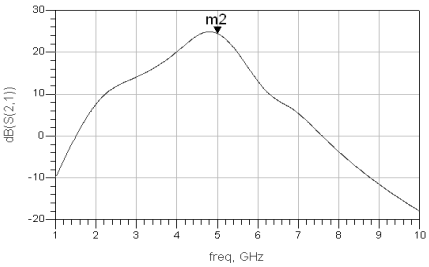

Figure13.(e)

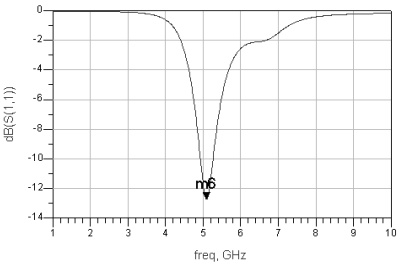

Figure13.(f)

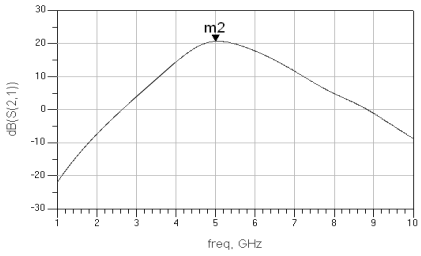

Figure 13.(g)

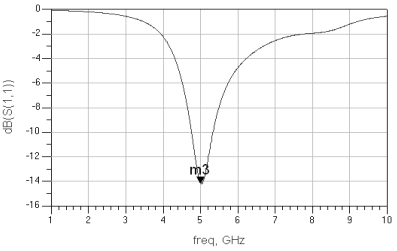

Figure13.(h)

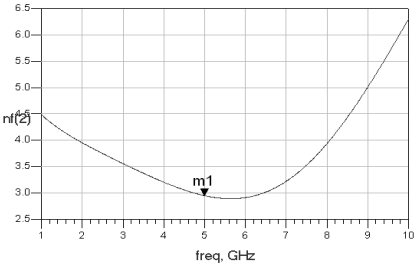

Figure14. (a)

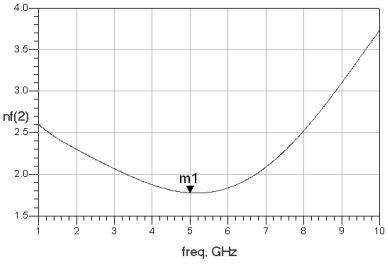

Figure14. (b)

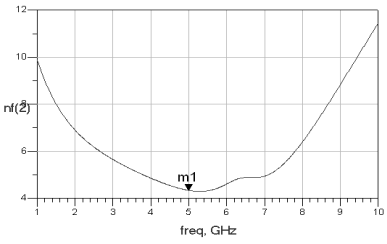

Figure14. (c)

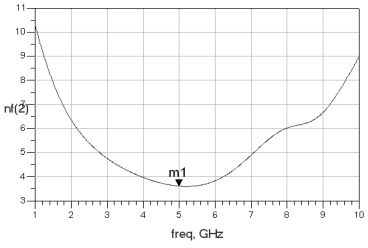

Figure14. (d)

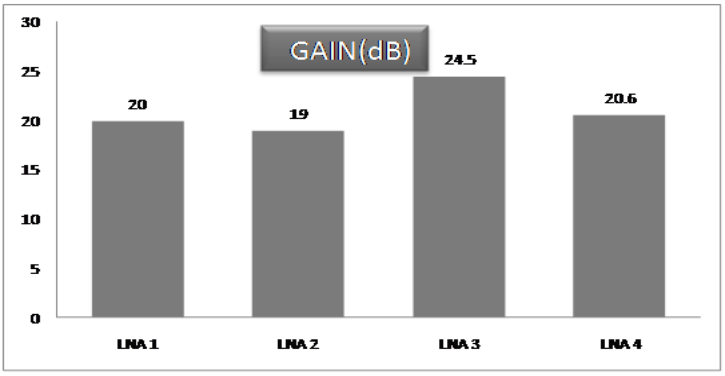

Figure15. Gain Comparison

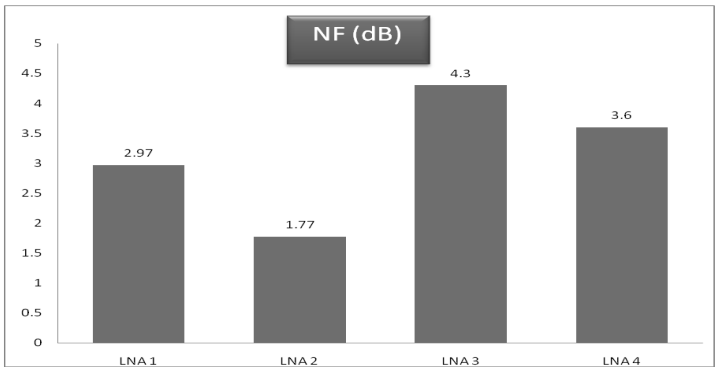

Figure16. NF Comparison

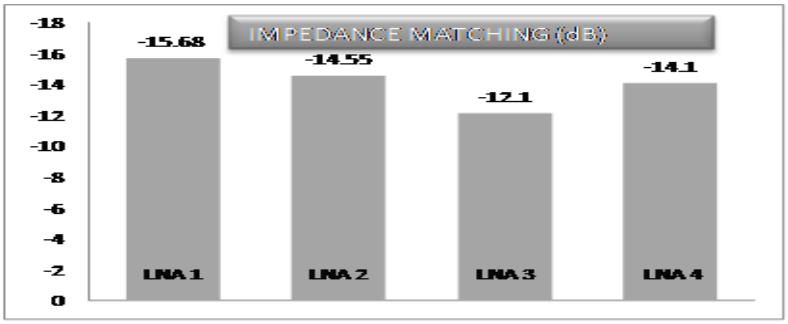

Figure17. Input Impedance Matching Comparison

5. Conclusion

The conventional LNA design techniques have been reviewed and four LNA design structures proposed whose performance analyzed using Agilent's ADS version9.0 software. All designs are evaluated using the supply voltage of 1.8V. The design principles, advantages and limitations of single-ended, differential LNA are discussed. From the simulation results, it is observed that LNA 1 and 2 shows good response by satisfying the noise figure value which is less than 3dB and meets the requirement of narrow band LNA design. LNA 3 exhibits both gain and NF high whereas LNA 2 exhibits little deviation in peak gain at centre frequency. But, LNA 4 shows good agreement with theoretical calculations and simulation results in all three performance factors.

The 5-GHz dual CS differential LNA exhibits the power gain of 20.6dB, input matching of -14.1dB and noise figure of 3.6 dB. The first two designs will require lesser active area in implementation than other two designs because the structures are very simple but it needs additional balun circuitry for transforming the single-ended output into differential output. Further this work can be extended for developing layouts and GDS II files.

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