A Fault Dictionary-Based Fault Diagnosis Approach for CMOS Analog Integrated Circuits

Mouna Karmani*, Chiraz Khedhiri*, Belgacem Hamdi* & Brahim Bensalem**

*Electronics and Microelectronics Laboratory, Monastir, Tunisia
**Embedded and Communication Group, Intel Corporation, Chandler, AZ, USA
mouna.karmani@yahoo.fr

Abstract:

In this paper, we propose a simulation-before-test (SBT) fault diagnosis methodology based on the use of a fault dictionary approach. This technique allows the detection and localization of the most likely defects of open-circuit type occurring in Complementary Metal–Oxide–Semiconductor (CMOS) analog integrated circuits (ICs) interconnects. The fault dictionary is built by simulating the most likely defects causing the faults to be detected at the layout level. Then, for each injected fault, the spectre's frequency responses and the power consumption obtained by simulation are stored in a table which constitutes the fault dictionary. In fact, each line in the fault dictionary constitutes a fault signature used to identify and locate a considered defect. When testing, the circuit under test is excited with the same stimulus, and the responses obtained are compared to the stored ones. To prove the efficiency of the proposed technique, a full custom CMOS operational amplifier is implemented in 0.25 µm technology and the most likely faults of open-circuit type are deliberately injected and simulated at the layout level.

Keywords:

Analog testing, fault diagnosis, fault dictionary, Fast Fourier Transform (FFT), power consumption, open-circuit fault.

INTRODUCTION

The evolutionary trend in very large scale integrated (VLSI) circuits technology fuelled by fierce industrial competition to reduce integrated circuits cost and time to market has driven to design and manufacture very complex ICs including digital, analog and mixed parts in the same chip, this approach is known as system-on-chip (SoC). Due to the increasing complexity and chip scale of SoCs, design and testing have become a real challenge to ensure the functionality and quality of the product [1-2].

The SoC design approach increases the testing complexity of the system, in particular testing of the analog blocks embedded in mixed-signal or analog cores [3]. The high analog test cost is due to many factors, such as expensive test equipment, long test development time, and long test production time [4]. Analog circuits testing difficulties are also caused by accessibility problems and by lack of common test strategies and standards. Due to those difficulties, fault diagnosis and testing techniques for analog and mixed signal circuits are gaining importance.

DOI : 10.5121/vlsic.2011.2301

The testing phase is one of the most important tasks in design and manufacturing of ICs. The role of testing is to detect whether something is wrong and the role of diagnosis is to determine exactly what is wrong, and where the process needs to be altered [5].

There are two approaches to fault diagnosis in analog circuits: simulation-before-test (SBT) including probabilistic and fault dictionary techniques and simulation-after-test (SAT) including optimization, fault verification, and parameter identification techniques [6].

The paper is organised as follows. Section 1 presents the physical defects and fault modelling in CMOS analog circuits. The proposed test approach is presented in section 2. A case is studied in sections 3 and 4. Finally we conclude in section 5.

1. PHYSICAL DEFECTS IN CMOS ANALOG INTEGRATED CIRCUITS

In analog CMOS technology, faults are further classified into catastrophic (open and bridging) and parametric faults. When a catastrophic defect occurs, the topology of the circuit is changed. In fact, a bridging defect is a short circuit between two or more nets on a die [7]. While an open circuit defect can result from missing metal material in the transistor interconnects.
In this paper, we address the most likely defects of open-circuit type occurring in analog CMOS circuits during the manufacturing process.

I_{DDQ} testing is a popular technique used to detect defects causing quiescent current elevation in VLSI CMOS circuits. This technique involves online monitoring of the power supply current. Usually, bridging faults induce an elevated I_{DDQ} current. Consequently these faults can be easily detected using a Built In Current Sensor (BICS) [1-9]. On the other side, open circuit faults, may decrease or cause only a small rise in I_{DDQ} current that can not be detected by the built in current sensor. Accordingly, I_{DDQ} testing cannot detect some of the open faults which result in decrease of the quiescent current. However, it has been shown that I_{DDQ} testing can be an excellent complement test [10].

In this paper, we consider that the use of I_{DDQ} testing with the proposed technique involves the coverage of catastrophic (open and short) and parametric faults in CMOS analog ICs.

2. THE PROPOSED TEST APPROACH

In this section, we introduce a novel test technique that serves to diagnose analog ICs, and distinguish a fault free from a faulty circuit with respect to open defects model. This technique is based on analysing both FFT of the output signal and the power consumption of the circuit under test.

On the other hand, the Fast Fourier Transform (FFT) provides the means of transforming a signal defined in the time domain into one defined in the frequency domain. It has been widely used in signal processing and instrumentation which are based on spectral analysis [11], [8].

The measured power consumption in our methodology is the average power consumed by the faulty circuit. Its value is obtained by SPICE simulation. In this work, we show that the value of this power is fault dependent. In fact, each open circuit injected in the circuit under test causes a well-defined and specific power consumption value that can be used to detect the fault and even locate the defect. In our investigation, we prove that the correlation between the injected fault and

its power consumption, and FFT spectrum can be used as unique signature to build the fault dictionary. The proposed test procedure consists of six steps:

Step 1: defining the target set of faults:

The set of faults to be tested is previously defined. This set contains typical parametric and catastrophic faults. The set of faults to consider is the most likely faults type open-circuit occurring during the manufacturing process of ICs. This set of faults includes defects in contacts metal/poly, N+ diffusion /metal and P+ diffusion /metal.

Fig.1 and fig.2 illustrate low leakage NMOS and PMOS transistors at the layout level.

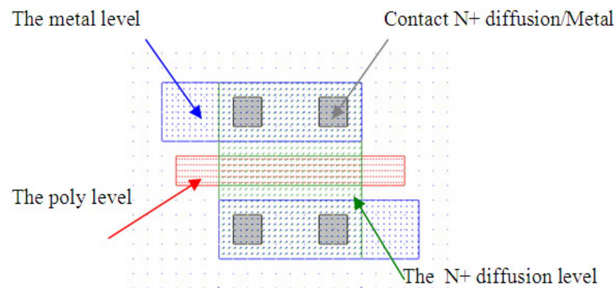

Figure 1: Low leakage NMOS Transistor at the layout level

In fact, the NMOS transistor contains N+diffusion/metal contacts which connect the metal and the N+diffusion levels in order to form the drain and the source of the considered transistor.

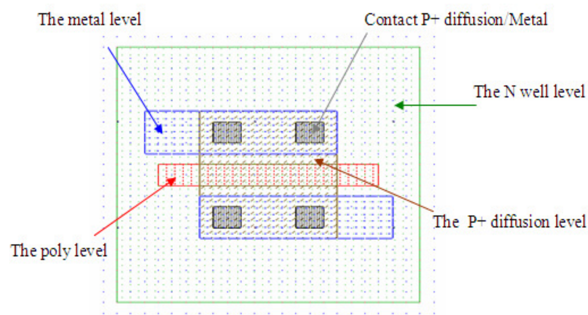

Figure 2: Low leakage PMOS Transistor at the layout level

As shown in the figure above, the PMOS transistor contains P+diffusion/metal contacts which connect the metal and the P+diffusion levels in order to form the drain and the source of the considered transistor.

The figure below presents an NMOS mirror current containing a Metal/ploy contact.

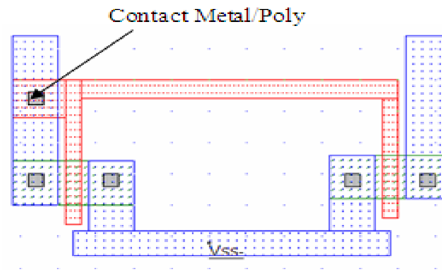

Figure 3: NMOS mirror current containing a Metal/Poly contact

The most likely defects of open-circuit type occurring in analog CMOS circuits during the manufacturing process can be simulated by providing a realistic missing material in the transistor interconnects at the layout level.

Step 2: Defining the set of test measurements:

This set includes all properties and test parameters which can be monitored during the test phase. In the case study section, we consider the FFT spectrum of the output signal of the CMOS OPA with injection of the faults under investigation. In addition, we consider the value of power consumed by the IC during the test time.

Step 3: Selection of the stimulus signal:

The stimuli used are sinusoidal waveforms. So, the first step is to choose the adequate input amplitude and frequencies. The input signal amplitude should not saturate the circuit (e.g. filter, amplifier) in the absence of faults. Thus, the frequency value applied must optimize the observability of all faults. Therefore, selected frequency range should allow the detection and location of most open faults occurring in the circuit under test. This problem is solved by successive simulation runs to determine optimal values of amplitude and frequency range.

Step 4: Fault injection and circuit simulation:

Defects causing the faults to be detected are injected and simulated at post-layout level. Furthermore, for each defect injected, an FFT analysis and a power consumption measurement are performed on the faulty circuit to be compared to the fault-free ones.

The set of faulty responses constitute the faulty signature of the circuit under test. Obtaining the faulty signature constitutes the first step to build the fault dictionary.

Step 5: Fault dictionary construction:

The fault dictionary is a collection of potential faulty and fault-free responses. The signatures obtained will be stored in the dictionary. This dictionary involves for each fault a correspondence between the faulty circuit responses and the defect sites.

When testing, the circuit under test is excited with the same input stimulus. The response parameters obtained are compared to the stored ones and the most similar one will be taken as solution.

Step 6: Physical defect characterization

Once the fault is detected and the defect site is located, we proceed to the physical characterization of the defect. The test is considered achieved and conclusive when the failure causing the defect is determined, localized and corrected.

3. CASE STUDY

In order to evaluate the merit of the proposed test technique, we apply the above mentioned test procedure steps on an operational amplifier circuit (OPA).

3.1. The CMOS operational amplifier

The operational amplifier (OPA) under test is a two stage amplifier, having a differential input amplifier and single-ended output stage. In general, an operational amplifier has three functional blocks [12]:

- A differential stage input to amplify the differential input of the amplifier.
- A floor conversion following the differential amplifier stage is responsible to producing a single output which is referenced to the ground.
- A secondary gain stage having an active common source to obtain an additional gain.

Fig.4 shows the circuit of the operational CMOS amplifier.

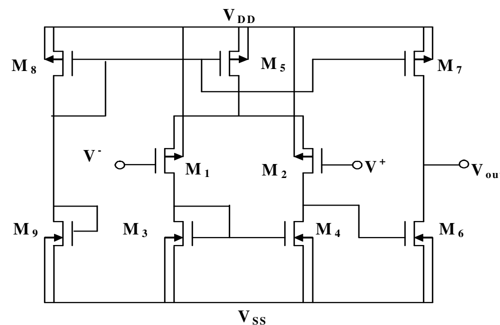

Figure 4: CMOS operational amplifier

The first floor of this CMOS amplifier includes a PMOS source coupled differential pair transistors M_1 and M_2, a current mirror with N-channel formed by the two transistors M_3 and M_4, a current mirror p-channel formed by two transistors M_8 and M_5 and active resistance composed by the N-channel transistor M_9. The second stage amplifier contains a common source N-channel formed by the transistor M_6 loaded by the current source formed by P-channel transistor M_7 [12].

The transistors are sized to have a bias current of 100µA intensity and an amplifier's quiescent current I_{DDQ} equal to 500µA. The operational amplifier is implemented in full-custom 0.25µm CMOS technology [13]. For this technology, the appropriate supply voltage VDD is equal to 2.5V while VSS is the ground (GND). SPICE simulations of the post-layout extracted OPA, which includes all parasitic, are used to demonstrate that this amplifier has an acceptable electrical behaviour. The layout of the amplifier is as shown in Fig.5.

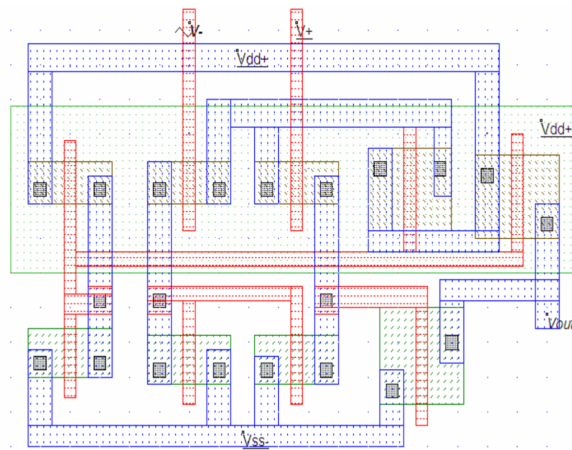

Figure 5: Layout of the operational amplifier in full-custom 0.25µm CMOS technology

a. Simulation Results

The Spice simulation results of the CMOS operational amplifier are shown in Fig.6 and Fig.7.

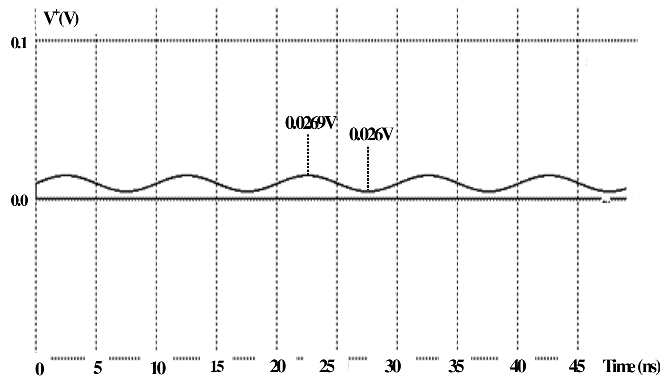

Figure 6: Input of the CMOS Operational Amplifier

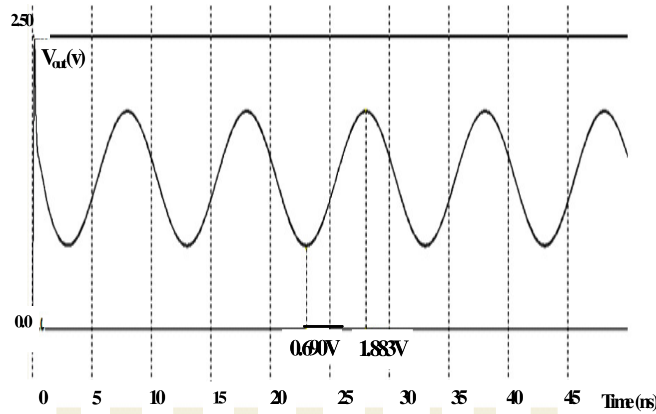

Figure 7: Output of the CMOS Operational Amplifier

The input and the output of the OPA are sinusoidal waveforms and its open loop gain is equal to 42.5 dB.

3.2. I_{DDQ} current in the fault free circuit

Fig.8 shows the I_{DDQ} current waveform of the OPA.

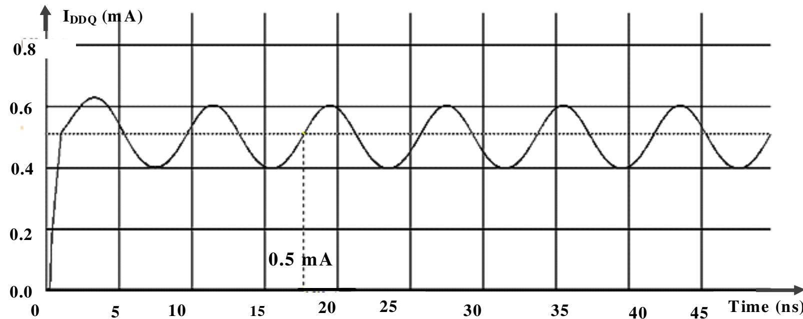

Figure 8: I_{DDQ} current of the fault free OPA

Figure 8 demonstrates the I_{DDQ} current of the fault free OPA circuit. The average value of this current is equal to 0.5 mA as expected. We note also, that all bridging faults involve a large difference between normal operating current and current under faulted condition. These faults can be, therefore, detected by I_{DDQ} testing. However, it is not the case for open circuit faults. The proposed test technique is adequate for these faults, which are not covered by I_{DDQ} testing.

Thus, when the value of the I_{DDQ} current is 0.5 mA we assume that there are no short-circuit defects, but it is not guaranteed that the circuit don't contain open-circuit defects.

3.3. I_{DDQ} current in the faulty circuit

We now inject a single bridging fault in the OPA between the source and the gate of the transistor M_5 as shown in Fig.9. This Bridging fault is placed in the CMOS amplifier design using fault injection NMOS transistors (FIT).

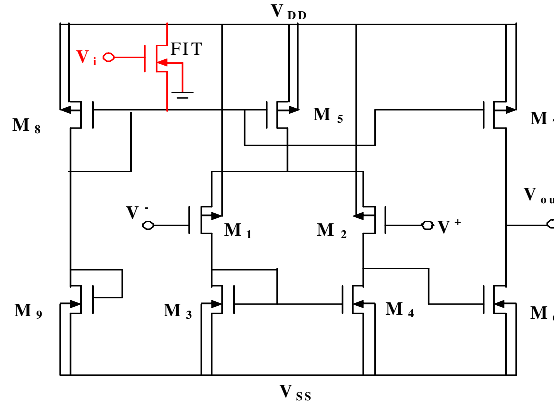

Figure 9: injection of a bridging fault between the source and the gate of the M5 transistor

When the gate of the fault injection transistor is connected to V_{DD}, the FIT is activated and consequently the fault is injected [1]. Figure 10 shows the I_{DDQ} current waveform in presence of the bridging fault.

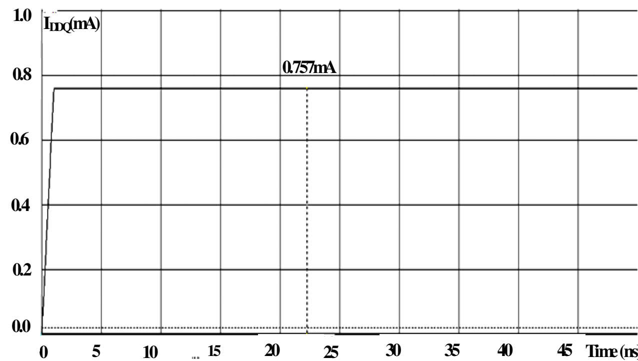

Figure 10: I_{DDQ} waveform current when the bridging fault is inserted in OPA of figure 8

We can notice the increase of the I_{DDQ} current that was sensitive to the fault injected between the source and gate of the transistor M_5. The I_{DDQ} current value is equal to 0.757mA. In fact, this value should be equal to 0.5 mA in absence of any bridging fault. This increase in current which is equal to 257 µA can be easily detected using a well dimensioned built in current sensor (BICS).

I_{DDQ} testing technique is efficient for bridging defects which induce the increase in the I_{DDQ} current. However, it is not appropriate for open circuit defects because, in most cases, this type of defect engenders the reduction of this current and then it goes undetected.

To illustrate the idea, we inject an open circuit defect in the contact metal/poly connecting the gate and the drain of the transistor M_3.

Fig.11 shows the I_{DDQ} current waveform after the injection of this defect.

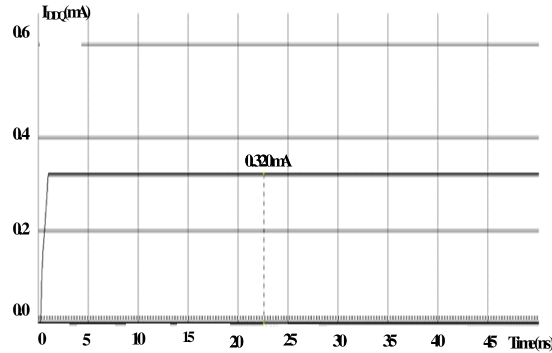

Figure 11: I_{DDQ} current waveform with an open circuit defect in the contact metal /poly of the transistor M3

The I_{DDQ} current value is equal to 0.320 mA. Thus, the injection of the open circuit defect causes a decrease of the I_{DDQ} current. Fig.12 shows the I_{DDQ} current waveform after the injection of another open circuit defect in the contact metal /poly of the transistor M_9.

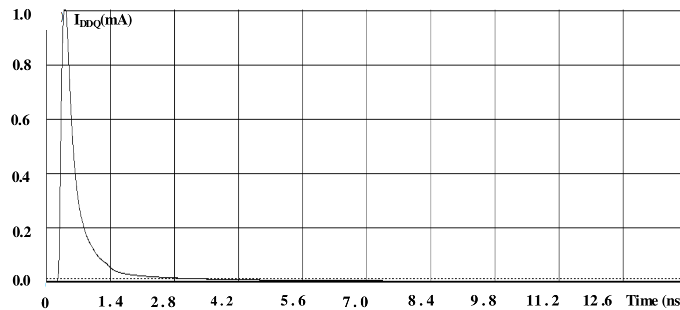

Figure 12: I_{DDQ} current waveform with an open circuit defect in the contact metal /poly of the transistor M9

In this case, the current I_{DDQ} flowing in the circuit decreases until reaching 0 mA.

4. Proposed technique applied to the OPA circuit

4.1. The fault-free circuit simulation results

In order to check the circuit's capability for realistic circuit defects, we simulate the amplifier in absence of any fault. The frequency of the input signal is fixed at 125MHZ and the power consumption is 1.218 mW. The simulation result is shown in Figure 13.

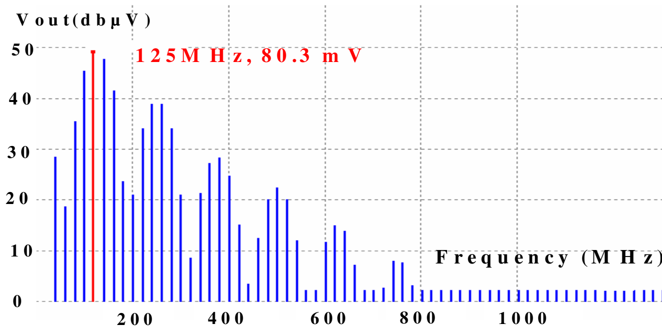

Figure 13: FFT specter of the output signal ofthe fault free circuit

Figure 13 shows the FFT of the output signal of the faulty free CMOS amplifier. From this figure, we notice that the fundamental frequency of the output signal is also equal to 125MHZ as the input frequency signal. In absence of any fault, the FFT presents a fundamental's amplitude equal to 80.3 mV and 5 harmonics.

4.2.The faulty circuit simulation results

To prove the efficiency of the proposed approach some likelihood faults type open-circuit are intentionally injected in the layout of the OPA.

4.2.1. Fault 1

The first fault (Fault 1) simulated is an open in the contact metal/poly connecting the gate and the drain of the active resistance formed by the transistor M_9 as shown by the Fig.14.

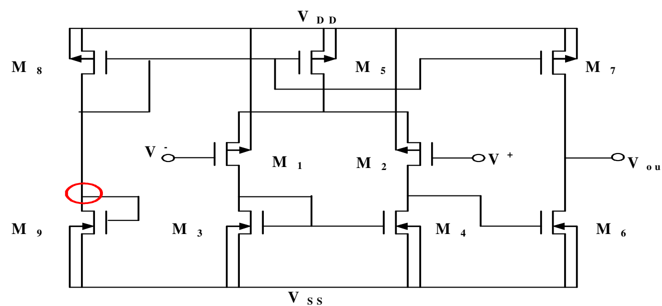

Figure 14: Fault 1

Figure 15 (a) and 15 (b) shows the FFT of the output signal of the faulty CMOS amplifier when fault1 is injected at two different spots.

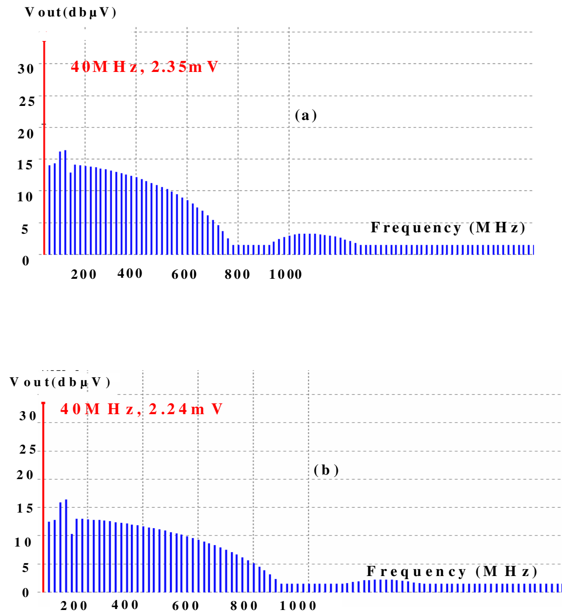

Figure 15: FFT of the output signal of the CMOS OPA:
(a) FFT response when Fault 1 is injected in the metal
(b) FFT response when Fault 1 is injected in the poly

We notice that the open circuit defect injected at the metal or at the poly level not only changes the FFT spectre shape but also the fundamental frequency from 125MHz to 40 MHz.

When the fault is injected at the metal level, the fundamental amplitude is equal to 2.35 mV while the power dissipated decreases to reach 3.193 µW. When the fault is injected at the poly level the fundamental amplitude is equal to 2.24 mV while the power dissipated decreases to reach 0.743µW (see table 1).

	Metal	Poly
Frequency (MHZ)	40	40
Amplitude of the fundamental (mV)	2.35	2.24
Power Consumption (µW)	3.193	0.743

TABLE 1: SIMULATION RESULT SUMMARY OF THE FAULTY CIRCUIT

4.2.2. FAULT 2

The second injected and simulated fault (Fault 2) is an open in the contact metal/poly connecting the gate and the drain of the transistor M_3. Figure 16 shows the location of this fault.

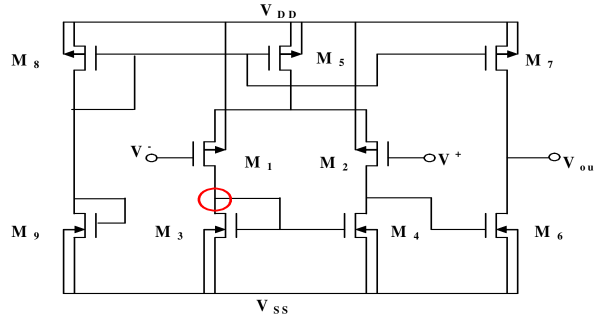

Figure 16: Fault 2

Fig.17 shows the FFT of the output signal of the faulty CMOS amplifier.

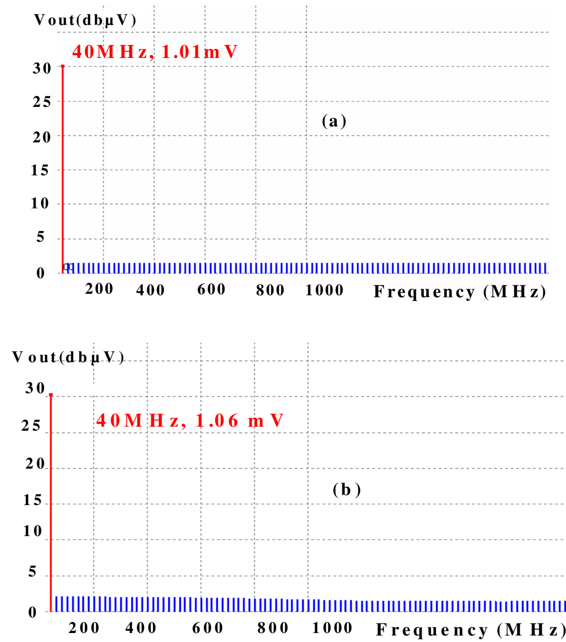

Figure 17: FFT of the output signal of the CMOS AOP.
(a): fault 2 in metal, (b): fault 2in poly

	Metal	Poly
Frequency (MHZ)	40	40
Amplitude of the fundamental (mV)	1.01	1.06
Power Consumption (µW)	1.19	1.179

TABLE 2: SIMULATION RESULT SUMMARY OF THE FAULTY CIRCUIT

From Table 2, we deduce that the injection of the defect in either the metal or the poly generates the same fundamental frequency but it changes the amplitude of the fundamental frequency and the power dissipated by the circuit.

4.2.3. Fault 3

The third fault injected and simulated is an open in the contact metal / poly connecting the gate of the transistor M_6 and the drain of the transistor M_4. Fig.18 shows the location of this fault.

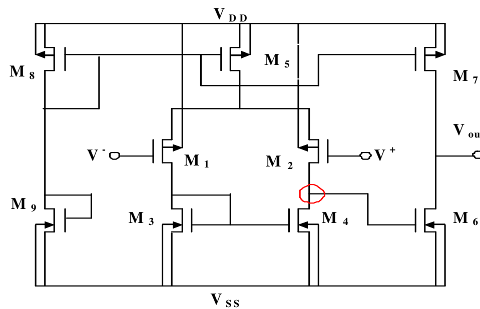

Figure 18: Fault 3

Figure 19 presents the FFT of the output signal of the faulty CMOS amplifier.

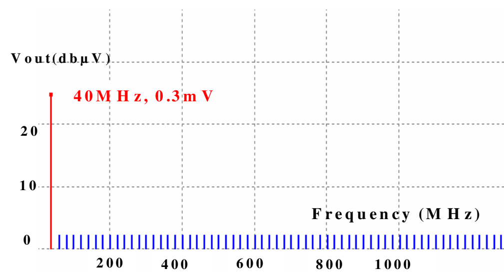

Figure 19: FFT of the output signal of the CMOS OPA under the Fault 3 (in the Metal or in the Poly)

In this case, we obtain the same FFT spectrum either at the metal or at the poly level. But only the power consumption has changed as it is indicated in the table below.

	Metal	Poly
Frequency (MHZ)	40	40
Amplitude of the fundamental (mV)	0.3	0.3
Power Consumption (µW)	0.793	0.644

TABLE 3: RESULT SIMULATION SUMMARY OF THE FAULTY CIRCUIT

4.2.4. FAULT 4

The open fault is injected in the contact metal / poly connecting the gate and the drain of the transistor M_8 as shown in Figure 20.

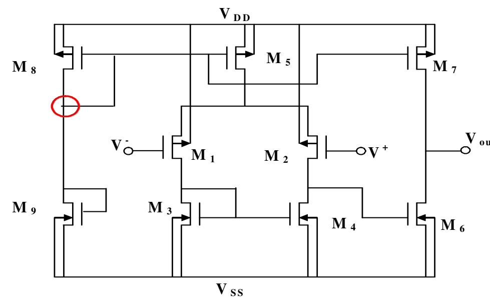

Figure 20: Fault 4.

Fig.21 presents the FFT of the output signal of the faulty CMOS amplifier.

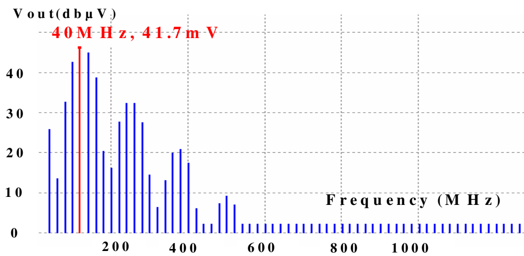

Figure 21: FFT of the output signal of the CMOS OPA in presence of the Fault 4 (in the Metal or in the Poly).

Also, in this case, we obtain the same FFT spectrum either at the metal or at the poly level, the same fundamental amplitude and the same power consumption as it is indicated in the table below.

	Metal	Poly
Frequency (MHZ)	125	125
Amplitude of the fundamental (mV)	41.7	41.7
Power Consumption (µW)	1.917	1.917

TABLE 4: SIMULATION RESULT SUMMARY OF THE FAULTY CIRCUIT

4.2.5. FAULT 5

Fault 5 consists of injection of an open in the contact N+ diffusion/metal of the transistor M_9. Figure 22 presents the FFT of the output signal of the CMOS amplifier under Fault 5.

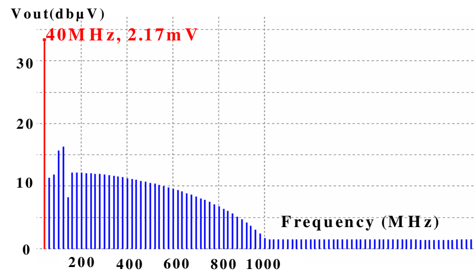

Figure 22: FFT of the output signal of the CMOS AOP with injection of Fault 5.

Table 5 shows the frequency and the amplitude of the fundamental and the power consumed by the circuit after the injection of fault 5.

	Metal	N+ diffusion
Frequency (MHZ)	40	40
Amplitude of the fundamental (mV)	2.17	2.17
Power Consumption (µW)	3.771	3.797

TABLE 5: RESULT SIMULATION SUMMARY OF THE FAULTY CIRCUIT

In the same way, we have simulated all open circuit defects that can occur in all contacts N+ diffusion/metal existing in the CMOS operational amplifier.

4.2.6. Fault 6

Open fault is injected in the contact P+ diffusion/metal of the transistor M_1. Fig.23 presents the FFT of the output signal of the faulty CMOS amplifier.

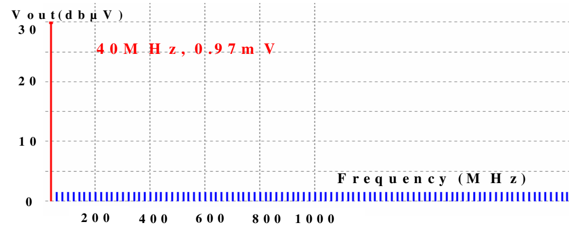

Figure 23: FFT under the Fault 6.

Table 6 summarizes the different results obtained after the injection of fault 6.

	Metal	P+ diffusion
Frequency (MHZ)	40	40
Amplitude of the fundamental (mV)	0.97	0.97
Power Consumption (µW)	1179	1179

TABLE 6: simulation result summary of the faulty circuit

From Table 6, we deduce that the injection of the defect in either the metal or the P+ diffusion generates the same fundamental frequency, the same amplitude of the fundamental and the same power dissipated by the circuit. In the same way, we have simulated all open circuit defects that can occur in all contacts P+ diffusion/metal existing in the CMOS operational amplifier.

4.2.7. Building the fault dictionary

Fault diagnosis is important in improving the design process and the manufacturing yield of ICs. In this work, a fault dictionary is used to detect and locate the open faults that can occur in the OPA. The dictionary is built by simulating the post-layout circuit and injecting the defects. Then, the responses corresponding to each fault considered (Frequency, Fundamental amplitude, Power consumption) are stored in a table. The table 7 presents this dictionary.

In the failure analysis laboratory, the circuit under test is excited with the same input stimulus chosen while building the fault dictionary. Using appropriate test equipment, the next step is to obtain the output FFT spectre and the power consumption value of the circuit under test. Then, the responses obtained are compared with the stored ones.

As shown in table 7, the fault dictionary table is divided in two parts: the fault signature and the defect localisation. The fault signature part contains the frequency, the fundamental amplitude and the power consumption of the circuit under test. Using this signature we can locate the defect site.

Fault signature			*Defect localisation*		
f (MHZ)	Fondamental amplitude (mV)	Power Consumption (µW)	Defect	Defect site	
				Tr	Contact
40	0.3	391	D1	M5	P+/M
40	0.3	644	D2	M2	P+/M
40	0.3	646	D3	M3D	N+/M
40	0.31	646	D4	M3S	N+/M
40	0	792	D5	M7	P+/M
40	0.23	793	D6	M6S	N+/M
40	0.3	793	D7	M6D	N+/M
125	41.7	990	D8	M8	P+/M
40	0.97	1179	D9	M1	P+/M
125	80.3	1218	No Defect	Fault free	Fault free
40	0.98	1432	D10	M4S	N+/M
40	1	1432	D11	M4S	N+/M
40	1.09	1432	D12	M4D	N+/M
125	41.7	1917	D13	M8	M/POLY
40	0.3	0.644	D14	M6	M/POLY
40	2.24	0.743	D15	M9	M/POLY
40	0.3	0.793	D16	M4D	M/POLY
40	1.06	1.179	D17	M3	M/POLY
40	1.01	1.19	D18	M3	M/POLY
40	2.35	3.193	D19	M9	M/POLY
40	2.17	3.771	D20	M9S	N+/M
40	2.17	3.797	D21	M9S	N+/M
40	2.16	4.073	D22	M9D	N+/M
40	2.17	4.175	D23	M9D	N+/M

Table 7: The fault dictionary Where f is the Frequency and Tr is the Transistor

The defect localisation part presents for each fault signature the corresponding defect noted D_i (i is the defect number). For each defect D_i we present the defect site which specifies the transistor number (D designs the drain and S designs the source) and the corresponding contact.

The fault dictionary developed is used to quickly locate the defect site and identify the failure mechanism causing abnormal behaviour of the circuit under test and low manufacturing yields. To more clarify this table let's take some examples. The following examples are given to explain how to use the abacus to detect and locate the fault.

- **M**/Poly: the defect is located in the contact Metal /Poly at the metal level.
- M/**Poly**: the fault is located in the contact metal /Poly at the Poly level.
- **M/Poly**: the fault is located in the contact metal /Poly and can be at the metal or at the Poly level.

In absence of any fault the frequency of the fundamental is equal to 125 MHz, the fundamental amplitude is 80.3 mV and the power consumption is 1218 µW. These values correspond to the signature of the fault free circuit.

When the frequency of the output of the OPA is 40MHZ, the fundamental amplitude is 0.3mV and the power consumption is equal to 793µW we consider that the circuit is faulty and the defect corresponding is D7. Consequently, this fault signature correspond to an open circuit defect located at the metal or at the N+ diffusion level in the contact N+ diffusion/Metal connecting the drain and the N+ diffusion of the transistor M6.

When the frequency of the output of the OPA is 125MHZ, the fundamental amplitude is 41.7 mV and the power consumption is equal to 990µW we consider that the circuit is faulty and the defect corresponding is D8. So, this faulty signature correspond to an open circuit defect which can be located either at the metal or at the P+ diffusion level in the contact P+ diffusion/Metal of the transistor M8.Conclusion

5. CONCLUSION

This paper has presented a novel test methodology based on a fault dictionary for the detection of open circuit faults occurring in CMOS analog circuits.

The method is based on comparing the spectral analysis and power consumption measurement of the fault free and faulty circuit. We used post-layout circuit to insure that parasitic are included and the model is realistic.

This approach is able to discriminate between the fault free circuit and the faulty one with respect to open fault model. It is also capable of localizing the defect site using the fault dictionary. Simulation results show that the technique is effective and can easily be implemented in the SOC environment. It can also be easily used with an I_{DDQ} testing technique to achieve coverage of catastrophic faults (open and short) in the analog blocks or analog functions embedded in mixed-signal or analog cores. As a future work, we can plan extending the proposed technique to multiple fault analog circuit testing and analysis.

REFERENCES

[1] M.Karmani, C.Khedhiri and B.Hamdi, "Design and test challenges in Nano-scale analog and mixed CMOS technology", International Journal of of VLSI design & Communication Systems, 2011.

[2] M.White, Yuan Chen, "Scaled CMOS Technology Reliability Users Guide", NASA Electronic Parts and Packaging (NEPP) Program, 2008.

[3] Y. Zorian, E. J. Marinissen, System Chip Test: How Will It Impact Your Design, Design Automation Conference - DAC, pp. 136-141, 2000

[4] P. Kalpana, K. Gunavathi, "Fault oriented Test Pattern Generator for Digital to Analog converters", Academic Open Internet Journal, Volume 13, 2004.

[5] M. BUSHNELL, A.VISHWANI, "ESSENTIALS OF ELECTRONIC TESTING FOR DIGITAL, MEMORY, AND MIXED-SIGNAL VLSI CIRCUITS", (2002).

[6] JA. Starzyk, D.Liu, Z. Liu, E. Nelson, and JO. Rutkowski, "Entropy-Based Optimum Test Points Selection for Analog Fault Dictionary Techniques", IEEE transactions on instrumentation and measurement, VOL. 53, NO. 3, 2004.

[7] National Technology Roadmap for Semiconductors, 1994.

[8] J. A. Abraham, W. K. Fuchs, "Fault and Error Models for VLSI", IEEE Proceedings, Vol. 74, No. 5, pp. 639-654, 1986.

[9] J. Figueras, Anna M. Borsa, A. Ferré, Test challenges in nanometric CMOS technologies Microelectronic Engineering, Volume 49, Issues 1-2, pp. 119-133, 1999.

[10] A. Ferré, E., Isern, J. Rius, R. Rodríguez-Montañés, J. Figueras, I_{DDQ} testing: state of the art and future trends, Integration, the VLSI Journal, Volume 26, Issues 1-2, pp 167-196, 1998.

[11] G. A. Zimmerman and S. Gulokis, Polyphase-Discrete Fourier Transform Spectrum Analysis for the Search for Extraterrestrial Intelligence, TDA Progress Report 42-107, Vol,1991.

[12] K. Pavan Alli, Testing a CMOS operational amplifier circuit using a combination of oscillation and I_{DDQ} test methods, Thesis, Osmania University, 2004.

[13] E. SICARD, Microwind and Dsch version 3. 1, INSA Toulouse, ISBN 2-87649-050-1, 2006.