A 80Ms/sec 10bit PIPELINED ADC Using 1.5Bit Stages And Built-in Digital Error Correction Logic

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Abstract

Use of pipelined ADCs is becoming increasingly popular both as stand alone parts and as embedded functional units in SOC design. They have acceptable resolution and high speed of operation and can be placed in relatively small area. The design is implemented in 0.18uM CMOS process. The design includes a folded cascode op-amp with a unity gain frequency of 200MHz at 88 deg. Phase margin and a dc gain of 75dB. The circuit employs a built in sample and hold circuit and a three phase non-overlapping clock.

Keywords

ADC, 1.5 bit stage, CMFB, Pipeline, Redundancy bit removal algorithm

1. INTRODUCTION

High resolution, high speed CMOS ADCs are used for scanners, high definition TVs, medical equipment, camcorders and radar systems and are limited to 10 bits because of various reasons. In this work, a fully differential 10 bit ADC was implemented using an inherent digital error correction technique. The fully differential Folded Cascode op-amp architecture is used. Power dissipation in op-amp can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both[10]. As the input current is lowered though power dissipation is reduced, the dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. The design takes care of power optimization at every level of design. The block diagram of general Pipelined ADC is shown in Fig. (1). Each stage contains a S/H circuit, a low resolution A/D subconverter, a low resolution D/A converter and a differencing fixed gain amplifier. Flash and subranging architectures need exponential rather than linear increase in area to increase their resolution and also require trimming and calibration. But for pipelined converters, area is small and is linearly related to the resolution because the resolution can be increased by adding stages to the end of the pipeline without increasing the number of clock phases required per conversion.

2. OP-AMP REQUIREMENTS FOR ADCs

The typical gain and phase responses of an op-amp are shown in fig.(2). The bandwidth and gain characteristics are crucial in the design of data converters. The op-amp is preferred to have 90^{o}

phase margin over full load conditions and process variations to avoid second order step response and its associated ringing.

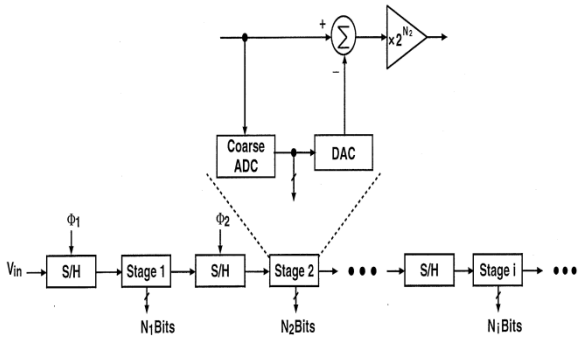

Figure 1. Block diagram of pipelined ADC

Decreasing the phase margin results in an increase of amplitude of ringing and this can increase the settling time. It can be proved that the DC open loop gain of an op-amp used in an ADC must satisfy the condition[1]

$$A_{ol} >= 2^{N+2}$$

Where N is the no. of bits of conversion. For example a 10 Bit data converter needs a minimum DC open loop gain of 2^{12} . The speed of an op-amp is decided by the op-amp used. The minimum unity gain frequency (f_u) for a given settling time ($t_s < 1/f_{clk}$) required to settle the output to within ± ½ LSB of its final value can be evaluated as[1]

$$f_u >= 0.22\ (N+1)\ f_{clk\_}$$

i.e. for a 10 bit ADC at 80 MHz clock frequency needs an op-amp with a unity gain frequency of around 200 MHz.

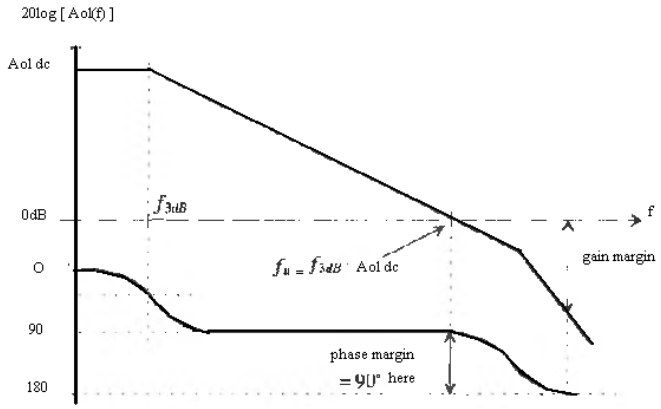

Figure 2. Magnitude and phase response of an op-amp

2.1. Folded Cascode Op-Amp

Modern integrated CMOS op-amps are designed to drive capacitive loads[7][8]. With only a capacitive load it is not necessary to use a buffer at the output for a low impedance node. Therefore, it is possible to design op-amps at higher speeds and larger voltage swings than those which drives resistive loads. These improvements are achieved with a single high impedance node at the output that drives only capacitive loads. For folded cascode op-amps the compensation is achieved by C_L itself and it is dominant pole compensation. As C_L increases, the op-amp stability improves but is slowed down. The folded cascode op-amp schematic is shown in Fig. (3).

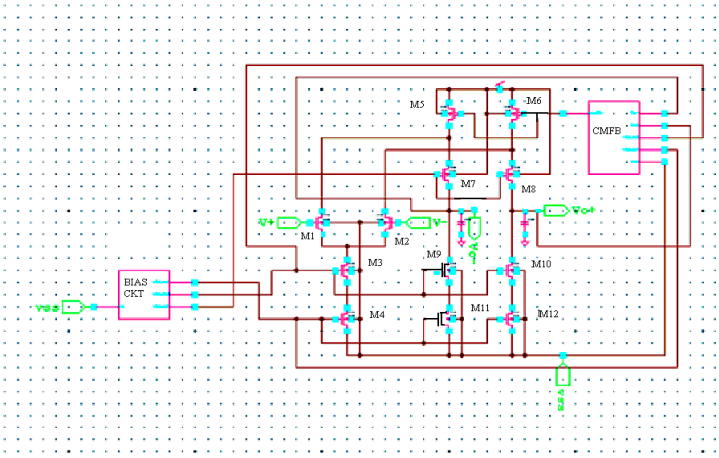

Figure 3. Fully differential folded cascode op-amp

The basic idea of folded cascode op-amp is to apply the opposite type PMOS cascode transistors to the input differential pair of NMOS type. This arrangement allows the output to be taken at the same bias levels as that of input signal. Even though it is a single stage, the gain is reasonable since the gain is decided by the product of input transconductance and the large output impedance. Applying AC input voltage v_{in} causes the drain of differential stage to be $g_m v_{in}$. This AC drain current is mirrored in the cascaded MOSFETs M7-M12.the output voltage of folded cascode is then

$$V_{out} = g_m \, v_{in} \, R_{out} . \quad \text{Where}$$

$$R_{out} = [(\text{R looking back into the drain of M10}) \text{ II } (\text{R looking into the drain of M8})].$$

$$= [r_{out10} (1 + g_{m10} \, r_{out12})] \text{ II } [r_{out8} (1 + g_{m8} r_{out6})]$$

The gain of folded cascode op-amp is then

$$A = v_{out} / v_{in} = g_m \, R_{out} . \ldots\ldots\ldots (1)$$

The dominant pole of the op-amp is at $1 / 2 \prod R_{out} C_L$.
Parasitic poles exist at M7/M8 & M9/M10 combination. These parasitic poles must be larger than the unity gain frequency of the op-amp given by

$$Fu = g_m / 2 \prod C_L . \ldots\ldots (2)$$

For the required unity gain frequency and for a given transistor $g_{m,}$ C_L is evaluated using eq. (2).

2.2. Biasing circuit

The bias voltages are generated using the circuit shown in fig. (4). The circuit basically has two wide swing current mirrors. M1 and M2 are sized ¼ of the size of other MOSFETs. If current through resistor, I = 5uA, then this biasing scheme results in 5uA to flow in M13 and M14 of figure 3. MOSFETs M1, M2 and M7-M12 will carry 5 uA of drain current. MOSFETs M5/M6 must now carry 7.5 uA. This biasing scheme gives maximum swing at the drains of M8/M10. The currents in M5-M6 are 7.5uA. The CMFB circuit must adjust the gate drive of M5 and M6 so that they provide 7.5 uA of current in them.

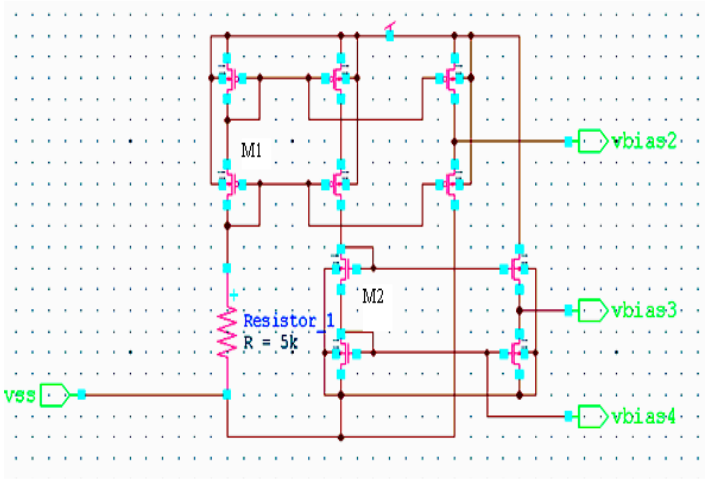

Figure 4. Biasing circuit for the folded cascode op-amp

2.3. CMFB circuit

The common mode feedback circuit is shown in figure 5.

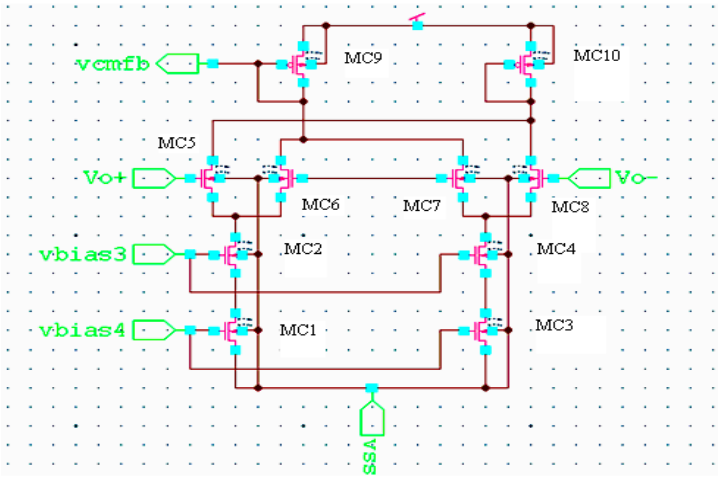

Figure 5. The CMFB circuit

Here, the output of folded cascode op-amp, v_{o+} and v_{o-} are the inputs to the CMFB circuit while the output is V_{cmfb}. This circuit rejects the difference mode signal at its input and amplifies the common mode signal. This is exactly opposite to that of a differential amplifier.

The expression for output is

$$Vcmfb = A[(v_{o+} + v_{o-}) / 2 – Vcm]$$

In the circuit, if v_{out+} and v_{out-} goes above Vcm, then drain currents of MC6 & MC7 starts to decrease. This makes Vcmfb to increase towards V_{dd}. This increase in Vcmfb will make the drain currents of M5/M6 of fig (3) to decrease. Since currents in M9 to M12 are constant, it results in a decrease of v_{o+} and v_{o-}. Similar arguments can be made if vo+ and vo- goes below Vcm.

Figure 6 shows a fully differential S/H implementation using an op-amp or an OTA. At $t = t_0$, the switches Φ1 and Φ2 are closed while Φ3 switches are open. During $t_1 \rightarrow t_2$ duration, the input voltage charges the capacitor C_H.

3. SAMPLE AND HOLD CIRCUIT

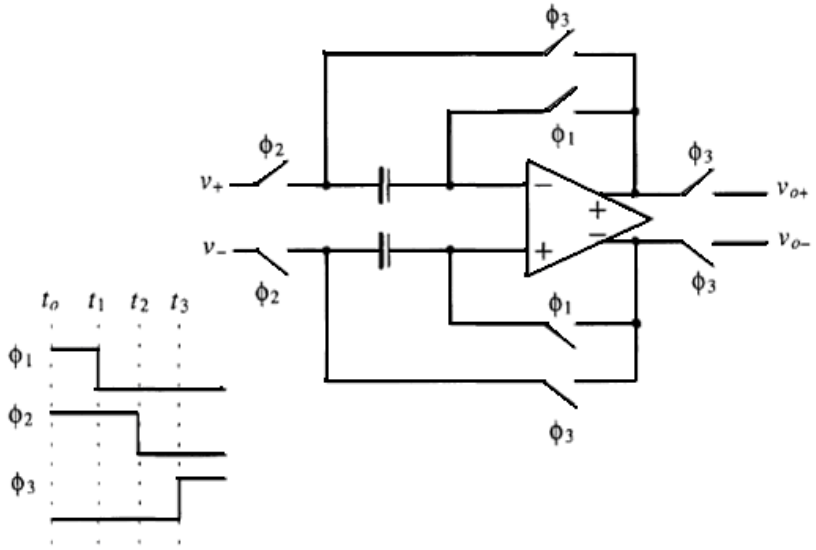

Figure 6. Fully differential sample and hold circuit

At t1, the switch Φ1 opens and for a very short duration $t_3 \rightarrow t_1$, the op-amp is in open loop [2] [5]. As the top plate of C_H is at gnd, the charge injection and capacitive feed through resulting from turning OFF of Φ3 switches becomes independent of input signal. When Φ2 switch turns OFF, the charge injection will flow into the low impedance vin and not into the right side of Φ2 as this impedance is large. This leaves the voltage across capacitor unaffected by the charge injection resulting from the turning OFF of the switches. This sequence of turning OFF of the switches is called bottom plate sampling. The fully differential Sample and Hold implementation is shown in fig. (7). We can determine the input/output relationship of sample and hold circuit by evaluating

the charge stored on Ci and Cf. Initially, assuming Vci+ and Vci- are combined and connected to a common voltage Vcm, we have

When Φ1 and Φ 2 switches are closed and Φ3 open then the charge on Ci and Cf

$$Q_{i,f} = C_{i,f} (v_{in} - v_{cm} \mp v_{offset})$$

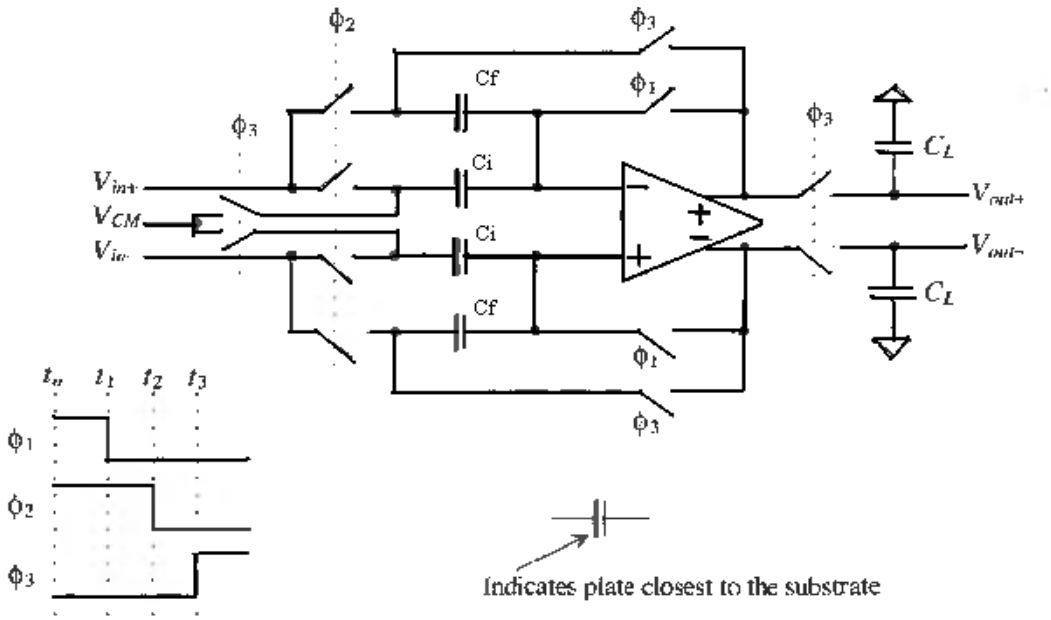

Figure 7. Fully differential S/H circuit implementation

When Φ 3 goes high, the charge on Ci is

$$Q_{in} = C_i (v_{cm} - v_{cm} +- v_{offset})$$

The difference between Qin (when Φ1 is ON) and Qin (when Φ3 is ON is transferred to Cf when Φ3 goes high. Since the charge must be conserved,

$$Cf (vout - vcm \pm v_{offset}) = C_f (v_{in} - v_{cm} \pm v_{offset}) + C_i (v_{in} - v_{cm} \pm v_{offset})$$

$$+ C_i (v_{cm} - v_{cm} \pm v_{offset})$$

OR when Φ3 is on,

$$Vout = [1+ Ci / Cf] vin - Ci / Cf \ vcm \ldots . \quad (3)$$

Notice that the op-amp offset is automatically zeroed out.
Eq. 3 can be used to find the relation of vin and vout for fully differential signals given by

$$Vout = (vout+ - vout-) = (1+ Ci / Cf) (vin+ - vin-)$$

Notice that the common mode voltage subtracts out.
If v_{cm} is replaced by Vci+ and Vci- as shown in figure 8, then

$$Vout+ = (1+ Ci / Cf)\ vin+ - Ci / Cf\ Vci+ \text{ and}$$

$$Vout = (vout+ - vout-) = (1+ Ci / Cf)\ (vin+ - vin-) \quad - Ci / Cf\ (Vci+ - Vci-)$$

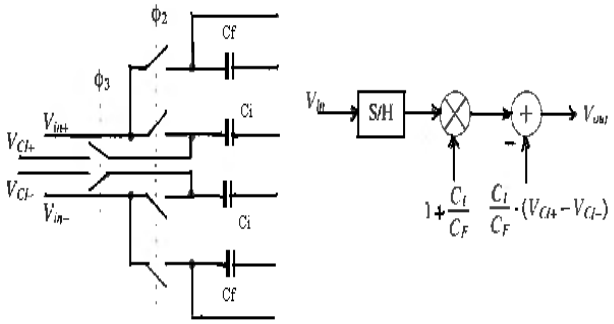

Figure 8. Implementing subtraction in S/H

4. 1.5 BITS / STAGE

Pipelined ADCs get their final resolution using a series of cascaded lower resolution stages [3][8][9]. For example, a 12 bit ADC can be a cascade of four 3-bit stages. Many designers are comfortable with 3-bit flash ADCs. However, 1.5 bits / stage is also becoming increasingly popular. For high speed converters there is an advantage of going for minimum stage resolution. It minimises the interstage gain required, which in turn maximises the bandwidth, since gain bandwidth product is a constant for a given technology.

A 1.5 bits/stage is a 1bit/stage into which some redundancy is added to provide for device tolerances and imperfections. A digital error correction later eliminates this redundancy. The 1.5bits/stage uses two analog comparison levels Vu & VL instead of a single level in a 1 bit/stage. Because of the introduction of gain of two, they must lie between –Vref/2 and +Vref/2. a common choice is Vu = +Vref/4 and VL = – Vref/4.
The voltage transfer characteristic is shown in fig. 9 (b) which is highly nonlinear.
The input voltage range is divided into three sections. The upper range (U) above Vu, mid range between Vu and V_L and low range (L) below V_L as shown in the table 1.

Table1.

Vin	Range	B1	B0	DAC o/p	Analog residue o/p
Vin > Vu	U	1	0	+ Vref	2Vin – Vref
V_L<Vin< Vu	M	0	1	0	2Vin
Vin < V_L	L	0	0	- Vref	2Vin + Vref

The implementation of 1.5bits/stage is shown in fig. 9 (a). A resistor string provides voltage division to create reference voltages. All other high accuracy operations such as multiply-by-two are achieved by capacitor ratios. The sample and hold circuit and multiply-by-two amplifier can be combined to form a multiplying DAC (MDAC). The cascaded MDAC outputs are passed through latches before fed to the redundancy bit removal circuit as shown in figure11.

4.1. Redundancy bit removal algorithm

The probable error sources in data converters include offset voltages in comparators and op-amps, gain error in amplifier, nonlinearity in converter and others. Many of these errors are corrected by this algorithm[8][9].

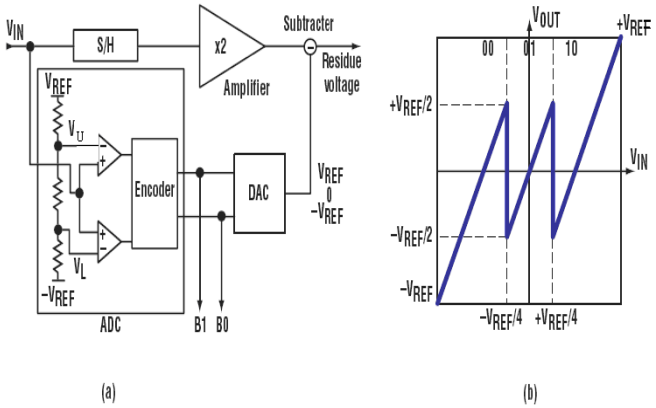

Figure 9. (a) A 1.5 bit pipelined ADC stage. (b)The stage voltage transfer characteristic.

Each 1.5bit pipelined stage produces a 2 bit code B1B0. Using redundancy bit removal algorithm, this is reduced to final 1 bit per stage code. For a resolution of 3 bits, the input voltage range of ±2V is divided into 8 equal slots and the input voltage, the code generation of each stage and corresponding stage residue voltages are shown in table 2. To generate the final code, the two bit codes generated by each stage are added in a systematic way. For example, as highlighted in table 2, for Vin = 1.33V, the codes generated by successive stages are 10, 10 and 00.

Table 2. Development of error corrected output code

INPUT RANGE (V)	DESIGN OUTPUT CODE	VIN (V)	RANGE 1	CODE 1	RES 1	RANGE 2	CODE 2	RES 2	RANGE 3	CODE 3	DERIVED OUTPUT CODE
2.00	111	1.70	H	10	1.40	H	10	0.80	H	10	111
1.50	110	1.33	H	10	0.66	H	10	-0.68	L	00	110
1.00	101	.79	H	10	-0.42	M	01	-0.84	L	00	101
0.50	100	.19	M	01	0.38	M	01	0.76	H	10	100
0.00	011	-0.35	M	01	-0.70	L	00	0.60	H	10	011
-0.50	010	-0.68	L	00	0.64	H	10	-0.72	L	00	010
-1.50	001	-1.21	L	00	-0.42	M	01	-0.84	L	00	001
-2.00	000	-1.82	L	00	-1.64	L	00	-1.28	L	00	000

These bits must be added as follows to generate the final 3 bit code.

```
    1  0
+       1  0
+          0  0
  ---------------
    1  1  0  0
  ---------------
```

Discard LSB and the final digital code is 110 for the case Vin = 1.33V. The circuit to implement this algorithm is shown in fig. (10).

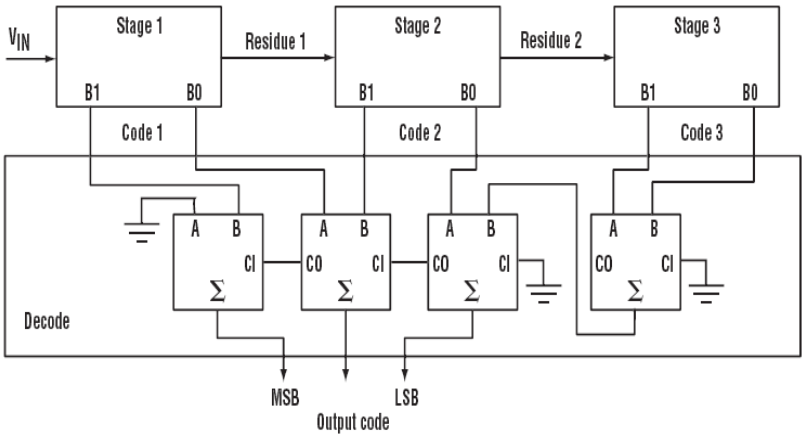

Figure10. Implementation of redundancy bit removal algorithm

5. RESULTS

The gain and phase margin curves are as shown in figure11 where the gain in 75dB and the unity gain frequency is 200MHz at a phase margin of 88^0. The differential outputs of 100Msps sample and hold circuit with a gain of two are shown in figure12.

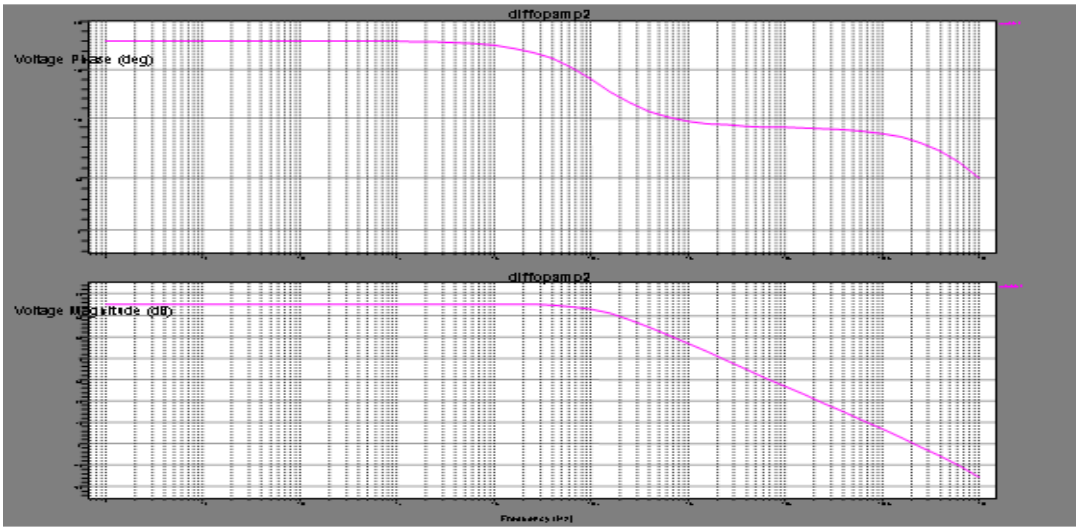

Figure 11. Gain and phase plots of folded cascode op-amp

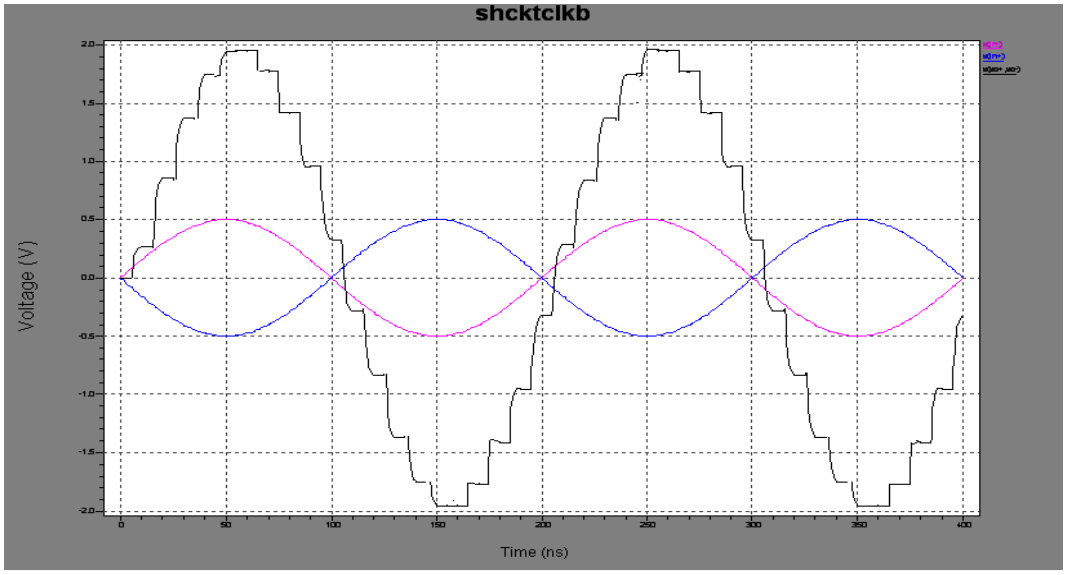

Figure 12. Sample and Hold outputs

The input signals are 0.5V differential and the output is seen to be 2V i.e. the differential input signals are sampled and given a gain of 2.The INL and DNL errors are observed to be less than ½ LSB as in figure13.

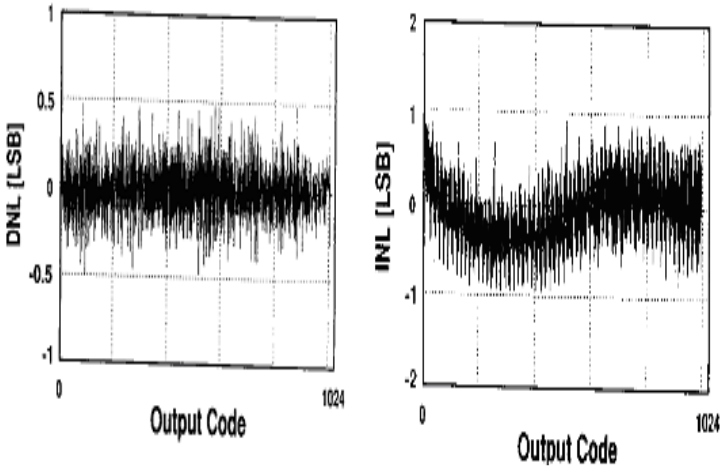

Figure13. INL and DNL error

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