RELEVANCE OF GROOVED NMOSFETS IN ULTRA DEEP SUBMICRON REGION IN LOW POWER APPLICATIONS

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ABSTRACT

To manage the increasing static leakage in low power applications, solutions for leakage reduction are sought at the device design and process technology levels. In this paper, 90nm, 70nm and 50 nm grooved-gate nMOS devices are simulated using Silvaco device simulator. By changing the corner angle and adjusting few structural parameters, static leakage reduction is achieved in grooved nMOSFETS in ultralow power applications. The simulation results show that leakage contributing currents like the subthreshold current, punchthrough current and tunneling leakage current are reduced. The oxide thickness can be increased without increase in the gate induced drain leakage current, and ON-OFF current ratio is improved and maintained constant even in the deep submicron region. This study can be helpful for low power applications as the static leakage is reduced drastically, as well as be applicable to high speed devices as the ON current is maintained at a constant value. The results are compared with those of corresponding conventional planar devices to bring out the achievements of this work.

KEYWORDS

Planar MOSFET, Grooved MOSFET, Concave corner, Corner angle, Deep Submicron regime, DIBL

1. INTRODUCTION

For the last four decades, silicon technology has been progressively reducing the channel length of MOSFETs from 25µm at 5-10V supply voltage to nanometric lengths and power supplies below 1V in current production technologies. As technology evolves and channel length becomes nanometric, total leakage current increases. The attributing factors are mainly: due to the lowering of threshold which increases the subthreshold current, the increased short channel effects which also increase the subthreshold current and reduction of oxide thickness which increases the gate tunneling current. Different physical phenomena contribute to the leakage currents causing the static consumption when one or more transistors in the V_{dd} to GND paths are in OFF-state. For submicron technologies below 0.5µm, the dominant mechanism is the subthreshold leakage current. For nanometric technologies below 100nm, the decrease in the gate oxide thickness needed to achieve a high current drive capability and to reduce the short channel effects causes the magnification of nonideal effects such as gate tunneling currents. For sub-50nm MOSFETS, the body to drain junction tunneling current has become one of the dominant

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mechanisms due to high doping concentration [1]. The device scaling concept leads to increase in both switching speed and number density of MOSFETs under reasonable power consumption. This had been the main guiding principle of the MOS device engineering over the past 30 years. The conventional device scaling has confronted the difficulty that the three main indexes associated with MOSFET performance: ON current, power consumption and short channel effects have the trade off relationship with each other owing to several physical and essential limitations related to device miniaturization in the sub 100nm regime (Fig.1).

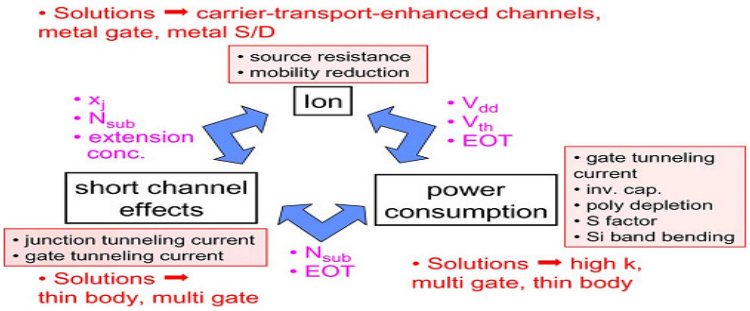

Figure.1.Tradeoff factors among ON current, power consumption/leakage current, and short channel effects under simple device scaling and possible solutions to mitigate the relationship [2].

Lower supply voltage (V_{dd}) and higher threshold voltage (V_{th}) lead to significant reduction in ON current (I_{on}). Thick gate oxides are needed for reducing the direct tunneling current and significant increase in leakage current (I_{OFF}) under ultrathin gate oxide regime decrease I_{on} and increase the subthreshold swing (S) because of lower gate capacitance (C_g). The increase in substrate impurity concentration (N_{sub}) necessary for suppressing short channel effects in bulk MOSFETS and obtaining smaller S causes the increase in I_{OFF} due to junction tunneling current and gate induced drain leakage current and the reduction in I_{ON} due to lower mobility and resulting lower velocity near the source region. In order to make both requirements of low power consumption and high performance compatible, the introduction of channels with high carrier velocity is suggested in [2] because these channels can provide not only higher I_{on} due to higher V_{th} but also reduce V_{dd} or increase T_{ox} under a constant value of I_{on} resulting in reduction of the active power or the standby power. This paper also suggests choosing III-V MOSFETs to be suitable for low power consumption while maintaining high performance. III-V MOSFETs with low gate and junction leakage currents can be realized by choosing relatively thick gate oxides. Aggressive scaling of device not only increase subthreshold leakage but also has other negative impacts such as increased drain induced barrier lowering, V_{th} roll off, reduced on current to off current ratio and source–drain resistance. To avoid the short channel effects, oxide thickness scaling and higher and non uniform doping needs to be incorporated as the devices are scaled to the nanometer regime, but low oxide thickness gives rise to high electric field resulting in considerable direct tunneling currents(gate leakage). Controlling the variation in device parameters is becoming a great challenge for scaled technologies. The delay and leakage current in a device depend on the transistor geometries gate length, oxide thickness width, the doping profile, the supply voltage. Any low leakage design needs to consider the spread of leakage and delay both at the circuit and device design phase to minimize overall leakage while maintaining yield with respect to a target delay under process variation [3]. The contribution of different leakage components in nMOS devices at different technology generation are shown in Fig 2. It can be observed that for the 90-nm device, the major leakage component is the subthreshold leakage, but in the scaled devices, contributions of the junction leakage and the gate leakage have significantly increased.

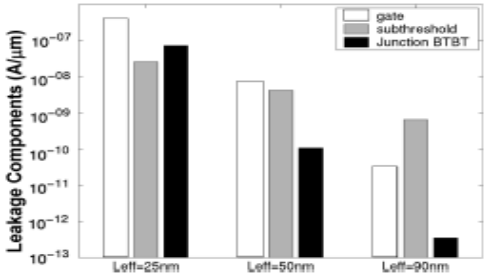

Figure. 2 Contribution of different leakage components in NMOS devices at different technology generation [3]

According to the National Technological Roadmap for Semiconductors (NTRS), an equivalent silicon dioxide thickness of less than 2.0nm will be required for sub-100nm generation MOS devices. Several physical limiting factors associated with the ultra thin gate oxides have been identified, including direct tunneling currents, quantum mechanical effect in the substrate, polysilicon depletion effects, and oxide reliability. Among them, the direct tunneling current is the most sensitive one to the oxide thickness. As the thickness of the oxide layer decreases, the tunneling current increases in an exponential manner. This increased current not only adversely affects the MOS device performance but also greatly increases the standby power consumption of a highly integrated chip. As the channel length of the MOSFET is scaled, concerns also arise regarding the tunneling currents associated with the source and drain extension (SDE) area to the gate overlap regions. For deep submicron devices, the SDE region can become a significant part of the channel. The drain leakage currents such as band-to-band tunneling and gate-induced drain leakage currents have always been a concern for MOSFET scaling. When combined with ultra thin oxides, these effects can become important when compared to the gate direct tunneling currents [4].

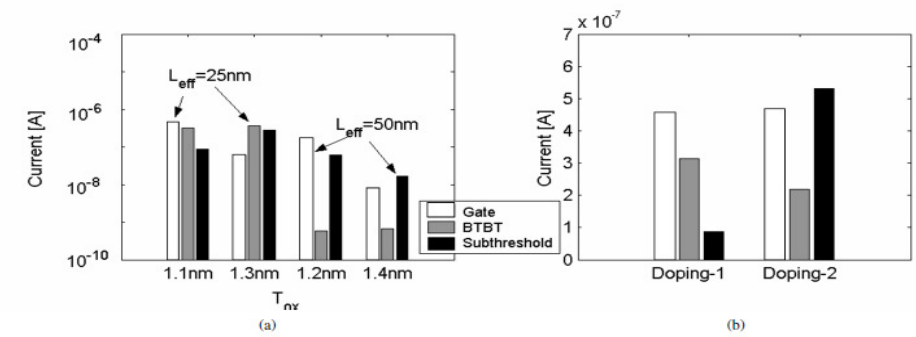

Figure.3 Variation of different leakage components with **(a)** technology generation and oxide thickness; and **(b)** doping profile [3]

In a nanoscale device, where short channel effects are extremely severe, an increase in the oxide thickness will increase the subthreshold leakage as in Fig 3(a). The subthreshold leakage and the junction BTBT are strongly coupled through the doping profile. Fig. 3(b) shows the different leakage components of a 25-nm device at different doping profile (oxide thickness and V_{dd} were kept constant). A strong "halo" doping reduces the subthreshold current but results in a high BTBT. Reduction of the halo-strength lowers the BTBT, but increases subthreshold current considerably Fig. 3(b). Magnitude of the leakage components and their relative dominance on each other depends strongly on device geometry and doping profile.[5] Changing the device structure in such a way that the MOSFET can be scaled further even with a relatively thicker oxide is suggested in [6]. By proper codesign it is possible to obtain hundreds of MHz of performance in subthreshold systems with very low power [7].

To achieve higher speed and packing density in VLSI, the size of MOSFET's has been continuously scaled down, and the short channel effects becomes the stringent limitation to the performance of deep-submicron devices and VLSI packing density. As the supply voltage and the gate oxide thickness are becoming close to the practical or inherent limits, various studies [8-12] propose concave MOSFET's to be the most promising devices for suppressing the short-channel effect and thereby subthreshold leakage currents in the deep-sub-micron and sub-0.1-micron regime, because structures with shallow junctions or even negative junctions can be fabricated without any increase in series resistance. The potential expansion from the drain to the channel area causes the short channel effects that reduce the controllability of device characteristics. A shallower junction is required to suppress the potential expansion. Elevated structures of source and drain or grooved gate MOSFETS are practical candidates in the 0.1µm regime from the viewpoint of suppressing the short channel effects because the source and drain junction in these devices can be located above the channel. The combination of extremely shallow junctions and heavy channel doping suppresses punchthrough and suppresses threshold voltage roll off. This is because DIBL and charge sharing are significantly suppressed by the extremely shallow junction. As long as the source and drain junctions are extremely shallow, the concentration can be made as high as possible for realizing high performance[13]. Therefore concave MOSFET's with changing corner angle and applying negative junction depths are good candidates in sub-0.1-micron regime. It was found that the grooved gate device exhibits high immunity to short channel effects such as hot carrier effects due to impact ionisation and drain induced barrier lowering while at the same time maintaining the major electrical performance parameters of the planar device. It is an effective way to change the concave corner angle in deep-sub-micron region to control threshold voltage roll off and thereby control subthreshold leakage currents. Considering the above advantages of grooved devices, an exhaustive study is required in the area of ultra low power applications in submicron and the deep submicron region. This work proposes that by changing the corner angle and adjusting structural parameters like junction depth, channel doping concentration, negative junction depth, and oxide thickness, leakage current in 90nm, 70 nm and 50 nm nMOS can be minimized. In this paper, the influence of the grooved gate nMOSFET's geometric structure on the subthreshold leakage is investigated.. The examined structural parameters include the negative junction depth, the concave corner and the effective channel length. Section II describes the devices structure and the simulation tools used for the work. Section III discusses the simulation results obtained in terms of controlling of V_{th} roll off and reductions in DIBL, reduced leakage power due to the reduction in off state leakage and punchthrough current, minimizing gate induced drain leakage and ON current to OFF current characteristics are explained in the results. Section IV concludes the paper.

2. DEVICE STRUCTURE

The grooved gate device structure is described by the schematic cross section in Fig 4.

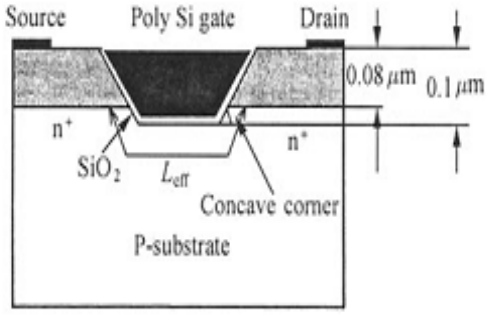

Figure.4. Schematic cross section of grooved gate nMOSFET[11]

Concave MOS Structure

The cross-sectional view of an ideal concave nMOSFET is shown in Fig. 4. The source and drain junction depth is shallower than the channel region. The corner of the grooved gate at the drain limits the extension of the drain potential, because of which the V_{th} lowering is not observed. The potential barriers at the corners become sharper and higher for small corner radii and higher substrate doping, and less current surmounts the barrier [11]. The threshold voltage is controlled by the concave corner angle, junction depths, channel doping and threshold voltage roll off is eliminated by optimizing these structural parameters

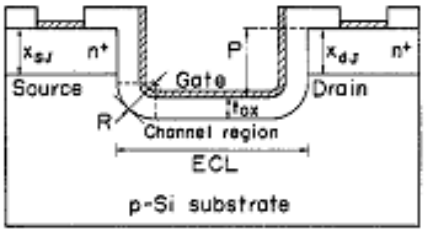

Figure. 5. Cross sectional structure of the n-MOSFET along with the characteristic parameters [8]

A device with a radius of zero or a sharp corner has a very large corner effect due to the difficulty the electric field experiences in reaching into the corner . Further there is a rapid increase in the available depletion charge as the depletion width increases. Thus the corner radius and the angle are the additional parameters having significant influence on the grooved gate device to characterize the sub threshold behavior. Also [12] suggests that the sharp corner occurring at a lower corner radius provides sufficient condition to decrease the DIBL effect dramatically. In Fig. 5 the cross sectional structure of the n-channel MOSFET along with the characteristic parameters are shown[8].

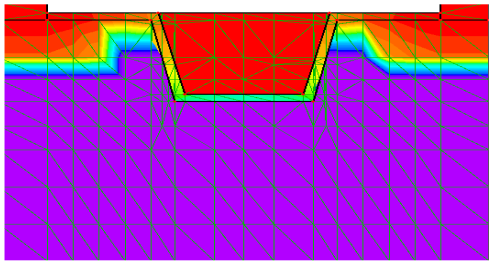

Figure.6. Simulated structure of 70nm grooved nMOSFET

A 90nm, 70nm and a 50nm grooved gate nMOSFETs are designed and simulated for analyzing the electrical characteristics using two dimensional device simulator, DEVEDIT and process simulator, DECKBUILD. A conventional short channel planar device is also simulated to obtain a reference for comparison of major electrical parameters.

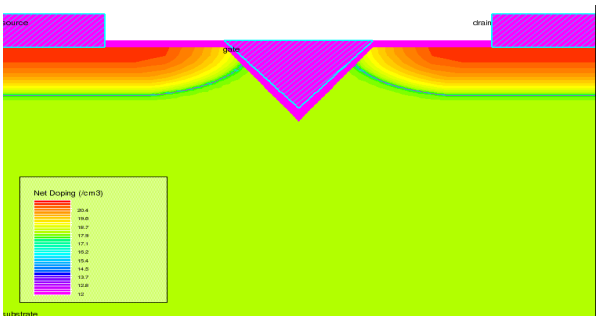

Figure.7 Simulated structure of 50nm grooved nMOSFET

The simulated structures of 70nm and 50nm grooved nMOSFET is shown in Fig. 6 and 7. In the simulated grooved gate nMOSFET, the source/drain junction depths are 0.03µm above the bottom of the groove (form 0.025µm negative junction). The bottom concave corner angles are 90°, and 75°and single sharp corner angle 57° respectively. The substrate concentration is kept at 1e18 for both the planar as well as the grooved devices. Optimizing the oxide thickness for low power consumption being of serious concern, the gate oxide thickness is kept at 3 nm for the grooved devices as well as the planar devices. The grooved devices successfully limit the tunneling through the oxide as against the planar ones.

3 RESULTS AND DISCUSSION

3.1 Controlling V_{th} roll-off and DIBL:

Scaling into deep and ultra deep sub micron regions increases the short channel effects and thus leakage current increases due to various sources. In the simulated structure of gate length of 90nm ,70nm and 50nm, this work shows the V_{th} roll off in the ultra deep region(Fig.8).

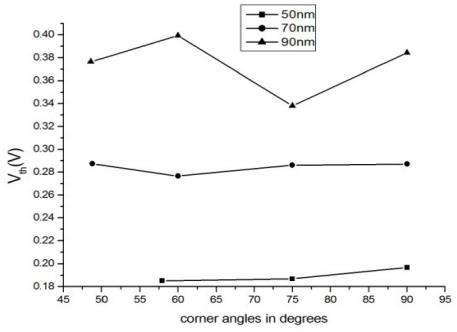

Fig. 8. Variation of V_{th} in 90, 70 and 50nm grooved nMOSFETs

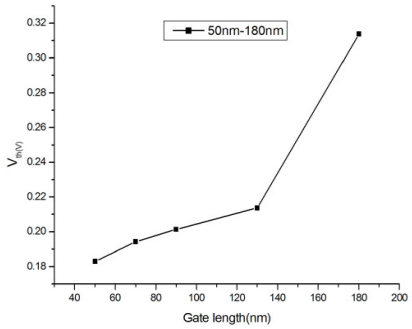

Fig. 9 Planar nMOSFETs threshold voltage as function of gate lengths

Comparing this to the planar nMOSFET, V_{th} roll off is observed from180nm gate lengths down till 50nm(Fig.9) The presence of the threshold voltage roll off in the planar nMOSFET is due to the source and drain depletion widths. High drain bias results in more depletion charge in the channel from the drain and source leading to larger subthreshold current[14]. With the increase in drain bias voltage, the surface potential distribution is affected directly by the drain voltage using depleted area, the potential in the channel is distorted intensely. The effect of drain voltage on the electric field in channel is very severe and the drain area potential extends to the source region and the only one potential barrier disappears in planar nMOSFETs.

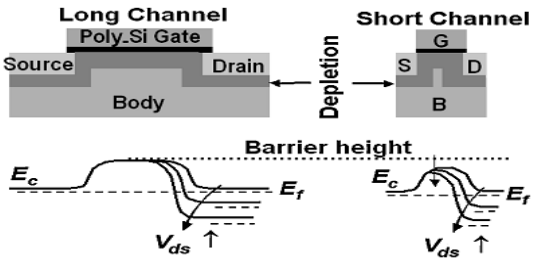

Figure. 10. Barrier height lowering due to channel length reduction and drain voltage increase in a MOSFET[15]

Drain-Induced Barrier Lowering (DIBL) effect for a short channel transistor in short channel transistors, in case of deep sub-micron and nanometer technologies, the depletion regions of the source and drain junctions causes some parts of the channel to be already depleted under the gate which, in turn, lowers the value of the threshold voltage needed for conduction to occur as in Fig 10. As a result of DIBL, threshold voltage is reduced with shorter channel lengths as shown in fig.11 and, consequently, the subthreshold leakage current is increased[16].

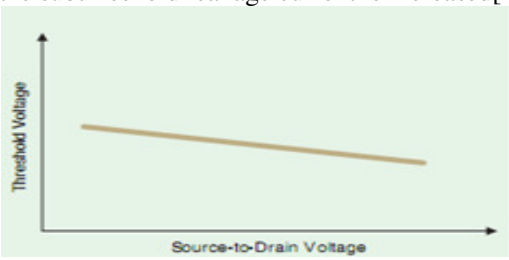

Figure 11. DIBL vs V_{th} [16]

On the contrary, in the grooved nMOSFET simulated in this paper, the grooved structure nearly keeps the same threshold voltage for the simulated channel lengths for 90nm, 70nm and 50nm at 3nm, 4nm, and 5nm gate oxide thickness. The threshold voltage even increases as the channel length is reduced[17]. This is due to the coupling of the potential barriers created at both corners of the gate which slightly increases the total barrier between the source and the drain as the U grooved channel converts into a V grooved channel. The potential barrier near the drain decreases a little, but these two barriers diminish the effect of drain electric field on the channel and the drain induced barrier lowering effect (DIBL) is suppressed [18]. The effect of drain voltage is almost shielded by these two barriers formed at each concave corner and thus the short channel effects are controlled. Here, the potential barrier being slightly affected in the drain region, the corner effect acts against the DIBL effect. The potential barriers at the corners become sharper and higher for smaller corner radii and higher substrate doping, allowing less current to surmount the barrier. The height of the barriers for the grooved gate increases as the channel length is shortened until the two barriers fuse into one and an additional increase in the threshold voltage occurs.

3.2 Reducing leakage currents: [OFF state, GIDL, Punchthrough]

In order to realize low power MOSFETs lower supply voltage (V_{dd}), higher threshold voltage (V_{th}), smaller subthreshold slope (S) and lower off state current (I_{off}) are necessary. Gate direct tunneling currents are produced by the quantum mechanical wavefunction of a charged carrier through the gate oxide potential barrier into the gate, which depends not only on the device structure but also the bias conditions(Fig.12).

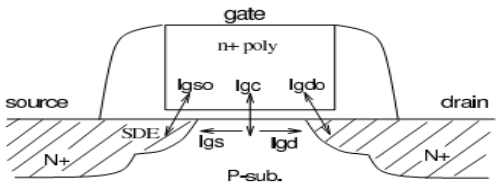

Figure. 12. Gate tunneling components of a very short channel nmosfet , Igso, Igdo are edge direct tunneling currents[20].

Gate Induced Drain Leakage (GIDL) is due to the high electric field effect in the drain junction. GIDL at the NMOS gate-drain edge is important at low current levels and high applied voltages. For a MOS device with 0 V gate voltage and drain potential V_{DD}, significant band bending in the drain allows electron-hole pair generation. A deep depletion condition is created since the holes are rapidly swept out. This leakage mechanism is exacerbated by high source or drain to body voltages as well as high drain to gate voltages[19]. GIDL effect can be minimized by carefully controlling the doping profile in the drain of an MOS transistor. Punchthrough occurs in short channel devices because of the very small distance that separates the MOS source from the drain and because of the increase in the reverse-bias voltage of the source/substrate and drain/substrate junctions. The punchthrough can be controlled by using implants at the bottom or the edges of the source and drain junction boundaries. Fig. 13 shows Gate Induced Drain Leakage and Punchthrough currents in nMOSFET[15].

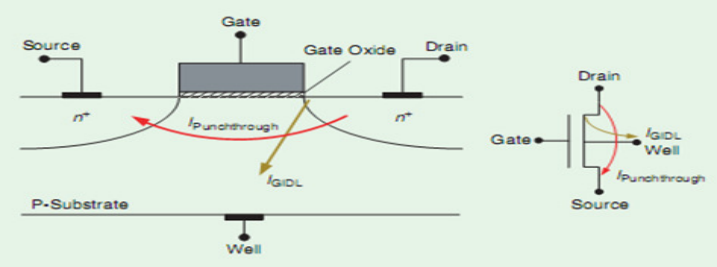

Figure.13 Gate Induced Drain Leakage and Punchthrough currents in nMOSFET [15]

The corner of the grooved gate at the drain limits the extension of the drain potential, controlling the punchthrough current. The drain separation from the implanted channel region as well as the curved structure at the drain is effective to reduce the electric field at the drain improving reliability. This also decreases the substrate current and increases the highest applicable gate to drain voltage improving the reliability of the device[12]. Punchthrough current also occupies an important part of the total leakage power due to any device. As the corner of the grooved gate at the drain limits the extension of the drain potential, the punchthrough current is controlled. Limiting the punchthrough current also controls the subthreshold current. The subthreshold leakage is the drain source current of a transistor during operation in weak inversion. For smaller channels, the threshold voltage tends to decrease, increasing subthreshold current. The physical origin of lowering of V_{th} is due to the extension of the depletion region of the channel into the isolating field oxide[4]. In the grooved gate nMOSFETs, the inverted gate along with the oxide around it prevents the above said extension of the depletion region of the channel.

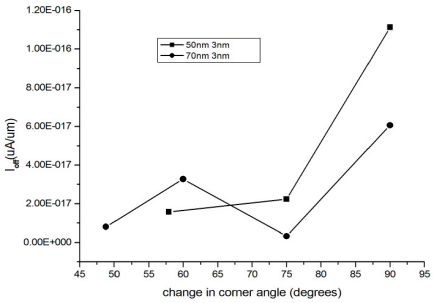

Fig. 14 Leakage current reduction due to change in corner angles in 50-70nm grooved nMOSFETs

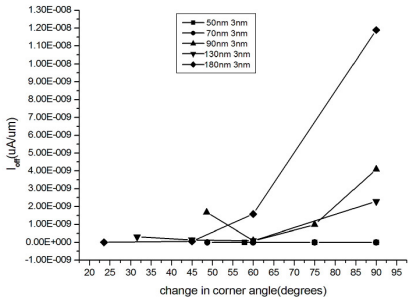

Fig. 15 Leakage current reduction due to change in corner angles in 50-180 nm grooved nMOSFETs

Analyzing the off state current of 90, 70 and 50nm grooved nMOSFET, we find substantial decrease in the leakage current(Fig.14,15) when the corner angle is changed from 90 degrees to the sharp single corner. At the process level, leakage reduction can be achieved by controlling the dimensions like gate length, oxide thickness, junction depths etc., and doping profile of planar nMOS transistors. Grooved gate nMOSFETS has a number structural parameters like junction depth, channel doping concentration, negative junction depth, oxide thickness which can be adjusted to give optimum results. The gate oxide tunneling current is minimized by increasing the oxide thickness to 3nm in the deep submicron region. As the gate oxide thickness is increased, it results in decrease in the field across the oxide. The low electric field coupled with high oxide thickness results in reduced tunneling of electrons from the substrate to the gate and also from the gate to the substrate through the gate oxide resulting in reduction of the GIDL.

Simulating the 50nm device structure, one finds interesting result while changing the oxide thickness from 3nm to 5nm. This structure reduces oxide tunneling while minimizing the leakage current. Similar result is observed in 70nm and 90 nm region too (Fig.16, 17, 18). Changing the oxide thickness to 4nm and 5nm from 3nm, one finds favourable characteristics at 3nm and 4nm. The rise in the leakage current at 60° corner angle of 70nm grooved nMOSFET can be attributed to the roll off of V_{th} at the same corner angle.(Fig.18). According to the application, one can adjust the oxide thickness and the corner angle at which the device should be operated.

3.3 ON Current-OFF Current Characteristics:

The simulation results of I_{on} vs I_{off} of 90nm, 70nm and 50nm planar and grooved nMOSFETs are compared and tabulated in Table 1 and Table 2. Table 1, shows the ON-OFF curent values with changing corner angles, whereas Table 2 shows the ON-OFF curent values with varying thickness for planar nMOSFET. The grooved values are for 3nm oxide thickness. Due to the curved channel the saturation drain curent of the grooved gate MOSFET is less than the conventional MOSFET especially for single corner angles.

For the 90nm device, as depicted in Table 1, ON current has a near steady value though less than its planar counterpart. This is the main drawback of the corner effect for high speed applications as stated in [13]. In grooved nMOS the maximum saturation curent is reduced as the corner angles are changed. The OFF state values show that the corner angle doesn't have much effect on the leakage current(Fig.17). This result can be traded off by the I_{on}/I_{off} value which suggests a reduced but steady trend observed in this region.

For the 70nm device, as seen in Table 1, ON current has a decreasing trend w.r.t. the corner angles. The corresponding planar value in Table 2 shows a much higher value. The OFF current characteristics are discussed in section 3.2., (Fig.18). A very interesting result observed in 70nm region is its near steady I_{ON}/I_{OFF} behaviour. While scaling down from 90nm to 70nm, the average ON-OFF current ratio maintains a steady value instead of reducing like the planar one. This behaviour along with the enhanced OFF state characteristics in this region can be used for low power and high performance applications.

For the 50nm device simulation values, the OFF state characteristics show more promise than the ON current characteristics(Fig.16). Reduced ON-OFF current ratio is observed in this region, much similar to the planar one. These results are shown in Fig.19.

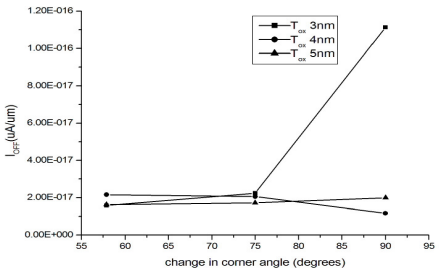

Fig. 16 Off state characteristics in 50nm L_g for grooved nMOS

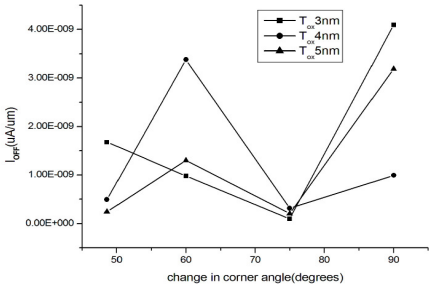

Fig.17 Off state characteristics in 90nm L_g for grooved nMOS

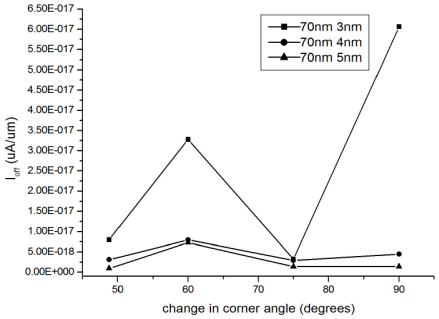

Fig. 18 Off state characteristics in 70nm for grooved nMOS

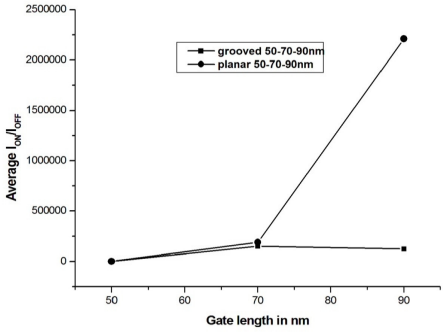

Fig. 19 ON-OFF ratios varies L_g with gate length 90nm-50nm

It is observed from Table 1, the current drive has improved immensely in the 70nm region at its single corner angle, and drastically reduced leakage current at its single corner angle makes the 70nm grooved nMOSFET ideal for low power as well as high performance applications. The 50nm grooved nMOSFET is ideal for low power applications as the OFF state characteristics show a highly positive result. The average values of Ion /Ioff for the 90nm, 70nm and 50nm grooved nMOSFET are very encouraging as against the planar ones, see Table1and 2. For the grooved nMOSFETs, the average ON/OFF for 50nm is 2.01E+03; for 70nm is 1.51E+05 and for 90nm is 1.24E+05. For the planar nMOSFETs, the average ON/OFF for 50nm is 3.59E+03; for 70nm is 1.22E+05 and for 90nm is 1.67E+06.

Table 1: ON-OFF current ratios comparison of Grooved 50nm, 70nm and 90nm nMOSFETs

Corner angles	50nm ON	50nm OFF	50nm ON/OFF	70nm ON	70nm OFF	70nm ON/OFF	90nm ON	90nm OFF	90nm ON/OFF
90	1.20E-13	1.11E-16	1.08E+03	1.02E-11	6.06E-17	1.68E+05	8.70E-05	4.09E-09	2.13E+04
75	6.64E-14	2.24E-17	2.96E+03	4.43E-13	3.26E-18	1.36E+05	3.80E-05	9.49E-11	4.01E+05
60	3.15E-14	1.57E-17	2.00E+03	1.42E-12	3.28E-17	4.34E+04	4.02E-05	9.80E-10	4.10E+04
48.6	--	--	--	2.06E-12	8.01E-18	2.57E+05	5.31E-05	1.68E-09	3.17E+04

Table 2: ON-OFF current ratios comparison of Planar 50nm, 70nm and 90nm nMOSFETs

Oxide thickness	50nm ON	50nm OFF	50nm ON/OFF	70nm ON	70nm OFF	70nm ON/OFF	90nm ON	90nm OFF	90nm ON/OFF
3nm	1.05E-11	8.17E-15	1.28E+03	2.20E-08	1.17E-13	1.88E+05	1.67E-04	7.58E-11	2.21E+06
4nm	6.51E-12	8.06E-16	8.08E+03	6.54E-10	4.43E-15	1.48E+05	1.41E-04	7.93E-11	1.78E+06
5nm	6.88E-13	4.89E-16	1.40E+03	3.65E-11	1.24E-15	2.95E+04	1.16E-04	1.14E-10	1.01E+06

4 Conclusion

With the continuous scaling of CMOS devices, leakage current is a major contributor to the total power consumption. In current ultra deep submicron devices with low threshold voltages, subthreshold leakage has become the dominant source of leakage along with the oxide induced leakage and punchthrough leakage. This work proposed changing the corner angles suitably in grooved gate nMOSFETs to minimize off state leakage, enhance ON-OFF current ratio, optimizing oxide thickness and moving onto single corner grooves to reduce the DIBL effect. Because of the emergence of the corner effect, the threshold voltage roll-off with the shortness of channel length is removed completely for grooved gate nMOSFETs even in ultra deep submicron region. The lowest values of off state leakage obtained for 70nm gate length is 1.00813×10^{-17} for 3nm thickness of gate oxide whereas it is 1.57442×10^{-17} for the 50nm gate length for the same thickness for their single corner angles of 48.8° and 57.9° respectively. The contributing leakage currents namely subthreshold leakage current, tunnelling leakage current and punchthrough current which add up to the total leakage power of a device are effectively minimized. The study proves corner potential barriers play an important role in threshold voltage enhancement and short channel immunity in grooved gate nMOSFETS. Further it is established that leakage current can be minimized effectively by changing corner angles in grooved gate nMOSFETS. Tradeoffs between reduced off state current and enhanced Ion//Ioff ratio can be made for low power and high performance applications. The 90nm region doesn't show much improvement in its ON-OFF state current characteristics, whereas the 70nm device suits aptly for low power and high performance applications by changing the corner angle especially to the single corner grooves. The 50nm device behaves extremely well as far as the leakage currents are concerned and thus should be used for low power applications.

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