

POWER COMPARISON OF CMOS AND ADIABATIC FULL ADDER CIRCUITS

Y. Sunil Gavaskar Reddy¹ and V.V.G.S.Rajendra Prasad²

¹Department of Electronics &Communication Engineering, Anurag Engineering College,
JNTUniversity, Andhrapradesh,India
sunil_hanu123@gmail.com

²Department of Electronics &Communication Engineering, Anurag Engineering College,
JNTUniversity, Andhrapradesh,India
veguntav@gmail.com

ABSTRACT

Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper conventional complementary metal oxide semiconductor (CMOS) and adiabatic adder circuits are analyzed in terms of power and transistor count using 0.18UM technology.

KEYWORDS

Low-power, adiabatic logic, Full adder, CMOS, Pass transistor logic, Positive feed back adiabatic logic, Transmission gate logic, SERF adder

1. INTRODUCTION

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

The low-power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit. One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching [1][2][14][18], has been proposed in the last years. In such approach, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

In literature, various kinds of adiabatic circuits proposed [1][12][18][20] all of them can be grouped into two fundamental classes: fully adiabatic circuits and quasi-adiabatic or partial energy recovery circuits[1].In the first class, in particular working conditions can consume asymptotically zero energy for operation, the large area occupation and the design complexity

make these circuits not competitive with traditional CMOS where as in second class circuits designed to recover large portion of the energy stored in the circuit node capacitances. This energy loss drawback however allows a good trade-off between circuit complexity and then area occupation.

Microprocessors and digital signal processors rely on the efficient implementation of generic arithmetic units to execute complicated algorithms like filtering, FFT. In these applications, multipliers are an important dissipation source. The basic element in multiplier is adder circuit so Therefore, power-efficient multipliers require power efficient implementation of adder circuit. In the literature different works presented on comparison of conventional CMOS adder circuits [3][5][15][16][17] and also comparison of adiabatic families[11][19][20][21]. In this work we analyzed the performance of conventional and adiabatic adder circuit's in-terms of power and transistor count.

The rest of the paper is organized as follows. Section 2 gives details of conventional charging and adiabatic charging principle, Section 3 explains different full adder implementations, section 4 simulation results and finally section 5 is conclusion.

2. ADIABATIC PRINCIPLE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail.

2.1. Conventional Switching

There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance [2]. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1. The expression for total power dissipation is given by

$$P_{tot} = \alpha \cdot C_L \cdot V \cdot V_{DD} \cdot f_{clk} + I_{SC} \cdot V_{DD} + I_{le} \cdot V_{DD} \quad (1)$$

Equation (1), the first term represents the dynamic power, where C_L is the loading capacitance, f_{clk} is the clock frequency, and α is the switching activity. In most cases, the voltage swing V is the same as the supply voltage V_{dd} ; however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct-path short circuit current I_{sc} which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{le} which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations. [2][4]

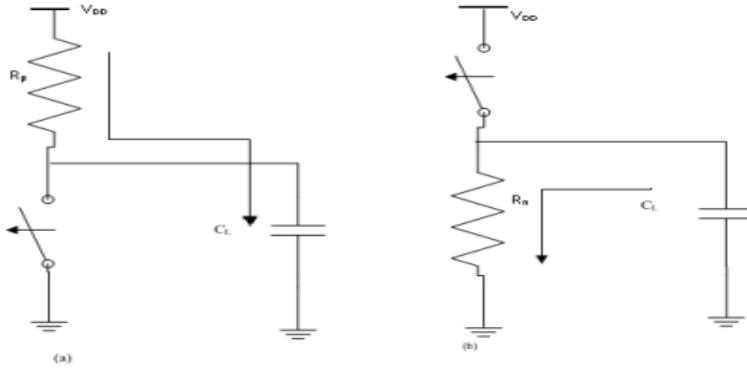


Figure 1Conventional CMOS a) Charging b) Discharging

2.2. Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source [1][4][9], as shown in Fig. 2. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. Assuming that the capacitance voltage V_C is zero initially, the variation of the voltage as a function of time can be found as

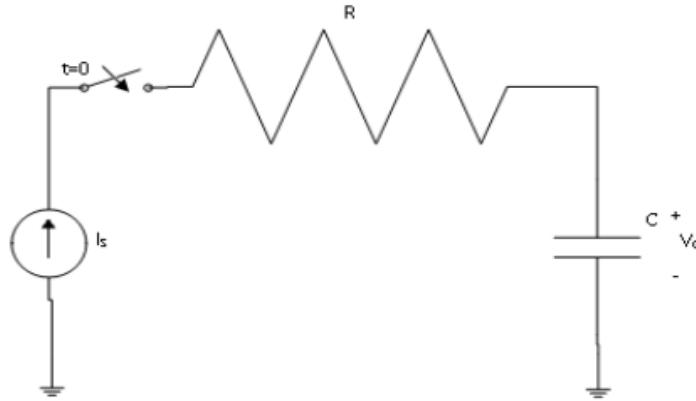


Figure 2 Schematic for adiabatic charging process

$$V_C(t) = I_S \cdot t / C \quad (2)$$

Hence the charging current can be expressed as a function of V_C and time t

$$I_S = C \cdot V_C(t) / t \quad (3)$$

The amount of energy dissipated in the resistor R from $t = 0$ to $t = T$ can be found as

$$E_{diss} = R \int_0^T I_S^2 dt = R I_S^2 T \quad (4)$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = \frac{RC}{T} \cdot CV_C^2(T) \quad (5)$$

From (5) we can say that the dissipated energy is smaller than for the conventional case if the charging time $T \gg 2RC$ and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. The additional hardware overhead associated with these specific power supply circuits is one of the design trade-off. Practical supplies can be constructed by using resonant inductor circuits. But the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc. [4]

An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on the average voltage drop across the resistor by using smaller voltage steps the dissipation can be reduced considerably [4]. The total dissipation using step wise charging is given by (6)

$$E_{tdiss} = \frac{1}{n} CV_{DD}^2 / 2 \quad (6)$$

Where n is number of steps used to charge up capacitance to V_{DD} .

In literature, adiabatic logic circuits classified into two types: full adiabatic and quasi or partial adiabatic circuits. Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. Quasi-adiabatic circuits have simple architecture and power clock system. There are two types of energy loss in quasi-adiabatic circuits, adiabatic loss and nonadiabatic loss. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock. If any voltage difference between the two terminals of a switch exists when it is turned on, non-adiabatic loss occurs. The non-adiabatic loss, which is independent of the frequency of the power-clock, is proportional to the node capacitance and the square of the voltage difference. Several quasi-adiabatic logic architectures have been reported, such as ECRL, 2N-2N-2P, PFAL etc.[1][9][12][13][14]

3. ADDER IMPLEMENTATION

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as

$$\overline{\overline{Sum}} = \overline{ABC} + \overline{AB}\overline{C} + \overline{A}\overline{BC} + ABC \quad (7a)$$

$$\overline{Carry} = AB + BC + CA \quad (7b)$$

3.1 Conventional adder [2], [4], [6]

Conventional CMOS Implementation consists of two functional blocks pull-up and pull-down. Pull-up functional block is implemented with P-channel MOS transistors and pull-down

functional block is implemented with N-channel MOS transistors. In order to get symmetrical structure (7a) is rearranged as (8) and sum and carry implementation is shown in Fig.3.

$$Sum = ABC + (A + B + C)\overline{Carry}$$

(8)

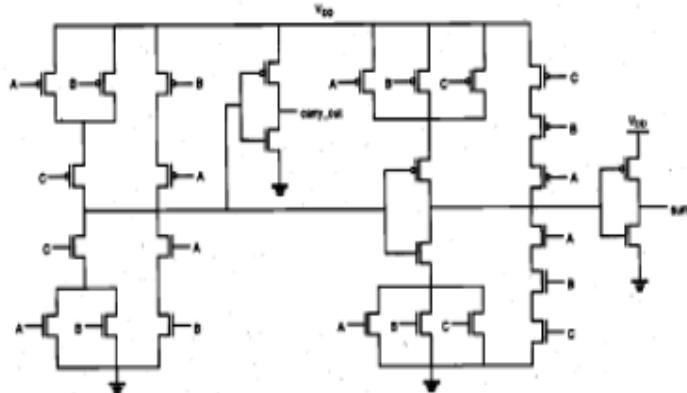


Figure 3 Conventional Symmetrical CMOS Full Adder

3.2 Pass transistor logic (PL) based adder [6]

Pass transistor logic is one of the well known nMOS logic style used to implement different functions. General method for deriving pass transistor logic diagram for a function is choosing control variable and pass variable based on the functional description. The main concept behind Complementary PL (CPL) is the use of only an nMOSFET network for the implementation of logic functions. This results in low input capacitance and high speed operation. The schematic diagram of the CPL full adder circuit is shown in Fig 4. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level.

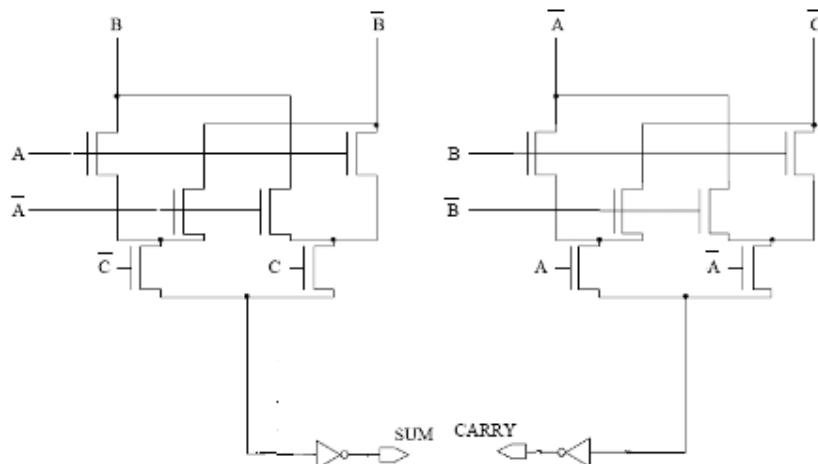


Figure 4 Pass transistor based full adder

3.3 Transmission gate (TG) based adder [4]

Transmission gate approach is another widely used CMOS design style to implement digital function. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses nMOS and pMOS transistors where as pass transistor logic uses only one type of transistor i.e. either nMOS or pMOS. Full adder implementation based on TG logic is shown in Fig.5. [4]

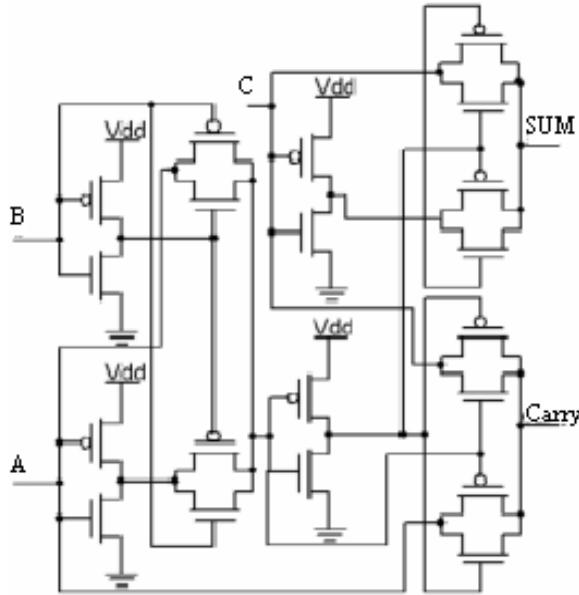


Figure 5 Transmission gate based full adder

3.4 10T adder or Static Energy Recovery Full adder (SERF)[8][15][19]

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signals. The capacitance at the outputs of XOR and XNOR gates is also reduced as they are not loaded with inverter. If the signal degradation at the SUM and Carry is significant for deep sub-micron circuits, drivers can be used to reduce the degradation. The driver will help in generating outputs with equal rise and fall times. This results in better performance regarding speed, low power dissipation and driving capabilities. The output voltage swing will be equal to the V_{DD} , if a driver is used at the output. The circuit diagram of static energy recovery adder is shown in fig 6

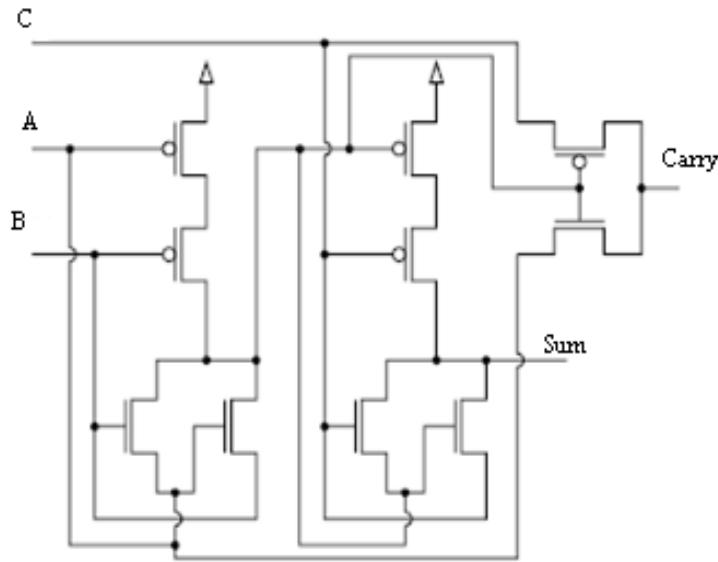


Figure 6: Static energy recovery adder

3.4 Pass transistor based adiabatic adder [7]

The sum and carry expressions for one bit full adder is given by

$$Sum = A \oplus B \oplus C$$

$$Carry = AB + BC + CA$$

(9)

The above equations can be re arranged as

$$Sum = (A \oplus B)\bar{C} + (\bar{A} \oplus B)C$$

$$Carry = (A \oplus B)C + (\bar{A} \oplus B)\bar{B}$$

(10)

The sum and carry expressions in (10) have common terms and can be implemented using Fig.7. [7]

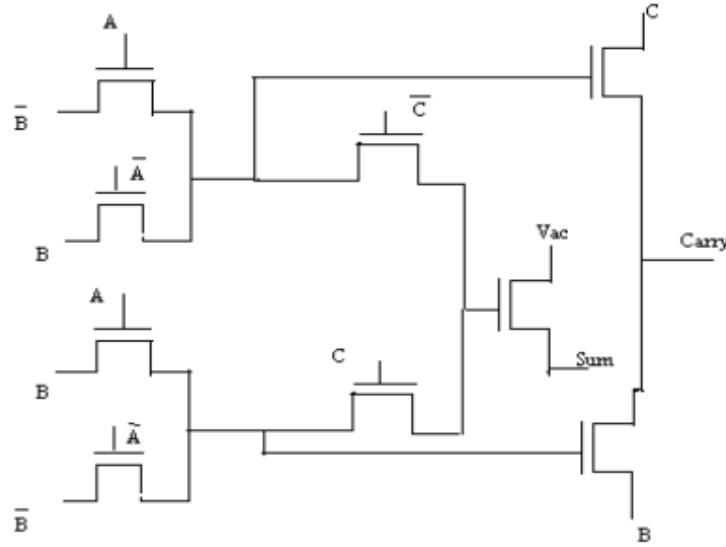


Figure 7Pass transistor based adiabatic full adder

3.5 Positive feedback adiabatic logic (PFAL) adder [12][18][21]

The general PFAL gate consists of a two cross coupled inverters and two functional blocks F and /F (complement of F) driven by normal and complemented inputs which realizes both normal and complemented outputs. Both the functional blocks implemented with n channel MOS transistors. The equations used to implement PFAL adder given by (11) and the corresponding sum and carry implementations are shown in Fig.8a and Fig.8b

$$\text{Sum} = \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC}$$

$$\text{Carry} = AB + BC + CA$$

(11)

3.6 Transmission gate based adiabatic adder (TGAL)

The general block diagram of transmission gate based adiabatic logic consists of two functional blocks F and complement of F operated with single clock power supply. Both normal and complemented inputs are available to functional blocks. Functional blocks are implemented using transmission gate or pass gate. The sum and carry implementation using transmission gate logic is shown in Fig .9a and Fig.9b. [4][11]

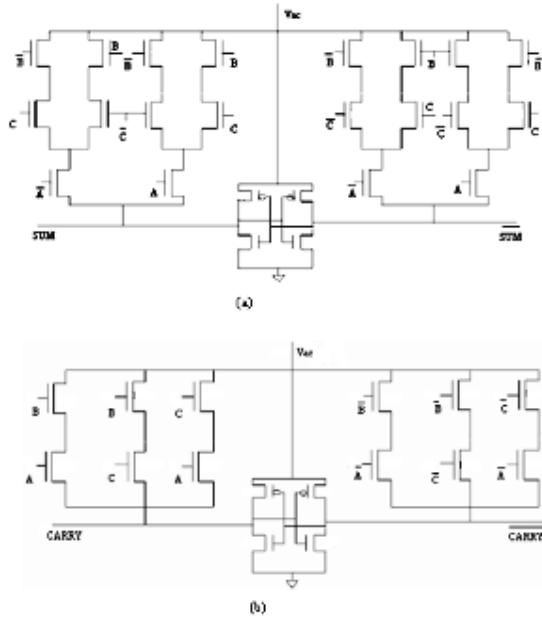


Figure 8 Positive feedback adiabatic full adder a) Sum b) carry

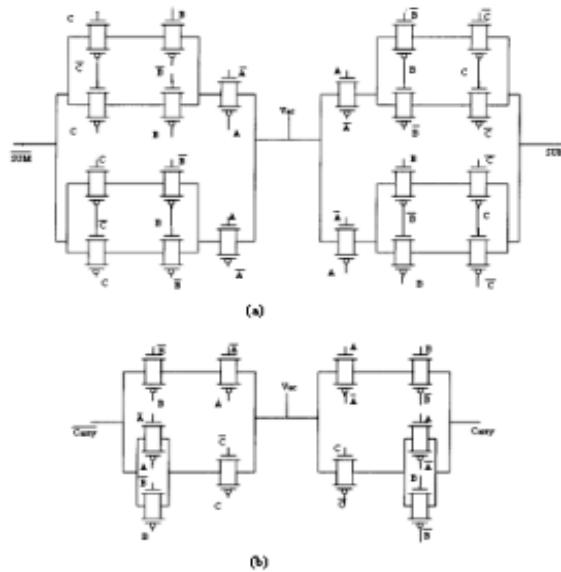


Figure 9 Transmission gate based adiabatic full adder a) Sum b) Carry

4 SIMULATION RESULTS

In order to estimate the power dissipation of the different circuits present in previous section we used power meter simulation model present in [4] and RC model present in [10].The schematic diagram of the test setup to estimate the power dissipation is shown in fig.10 and it contains DUT (design under test), linear current controlled current source, resistor, capacitor connected in parallel. All the circuits are designed and simulated using Tanner tools(S-edit, TSPICE) with 0.18um technology parameters.Fig.11 shows the simulation results of comparison of transmission

gate adiabatic logic and static energy recovery full adder circuits. Table. I gives power dissipation values under the operating conditions $V_{DD}=1.8V$, $C_L=20fF$ and frequency 50MHz. Fig.12 shows the variation of power dissipation with the frequency for the different circuit implementations.

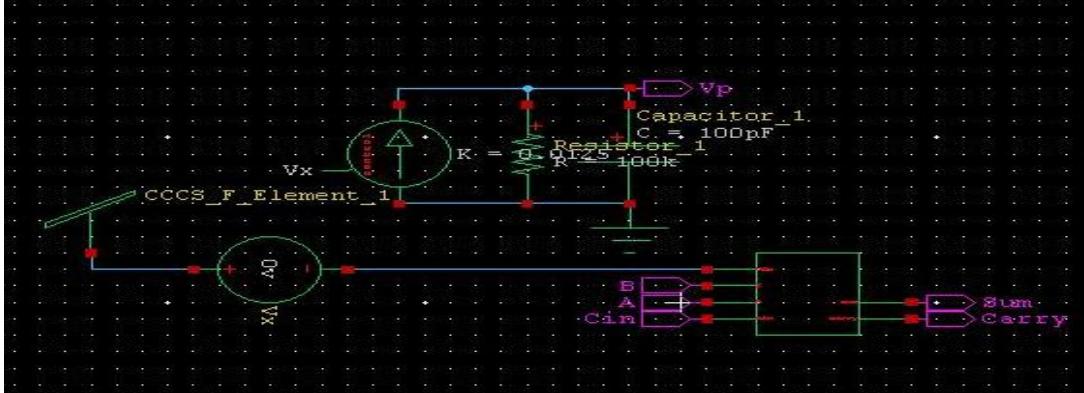


Figure 10 power meter simulation setup for conventional CMOS adder

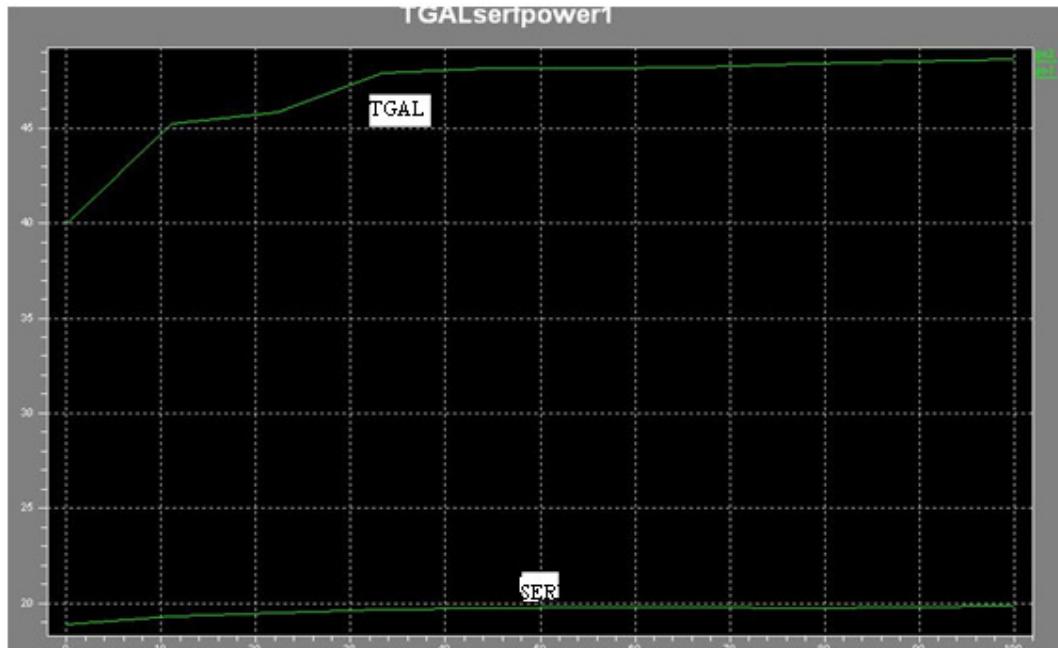


Figure 11 Comparision of TGAL and SERF power with frequency variation from 0 to 100MHz

Table 1 Power dissipation of various adders under the operating conditions ($V_{DD}=1.8v$, $C_L=20fF$, $f_{clk}=50MHz$)

Parameter	ADDER TYPE						
	CMOS	PL	TGL	PAL	PFAL	TGAL	SERF
Transistor Count	28	22(24 ^a)	20	10	38	60	10
Power dissipation(μW)	1.9	1.2	2.1	0.06	0.05	0.85	0.08

^a if optional pMOS transistors are considered

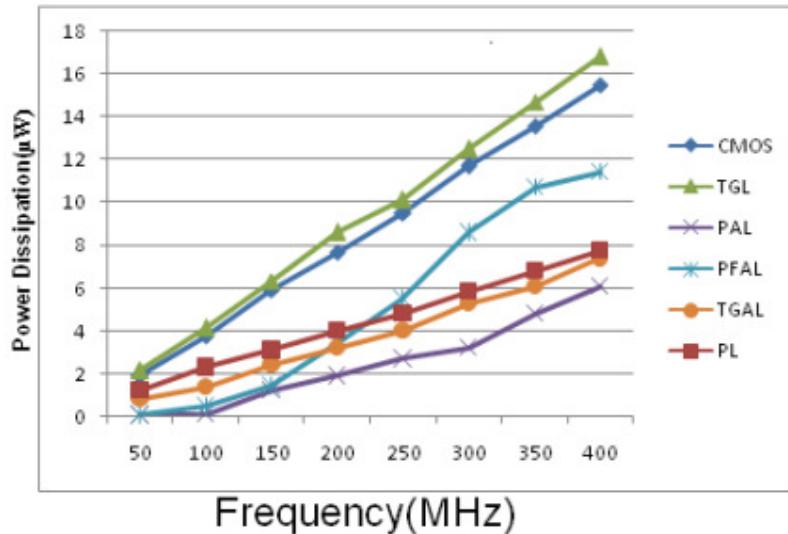


Figure 12 Variation of power dissipation with frequency for different full adder circuits

5. CONCLUSION

In this paper we compared the performance of different adiabatic logic adder circuits with traditional CMOS adder circuits. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

REFERENCES

- [1] W.C. Athas, L. Svensson, J.G. Koller, N.Tzartzanis and E.Y.Chou (1994), "Low-power Digital Systems Based on Adiabatic-switching Principles," IEEE Transactions on VLSI Systems Vol. 2, No. 4, pp. 398-407.
- [2] A. Chandrakasan, S. Sheng and R. Brodersen, (1992)"Low-power CMOS digital design," IEEE Journal of Solid State Circuits, Vol. 27, No 4, pp. 473-484.
- [3] N. Zhuang and H.Wu, (1992) "A New Design of the CMOS Full Adder," IEEE Journal of Solid-state Circuits, Vol. 27, No. 5, pp 840-844.
- [4] S.Kang and Y.Leblebici (2003), CMOS Digital Integrated Circuits - Analysis and Design, McGraw-Hill.
- [5] R. K. Navi, Md.Reza Saatchi and O.Daei,(2009) "A High-Speed Hybrid Full Adder," European Journal of Scientific Research,Vol 26 No.1,pp 29-33.
- [6] D. Soudris, C. Piguet and C. Goutis,(2002) " Designing CMOS Circuits for Low Power, European Low-Power Initiative for Electronic System Design", Reading pp 71-96, Kluwer Academic Publishers.
- [7] D. Soudris, V. Pavlidis and A. Thanailakis,(2001) "Designing Low-Power Energy Recovery Adders Based On Pass Transistor Logic," IEEE.
- [8] R. Shalem, E. John and L.K. John, "A Novel Low Power Energy Recovery Full Adder Cell", (publisher unknown).
- [9] A.G.Dickinson and J.S.Denker,(1995) "Adiabatic Dynamic Logic," IEEE Journal of Solid-state Circuits, Vol. 30 No.3, pp 311-315.

- [10] M.Alioto and G.Palumbo, (2001) "Power Estimation in Adiabatic Circuits: A Simple and Accurate Model", IEEE Trans on VLSI Systems, Vol. 9, No. 5, pp 608-615.
- [11] R.K. Yadav, A.K. Rana, Shweta Chauhan , Deepesh Ranka and Kamalesh Yadav (2011) "Adiabatic Technique for Energy Efficient Logic Circuits Design" Proceedings of ICETECT pp 776-780
- [12] J. Fischer, E. Amirante, A. B. Stoffi, and D. S. Landsiedel, (2004) "Improving the positive feedback adiabatic logic family," in Advances in Radio Science, pp. 221–225.
- [13] N. Anuar, Y.Takahashi, and T. Sekine, (2009) "Fundamental logics based on two phase clocked adiabatic static logic" Proceedings of IEEE ICECS pp. 503–506.
- [14] S. Kim, C.H. Ziesler, and M.C. Papaefthymiou, (2005) "Charge-recovery computing on silicon," IEEE Trans. Computers, vol. 54, no. 6, pp. 651–659.
- [15] E .S .Chew, M.W. Phy, and W.L. Goh (2009) "Ultra Low-Power Full-Adder for Biomedical Applications" IEEE pp115-118.
- [16] C. H. Chang, J. Gu and M. Zhang, (2005) "A review of 0.18um full adder performances for tree structured arithmetic circuits," IEEE Transactions on VLSI Systems, vol. 13, no. 6, pp. 686-695.
- [17] S. Goel, A. Kumar and M. A. Bayoumi,(2006) "Design of robust, energy efficient full adders for deep-submicrometer design using hybrid CMOS logic style," IEEE Transactions on VLSI Systems, vol.14, no.12, pp. 1309-1321.
- [18] A Blotti, M Castellucci, and R Saletti (2002) "Designing Carry Look-Ahead Adders with an Adiabatic Logic Standard-Cell Library" PATMOS, pp 118-127
- [19] Dhireesha K and E John (2005) "Implementation of Low Power Digital Multipliers Using 10 Transistor Adder Blocks", Journal of Low power Electronics, Vol 1 No.3 P 1-11.
- [20] M.Alioto and G.Palumbo, (2000) "Performance Evaluation of Adiabatic Gates" IEEE Trans on Circuits and Systems-I, VOL. 47, NO. 9, pp 1297-1308.
- [21] A Blotti. S Di Pascoli, R Saletti (2002) "A Comparison of Some Circuit Schemes for Semi-Reversible Adiabatic Logic" International Journal of Electronics. Vol. 89, No. 2, pp. 147–158.

Authors

V.V.G.S.Rajendra Prasad completed his B.Tech from Andhra University and M.Tech from JNTU,Hyderabad with specialization VLSI System Design



Y.Sunil Gavaskar Reddy Completed his B.Tech from JNTU Hyderabad and M.S fro, IIIT Pune with specialization Advance microelectronics & VLSI Design.

