

# SUB TEN MICRON CHANNEL DEVICES ACHIEVED BY VERTICAL ORGANIC THIN FILM TRANSISTOR

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## ABSTRACT

*The channel lengths of the top contact organic thin film transistors are usually defined during their fabrication by optical lithography or by shadow masking during the metal deposition process. Realizing short channel (sub-ten micron channel length) transistors by lithography will require costly lithography equipment. On the other hand, it is extremely challenging to achieve short channel transistors using the low cost shadow mask process. One low cost method of achieving short channel devices is to build vertical transistors with the transistor, where the channel gets defined in the vertical part of the device.*

*This paper shows that vertical channel top contact organic thin film transistor has been successfully realized on the vertical edge of trench. This helped in creating the device with channel lengths less than ten microns, much smaller than what could be typically achieved with the use of shadow masks.*

## KEYWORDS

*Organic Thin Film Transistors OTFT, Radio Frequency Identification RFID, Poly-thiophene PT, Thin film transistor TFT.*

## 1. INTRODUCTION

Since the last 30 years, OTFT have gained a high interest due to its potential application in small and large area electronics and low cost flexible display applications. The promising applications for OTFT include active matrix drivers for large area display, large area sensor matrix, and active matrix drivers for electronics paper and basic element for logic circuit in RFID tags. [2]

Since the first report on OTFT in 1986, which was based on PT polymer with mobility of  $10^{-5}$  [ $\text{cm}^2/\text{Vs}$ ] [1], great progress has been made in synthesis of new organic semiconductors and insulators materials, improving manufacturing techniques and in development of new TFT structures. The microscopic mobility upper limits of organic molecular crystal tested by time of flight experiments at room temperature is between 1 to 10 [ $\text{cm}^2/\text{Vs}$ ], impose by the weak intermolecular force between neighboring molecules [1]. There are also large efforts in pushing disordered polymers semiconductors, which are inherently more stable, toward the high mobility regime, but values higher than 0.1 seem to be out of reach at the moment.

Despite the fact that OTFT cannot compete with inorganic single crystalline TFT performance, but still OTFT have reached mobility's of 1.5 [ $\text{cm}^2/\text{Vs}$ ] which has been achieved in pentacene based top contact OTFT and current on/off ratio greater than  $10^7$ , and sub threshold slope  $< 0.3$  V/decade [1, 4]. Today, many research groups continue to improve the Pentacene OTFT by using different insulator materials, encapsulation methods, or by doped the Pentacene film. It becomes

obvious why we are doing research on pentacene based OTFT. This is more clear from advantages of OTFT technology which are listed below:

1. Mobility of pentacene (based OTFT) is comparable to amorphous silicon. The room temperature drift mobilities are found to range from 0.0005 to 0.0006 cm<sup>2</sup>/Vsec for holes in the p-type material [3] which is comparable with the mobility which we get in pentacene based top contact OTFT.
2. The processing of top contact OTFT is low cost and does not require sophisticated tools, which are required in the Si based TFT processing steps.
3. As we can see from table 1 that substrate material for OTFT is paper and that's why it is Compatible with flexible technology.
4. Using OTFT large area displays can be produced.
5. Since process steps of OTFT are very simple hence it is possible that OTFT can be printed.

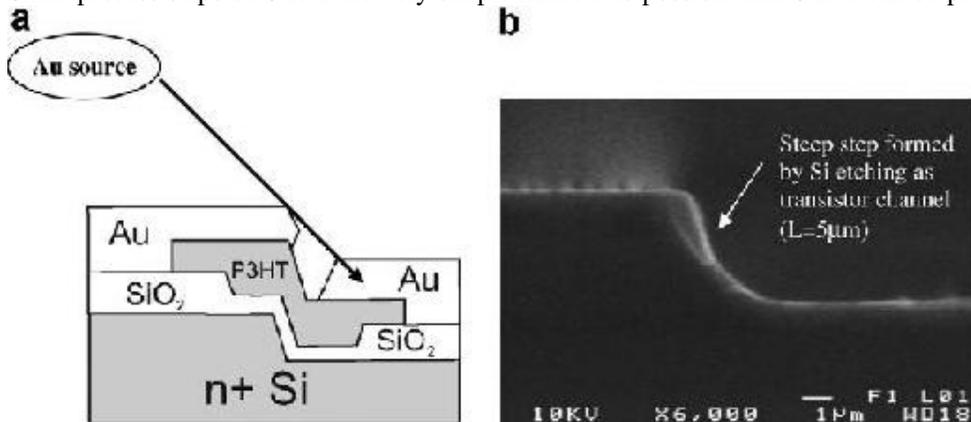


Figure 1: (a) Schematic device structure of a top contact vertical channel transistor. (b) A SEM image of a 5µm step step after the etching of Si. [13]

Since channel formed in top contact OTFT will be between gold which is done by placing wire in the mask and hence the thickness of wire will decide the channel length. So for decreasing the channel length a top contact vertical OTFT can be fabricated as shown in figure 1. This is done by forming a steep step on Si surface by etching Si from the place where we want to make step. Then depositing P3HT and gold at an angle to get the top contact vertical OTFT on the steep step [13].

## 2. OPERATING PRINCIPLE

A thin film transistor is composed of three basic elements:

1. A thin semiconductor film;
2. An insulating layer;
3. Three electrodes (source, drain and gate).

Two of them, the source and the drain, are in contact with the semiconductor film at a short distance from one another. The third electrode, the gate, is separated from the semiconductor film by the insulating layer. Figure 2 illustrates a widely used configuration of these elements, but as will be shown in the following, there exist several alternative ways of arranging the elements of the device. To demonstrate the operating mode of the thin-film transistor, typical current voltage characteristics are shown in Figure 3. These curves were measured on a device made of pentacene as the semiconductor and gold as source and drain electrodes. The Fermi level of gold and HOMO LUMO levels of pentacene are shown in Fig. 2. When a positive voltage is applied to the gate, negative charges are induced at the source electrode.

Table 1. MATERIAL FOR DIFFERENT TFT TECHNOLOGIES AND THEIR PROCESSING TEMPERATURE WITH COMPATIBLE SUBSTRATE TYPE. [5]

Technology	Process temperature	Substrate Material
ULSI	> 1050°C	Crystal Si
Poly Si: HTPS LTFS (TFT on glass)	1050°C > T > 600°C = 600°C (anneal) = 550°C (MILC) = 425°C (ELA)	Quartz Corning 1737 Corning 7539 Display glass
ULTPS	< 150°C	Polymer
Amorphous Si	< 250°C	Polymer, Glass
OTFT	Room Temperature	Paper

As can be seen in Fig. 2, the Fermi level of gold is far away from the LUMO level, so that electron injection is very unlikely. Accordingly, no current passes through the pentacene layer, and the small measured current essentially comes from leaks through the insulating layer. When the gate voltage is reversed, holes can be injected from the source to the semiconductor, because the Fermi level of gold is close to the HOMO level of pentacene. Accordingly, a conducting channel forms at the insulator semiconductor interface, and charge can be driven from source to drain by applying a second voltage to the drain. For this reason, pentacene is said to be a p-type semiconductor. However, it should be pointed out that this concept differs from that of doping in conventional semiconductors, which can be made either n-type or p-type by introducing tiny amounts of an electron donating or electron withdrawing element.

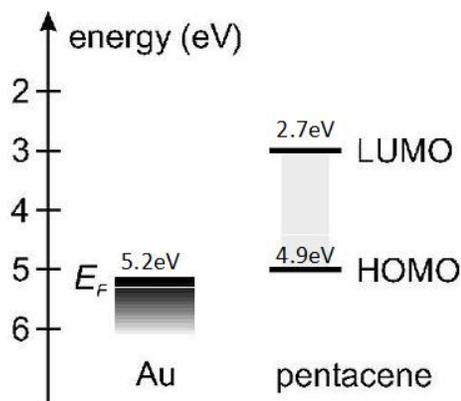


Figure 2: This energy scheme compares the work function of gold to the energy of the frontier orbital's of pentacene.[6]

Symmetrically, an organic semiconductor will be said n-type when the source and drain electrodes can inject electrons in its LUMO level, provided electron transport does occur, i.e., electron mobility is not too low. Basically, the thin-film transistor operates like a capacitor. When a voltage is applied between source and gate, a charge is induced at the insulator-semiconductor interface. This charge forms a conducting channel, the conductance of which is proportional to the gate voltage. At low drain voltages, the current increases linearly with drain voltage (Fig. 3), following Ohm's law. When the drain voltage is compared to gate voltage, the voltage drop at drain contact falls to zero and the conducting channel is pinched off. This corresponds to the so-called saturation regime where the current becomes independent of the drain voltage. In the

transfer characteristic (right-hand side of Fig. 2), the current is plotted as a function of the gate voltage at a constant drain bias.

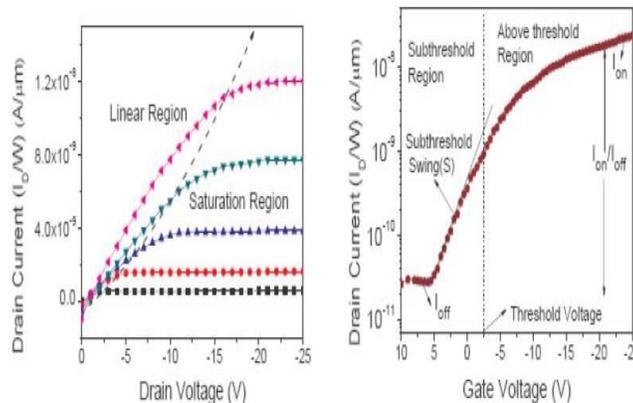


Figure 3: (a) Output characteristics for different gate voltages. (b) Transfer characteristics for a certain drain voltage [5].

Below a given threshold, the current increases exponentially. This corresponds to the below threshold regime. In the above threshold regime, the current becomes proportional to the gate bias, as expected from the above description of the operating mode of the transistor. Organic semiconductors are dielectric at room temperature. So to carry out the charge conduction, charges are induced into organic material by injection mechanism from the source and drain electrodes. By applying negative gate voltage ( $V_g$ ) positive charges are attracted towards dielectric organic semiconductor interface. The attracted charges accumulate at the dielectric organic semiconductor interface and form a channel of carriers. These carriers are collected at drain electrode by creating a potential drop from source to drain. In OTFT two types of measurements are possible by varying the gate ( $V_g$ ) and drain ( $V_d$ ) voltage, with respect to the source voltage which is normally grounded. They are the output characteristics between drain current ( $I_d$ ) and drain voltage for a constant gate voltage. And transfer characteristics between drain current and gate voltage for constant drain voltage. These are shown in Fig. 3. From the output characteristics two regions can be clearly demarcated they are the linear and saturation region. The transistor properties like mobility, threshold voltage, subthreshold slope, and the  $I_{on}/I_{off}$  ratio are shown in transfer characteristics. The definitions of each of these terms are explained below:

**MOBILITY:** It is the velocity with which carriers move per unit applied field.

**THRESHOLD VOLTAGE:** It is the minimum gate voltage at which the OTFT begins to conduct or it is the minimum gate voltage at which accumulation of holes takes at the insulator semiconductor interface of an OTFT. This is estimated from the transfer characteristics of saturation region ( $V_d \gg V_g$ ).

**SUBTHRESHOLD SLOPE:** It is defined as the drain voltage required to increase the drain current by one decade in the subthreshold region. It is an important parameter which explains how best we can use the transistor as a switch.

**ON CURRENT ( $I_{ON}$ ):** Drain current above threshold voltage ( $V_T$ ) at which saturation takes place.

**OFF CURRENT ( $I_{OFF}$ ):** It is the Drain current below threshold Voltage ( $V_T$ ) in transfer characteristics  $I_d - V_g$  graph.

Estimation of above parameters is done by assuming that OTFT follows ideal MOSFET equations. In the linear region ( $V_D \ll V_G - V_T$ ) the channel is continuous and  $I_D$  is given by

$$I_{D,lin} = \frac{W\mu C_i}{L} \left[ (V_G - V_T)V_D - \frac{V_D^2}{2} \right] \quad (1)$$

where  $C_i$  is the capacitance per unit area of gate insulator,  $L$  and  $W$  are channel length and channel width, respectively. On simplification the above equation changes to

$$I_{D,lin} = \frac{W\mu C_i}{L} (V_G - V_T)V_D \quad (2)$$

Further increasing  $V_D \gg V_G - V_T$  causes electric field to become zero at the drain contact. Due to this around drain contact a depletion area is created, which is called pinch off. Beyond this point, the saturation regime begins and the drain current is now independent of drain voltage, being controlled by gate voltage alone. In this region, the drain current varies quadratically with the field:

$$I_{D,lin} = \frac{W\mu C_i}{2L} (V_G - V_T)^2 \quad (3)$$

Eqn 1-3 represent the expressions used to calculate field effect mobility in OTFTs. The mobility can be estimated from the gate voltage sweep of Fig. 3 (b), the field effect mobility in the linear region is given by transconductance which is defined by

$$g_m = \frac{\partial I_{D,lin}}{\partial V_G} \quad (4)$$

For small and constant  $V_D$ , mobility in the linear region is calculated from the relationship

$$\mu_{lin} = \frac{L g_m}{W C_i V_D} \quad (5)$$

In the saturation region mobility is calculated using

$$\mu_{sat} = \frac{2L}{W C_i} \left( \frac{\partial \sqrt{I_{D,sat}}}{\partial V_G} \right)^2 \quad (6)$$

### 3. DEPOSITION

#### 3.1 PENTACENE DEPOSITION

Pentacene deposition for top contact vertical OTFT is also done similar to top contact OTFT in thermal evaporator as shown in Figure 4. For top contact vertical OTFT the only difference in pentacene deposition with respect to top contact OTFT is keeping the substrate at an angle while depositing rather all process remains same. Weighed amount of pentacene 5 mg is placed in  $Al_2O_3$  coated Mo boat and substrates are loaded. Here Substrate is hold on the substrate holder not horizontal rather at an angle so that pentacene will be deposit on the trench height also which is also shown in figure 4. After this the chamber is sealed. The system is evacuated by using diffusion pump which is assisted by the rotary pump. After attaining a vacuum of  $10 \times 10^{-6}$  mbar preheating of substrate is started at  $100^\circ C$  for 30 minutes. Then the substrate temperature is decreased from  $100^\circ C$  to required deposition temperature. We wait for a vacuum of  $3 \times 10^{-6}$  mbar to start our deposition. Deposition rate is maintained at some predefined experimental rate by adjusting the variac manually. For top contact vertical OTFT also we keep the pentacene deposition rate of 20-60 Å/min and thickness of pentacene was kept 80 nm for top contact vertical OTFT which worked. After the deposition substrate is removed from chamber and kept in box in

deicator. For my top contact vertical OTFT fabrication work substrate was kept at an angle of  $45^\circ$  while depositing pentacene.

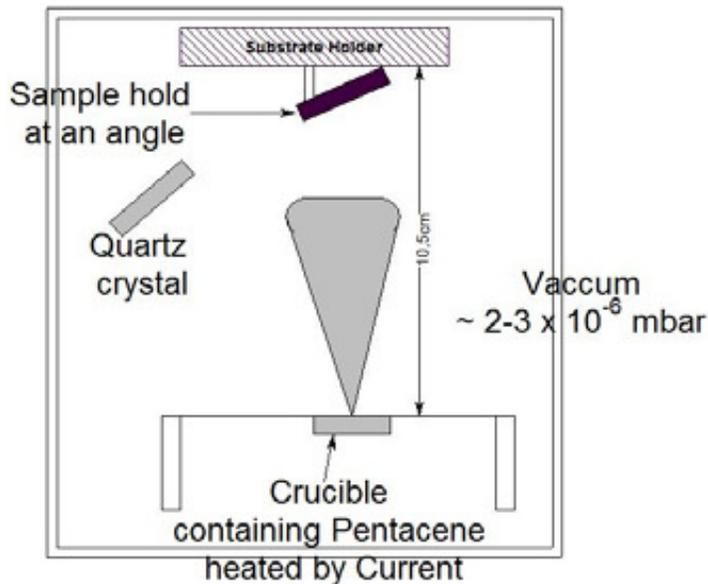


Figure 4: Thermal evaporator unit used for deposition of pentacene for top contact vertical OTFT.

### 3.2 GOLD DEPOSITION (ELECTRON BEAM/THERMAL EVAPORATION)

#### 3.2.1 FOR TOP CONTACT OTFT

Source and drain contacts, channel formation are made on the pentacene using e-beam deposition or thermal evaporator. For this purpose we use a shadow mask. The shape, dimension of mask, channel length and channel width area are shown in a Figure 5. Our pentacene substrate is placed on the substrate holder. The mask is fixed on pentacene deposited substrate with the wire touching the substrate. The entire setup is now ready to load in deposition chamber. Next we wait for vacuum of  $5 \times 10^{-6}$  mbar. After this we deposit 50 nm gold at determined experimental rate for making source and drain contacts.

#### 3.2.2 FOR TOP CONTACT VERTICAL OTFT

For top contact vertical OTFT we just need to attach substrate to the substrate holder at an angle such that gold should not be deposited on the trench height and here we will require mask without the wire.

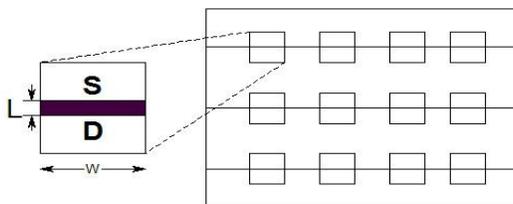


Figure 5: Dimensions of the shadow mask used for top contact OTFT.

After attaching this mask on the substrate such that trench height will be in middle as shown in figure 6. Now after adjusting the mask on substrate, substrate is hold on holder at an angle such that gold will not be deposited on trench height. The entire setup is now ready to load in deposition chamber. Next we wait for vacuum of  $5 \times 10^{-6}$  mbar. After this we deposit 50 nm gold at determined experimental rate for making source and drain contacts. For top contact vertical OTFT fabrication, substrate was kept at an angle of  $45^\circ$  while depositing gold.

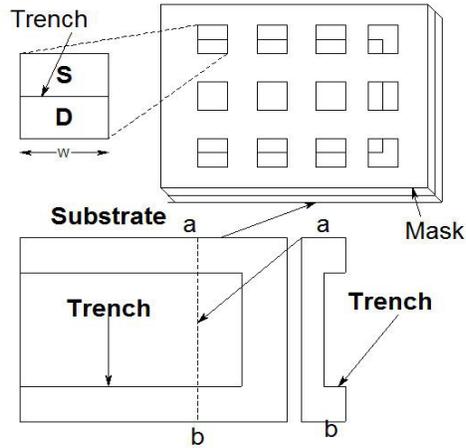


Figure 6: Shadow mask used for top contact vertical OTFT .

#### 4. OUTPUT AND TRANSFER CHARACTERISTICS

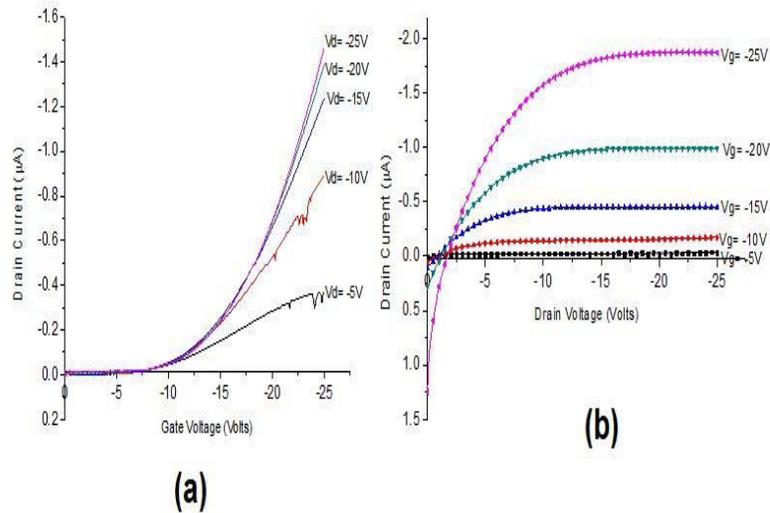


Figure 7: (a) Transfer characteristics for top contact OTFT ,(b) Output characteristics for top contact OTFT .

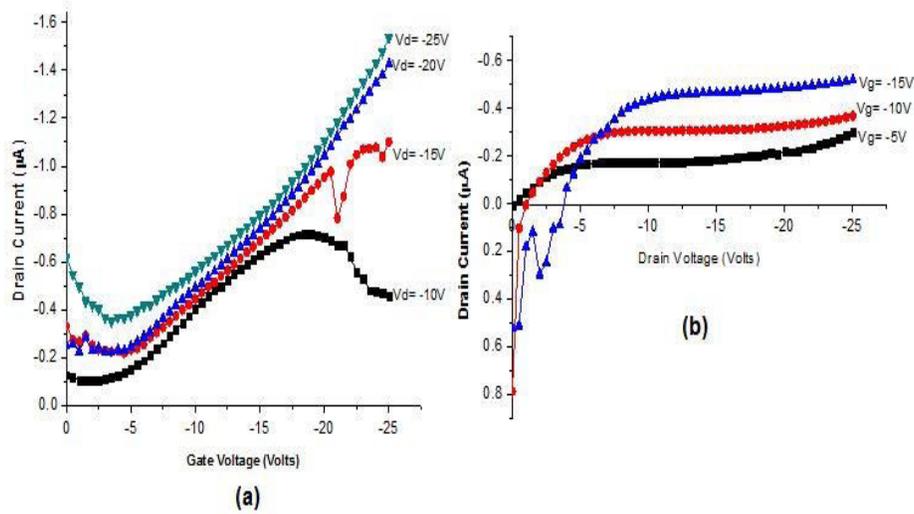


Figure 8: (a) Transfer characteristics for top contact vertical OTFT, (b) Output characteristics for top contact vertical OTFT .

Using instrument Keithly 4200, output and transfer characteristics were measured for both normal and vertical OTFTs. Figure 7 shows the output and transfer characteristics for top contact OTFT with gate voltage varying with step of  $-5\text{V}$  from  $-5\text{V}$  to  $-25\text{V}$  in transfer characteristic and drain voltage varying with a step of  $-5\text{V}$  from  $-5\text{V}$  to  $-25\text{V}$  is shown in output characteristics. Similarly, figure 8 shows the output and transfer characteristics for top contact vertical OTFT where gate voltage is varying with a step of  $-5\text{V}$  from  $-10\text{V}$  to  $-25\text{V}$  in transfer characteristics and similarly drain voltage is also varying with a step of  $-5\text{V}$  in output characteristics. For top contact OTFT we were not getting the transfer characteristics for  $V_D = 0\text{V}$  and output characteristics for  $V_G = 0\text{V}$ .

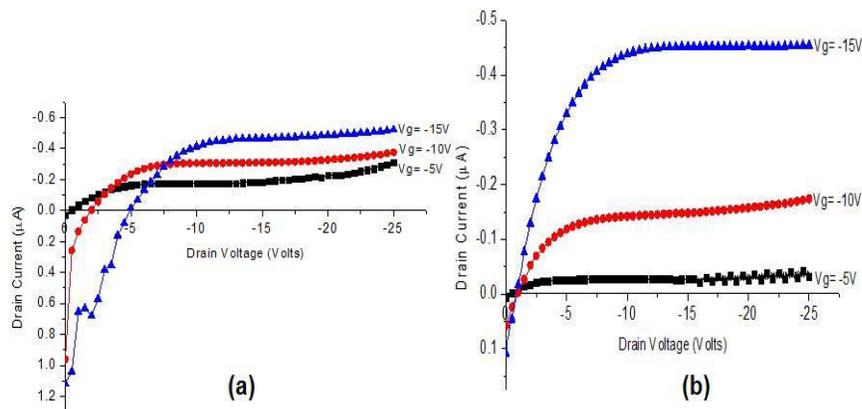


Figure 9: Output characteristics for (a) top contact vertical OTFT and (b) top contact OTFT with gate leakage removed.

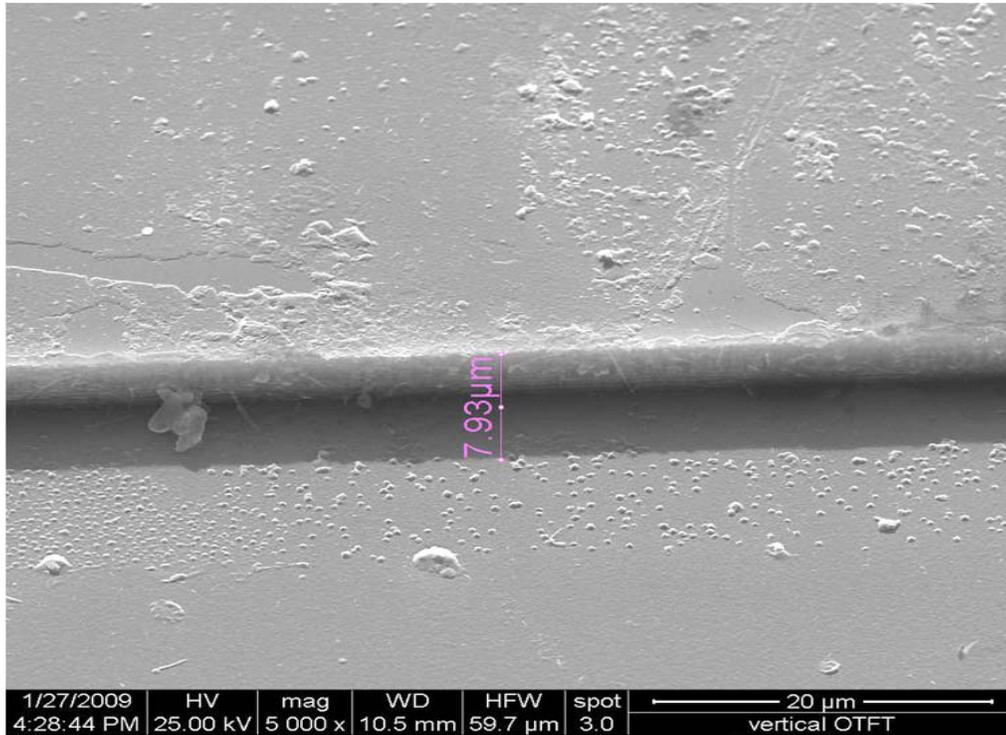


Figure 10: SEM image trench height after gold deposition is done for top contact vertical OTFT.

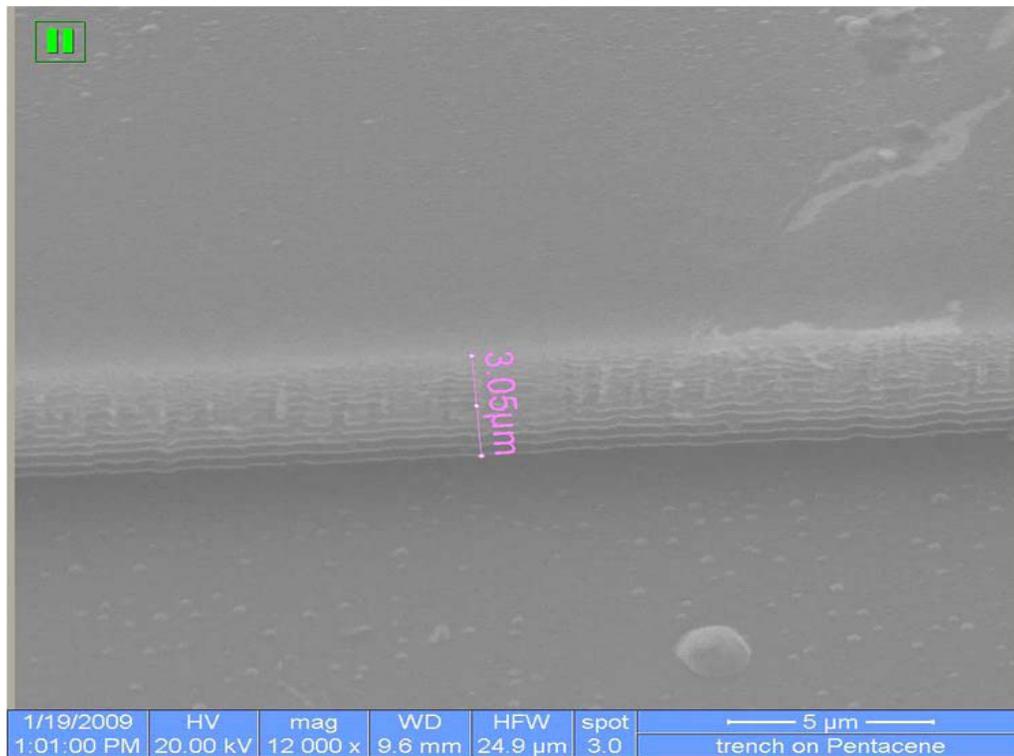


Figure 11: SEM image of trench height after deposition of pentacene

For top contact vertical OTFT we were not the transfer characteristics for  $V_D = 0V, -5V$  and output characteristics for  $V_G = 0V, -20V, -25V$  as shown in figure 7 and figure 8 respectively. The channel length for top contact OTFT devices is  $140\mu m$  and that for top contact vertical OTFT is around  $8\mu m$ . We can also check out from figure 7 and 8 that at  $V_D = 0V$  for output characteristics and for  $V_G = 0V$  for transfer characteristics the value of Drain current is not zero rather it is positive value. This can either be leakage current which is flowing through oxide. So in order to check this the current through oxide was also measured which is removed from the actual measured values to get the characteristics for top contact OTFT and top contact vertical OTFT with gate leakage removed. These evaluated output characteristics for top contact OTFT and top contact vertical OTFT with gate leakage removed is shown in figure 9. From figure 10 we can see that gold was not deposited on the trench height and the portion shadowed by trench height. So we get a channel length of around  $8\mu m$  without using the sophisticated mask.

## 5. CONCLUSION AND FUTURE WORK

For this paper, top contact OTFT and top contact vertical OTFT devices were fabricated. Both top contact OTFT and top contact vertical OTFT were made on same substrate (i.e. substrate having  $50nm SiO_2$  thickness). We got results for both top contact OTFT and top contact vertical OTFT on that substrate. For making the top contact vertical OTFT we keep the substrate at an angle of  $45^\circ$  for pentacene and gold deposition. By keeping substrate on that angle we also make top contact OTFT on the substrate simultaneously with top contact vertical OTFT. Thus we got top contact OTFT and top contact vertical OTFT on same substrate and hence got characteristics from that also.

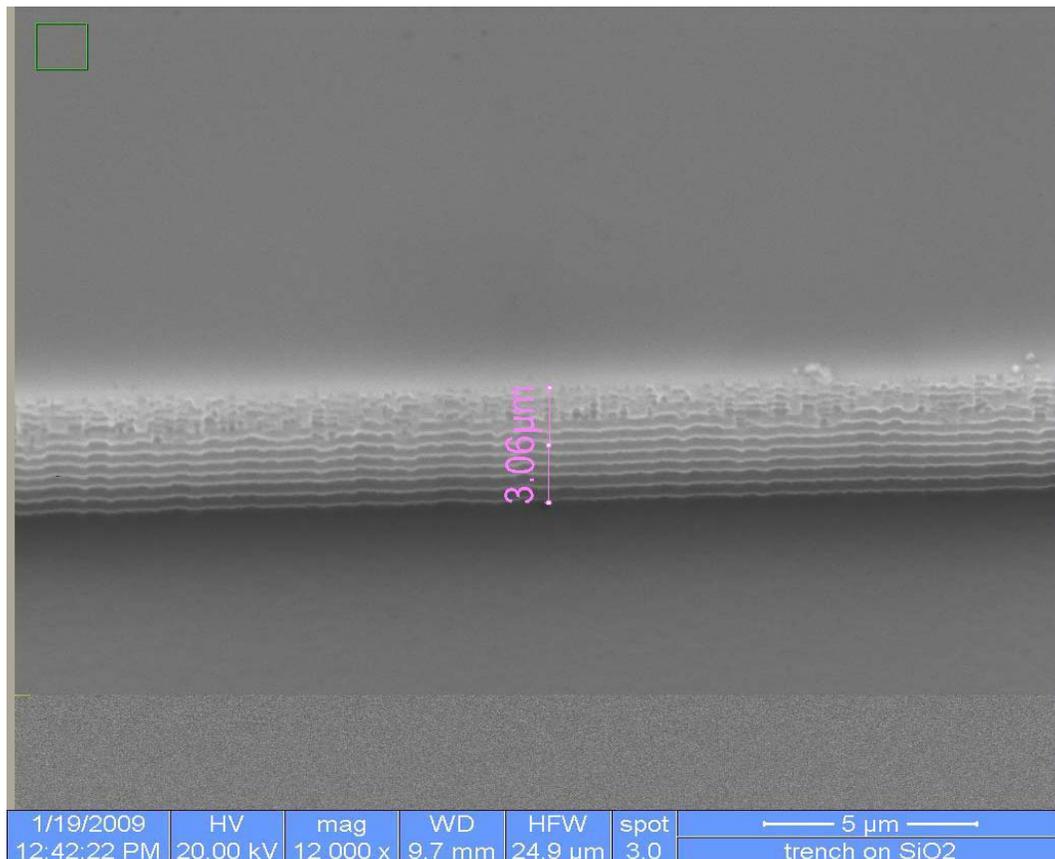


Figure 12: SEM image of substrate trench height without pentacene on SiO<sub>2</sub>.

For top contact vertical OTFT to work we should see while depositing pentacene that it gets deposited on the trench height. So to examine this we took the SEM images of substrate after pentacene deposition which is shown in figure 11. For getting the information of pentacene deposition on that we also took SEM image of substrate without pentacene deposition and with we compared to check whether Pentacene was deposited or not. The SEM image of Substrate without pentacene deposited is shown in figure 12. With this and earlier image you can yourself clarify that pentacene was deposited on that trench height or not. After this we move forward for gold deposition deposition after confirmation of pentacene deposition on the trench height. Also for pentacene deposition earlier we were depositing 50nm of pentacene and when we were not able to get the characteristics for top contact vertical OTFT , thus then we deposit 80nm of pentacene so that by increasing the thickness it might be possible that pentacene will gets deposited on the trench height. Well we don't know about earlier devices weather pentacene was deposited or not but in this one with 80nm pentacene deposition, pentacene got deposited on the trench height and we got top contact vertical organic thin film transistor characteristics. Regarding the future scope of this work, we can come to following conclusions:

1. Results of changing the angle of substrate holder while deposition of pentacene and gold can be checked.
2. TFT with channel length in nm can also be achieved by having a substrate with smaller trench height i.e. trench height in nm.

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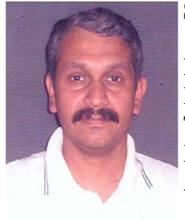
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