AREA OPTIMIZED FPGA IMPLEMENTATION FOR GENERATION OF RADAR PULSE COM-PRESSION SEQUENCES

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ABSTRACT

Pulse compression technique is most widely used in radar and communication areas. Its implementation requires an opti-mized and dedicated hardware. The real time implementation places several constraints such as area occupied, power con-sumption, etc. The good design needs optimization of these constraints. This paper concentrates on the design of optimized model which can reduce these. In the proposed architecture a single chip is used for generating the pulse compression se-quence like BPSk, QPSk, 6-PSK and other Polyphase codes. The VLSI architecture is implemented on the Field Programm-able Gate Array (FPGA) as it provides the flexibility of reconfigurability and reprogrammability .It was found that the pro-posed architecture has generated the pulse compression sequences efficiently while improving some of the parameters like area, power consumption and delay when compared to previous methods.

KEYWORDS

PULSE compression, Ternary sequence, Quaternary sequence, Polyphase sequence,Merit Factor, VLSI architecture, FPGA

1. INTRODUCTION

The Pulse compression codes with low autocorrelation side lobe levels and high Merit factor are useful for radar [20], channel estimation, and spread spectrum communication applications. Pulse compression can be defined as a technique that allows the radar to utilize a long pulse to achieve large radiated energy but simultaneously obtaining the range-resolution of a short pulse. Theoretically, in pulse compression, the code is modulated onto the pulsed waveform during transmission. At the receiver, the code is used to combine the signal to achieve a high range resolution. Range-resolution is the ability of the radar receiver to identify nearby targets. The main criterion of good pulse compression is the Merit factor and discrimination.

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Let

$S = [S_0, S_1, S_2 \ldots S_{N-1}]$ be a real sequence of length N.
Then aperiodic autocorrelation function of sequence S of length N is given as,

$$Q(K) = \sum_{i=0}^{N-1-K} S_i S_{i+K}$$

Where k=0, 1, 2… N-1 is its aperiodic autocorrelation. The Merit factor F is defined as the ratio of energy in the main peak and the side lobes. The merit factor F must be as large as possible for good sequence.

$$F = \frac{Q^2(0)}{2\sum_{K=1}^{N-1} Q^2(k)}$$

Discrimination is used to measure whether coded signal is a good or poor. This means a code with high discrimination is a good code while a code with low discrimination is a poor code. Discrimination can be defined as a ratio of main peak of autocorrelation function to the magnitude of peak side lobe value of autocorrelation function.

$$D = \frac{Q(0)}{max|Q(K)|_{K\neq 0}}$$

Merit factor is used to measure whether coded signal is a good or poor. This means that a code with high Merit factor is a good code while a code with low Merit factor is a poor code. Pulse compression can be achieved using different techniques in which phase coding is the widely used one. These include binary, ternary, quaternary, Quinquenary, etc. The selection of phase coding depends upon the application and requirements.

2. NEED FOR THE PROPOSED ARCHITECTURE

In the field of radar and sonar we have the problem of generating long sequences with peaky autocorrelation [21]. This signal design can be solved through binary, Ternary, Quinquenary and six phase sequences. Hence lot of work was done to generate binary, Ternary and Four Phase sequences with good merit factor and discrimination factor [5-17]. The Hardware Implementation architectures for Pulse compression systems available in the literature have the capability of generating the pulse compression sequences with limited speed [18-19].

To increase the speed of pulse compression system, VLSI architectures were developed for binary, Ternary, Quinquenary and six phase pulse compression systems which were described in literature [1-4]. But the VLSI architecture of six phase pulse compression system [4] has draw backs like it requires six memory units to generate the sine wave with six phases, hence the area is increased and it has generated the sine wave with low resolution i.e. 3bit resolution and if the resolution of the wave is increased the size of each memory unit will increase and hence the total area occupied will further increase and other drawback is it is limited to generate six phase codes

only. To overcome these draw backs we proposed an area efficient VLSI architecture without sacrificing the speed. The other advantage of the proposed VLSI architecture is it can generate different phase coded Pulse compression sequences like binary, Ternary, Quinquenary, six phase and other poly phase sequences, hence it is a single chip solution for generating different pulse compression sequences

3. PROPOSED ARCHITECTURE

The gate count should be as smaller as possible in the design implementation. The proposed model is shown in the Fig. 1. It consists of a pair of counters (up and down), memories (ROMs) and a control circuit. One memory is reprogrammable and the desired type of PSK can be implemented on it. The second memory holds the amplitude values of a sinusoidal waveform which are sampled for every 5^{o} from 0^{o} to 360^{o} in binary form. Equivalent binary representations are obtained by using the 8-bit floating point format. The phase shifted analog sinusoidal wave form is produced by outputting the binary equivalents continuously by controlling with a counter. All the binary values are fed to a DAC to convert digital equivalents to analog. The model has a pair of counters in which one is used as an up-counter and the other as down-counter. Up-counter assigns the starting count taken from the first memory and controls the continuous outputting of the sequences. Down counter sets and resets the up-counter using a control circuit. The model‟s control circuit is simply a Nand gate. From the functional property of Nand gate, it is known that it produces a low logic when all of its inputs are set high. The output from the Nand gate is fed to the up-counter for controlling the total counts or cycles of it. The same clock and clear signals are applied to both the counters. The input sequence is taken to be Barker sequence, which have reduced side lobe levels compared to other possible code sequences. The input sequence length varies from a single bit to several bits depending upon the type of Phase shift of implementation. The counters considered in this paper are 6-bit wide. So, to reset the counter state for every 64 clock cycles, we need additional counter that is implemented using a down-counter.

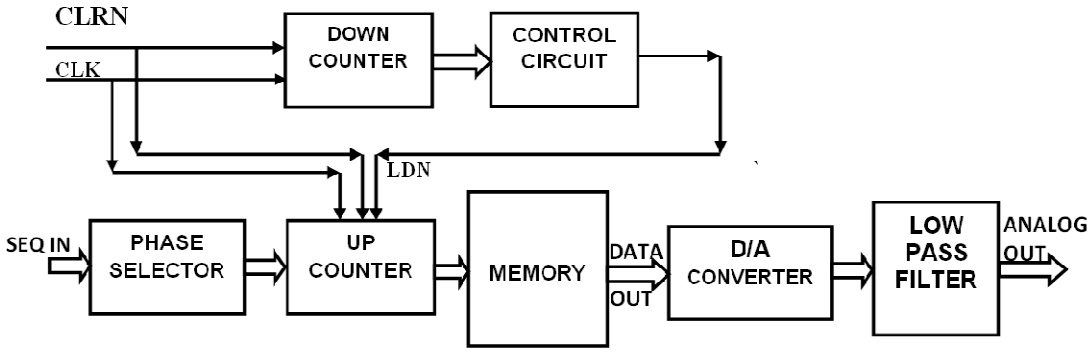

Figure. 1. VLSI architecture for generation of multi-phase (Binary, ternary, quaternary, Quinquenary, 6-Phase, etc...) Pulse Compression Sequences

Exactly after 64 clock cycles, it reaches its initial state thus enabling the control circuit to reset the up-counter. At this instant, the up-counter is loaded with the starting count obtained from the phase selector. The change in input sequence causes the phase change and changes the starting count which is stored in the phase selector. Hence this count is supplied to the up-counter and the

64 clock cycles produce the corresponding samples from the sine memory, thus producing equivalent analog phase shifted waveform.

4. IMPLEMENTATION OF PROPOSED ARCHITECTURE

Using the proposed architecture, a number of models can be developed and implemented on FPGA board. This section explains the VLSI implementations of some widely used pulse compression tech-niques for generation of binary, ternary, quaternary, Quinquenary and 6-phase.

4.1. Binary pulse compression code

Repeatedly flipping the phase of the radio frequency signal within the duration of the pulse, according to a binary code is referred as bi-phase coding. The binary pulse compression sequence consists of the elements +1 and -1. The element +1 is represented by a sine wave with 0^o phase shift and the element -1 is represented by a sine wave with phase shift 180^o.The input is of single bit type and thus has two possible outcomes, which are 0^o and 180^o phase shifts. Thus inputs '0' and '1' produce 0^o and 180^o phase shifted waveforms respectively.

The phase selector memory consists of data of two phase values corresponding to 0^o and 180^o .When input '0' is chosen then the phase selector will output the data value corresponding to 0^o phase, this data is then given to the up counter and the up counter then starts its count from 0_o phase to 360^0phase. These count values starting from 0^o to 360^o are given to the input of the sine memory. Then the sine memory unit will out put the amplitude levels corresponding to phases starting from 0^o,when these values are given to D/A Converter it generates a sine wave stating with 0^o phase And similarly if input '1' is chosen, then phase selector will out put the data corresponding to 180^o phase ,when this value is given to up counter it generates phase values starting from 180^0 phase, these phase values when given to the input of sine memory unit, it generates a sine wave with phase starting from 180^0. Hence a Binary pulse compression code is generated

4.2.Ternary pulse compression code

The Ternary pulse compression sequence elements are +1, 0 and -1. A '+1' is transmitted as sinusoid-al signal with 0° phase shift and a '-1' is transmitted as sinusoidal signal with 180° phase shift. During the period of the element '0' no signal is transmitted. The input is of length 2 bits and '-1' of the ter- nary sequence element is represented by input '11' and '+1' of the ternary sequence element is represented by input '01' and '0' of the ternary sequence element is represented by input '00' .

The phase selector stores the data of two phase values corresponding to 0^0, 180^0 .When input 01 is chosen then phase value corresponding to 0^o phase is selected and is given to the up counter. The up counter then generates all the phases starting from 0^o.When these phase values starting from 0^o is giv-en to sine memory unit, it generates a sine wave starting with 0^o phase. Similarly when input '11' is chosen then phase value corresponding to 180^o phase is selected and a sine wave with 180^o phase shift is generated with the help of counters and memory. When input

’00’ is chosen then no phase value is selected and no sine wave is generated during this input. Hence Ternary pulse compression code is generated

4.3.Quaternary pulse compression code

The Four phase pulse compressed sequence elements are +1, +j, -1, -j. The element ‘+1’ is transmitted as sinusoidal with 0 degree phase shift , the element ‘+j’ is transmitted as sinusoidal signal with 90 degree phase shift, the element ‘-1’ is transmitted as sinusoidal signal with 180 degree phase shift, and the element ‘–j’ is transmitted as sinusoidal signal with 270 degree phase shift. Hence four different phase shifts are observed in the analog sinusoidal output (i.e. 0º, 90º, 180º and 270º). In this case, the input is of length two bits and thus it has four possible outcomes. The input,,00‟ produces a sine wave with 0_o phase ,the input with ,,01‟ produces a sine wave with 90_o phase, the input with ‘10’ produces a sine wave with 180_0 phase and the input with ‘11’ produces a sine wave with 270^0 phase.

The phase selector stores the data of four phase values corresponding to 0º, 90º, 180º and 270º. When input ‘01’ is chosen then phase value corresponding to 90^o phase is selected and is given to the up counter. The up counter then generates all the phases starting from 90^o. When these phase values starting from 90^o is given to sine memory unit, it generates a sine wave with phase 90^o. Similarly sine waves with other phases can be generated. Hence Quaternary pulse compression code is generated

4.4. Quinquenary pulse compression code

The Quinquenary pulse compressed sequence elements are +1, +2, -1, -2, and 0. The element ‘+1’ is transmitted as sinusoidal with 0° phase shift The element ‘+2’ is transmitted as sinusoidal with 72° phase shift The element ‘-1’ is transmitted as sinusoidal with 144° phase shift The element ‘-2’ is transmitted as sinusoidal with 216° phase shift The element ‘0’ is transmitted as sinusoidal with 288° phase shift. The input is of 3 bit length and ‘+1’ of Quinquenary phase pulse compression sequence is represented by 001,‟-1‟ is represented by 011, ‘+2’ is represented by 101, ‘0’ is represented by 000 and ‘-2’ is represented by 111. The phase selector stores the data of four phase values corresponding to 0°, 72°, 144°, 216° and 288°. Depending on the input one of the phase values is selected and with the help of counters and sine memory the sine wave with required phase shift is generated

4.5. Six Phase pulse compression code

The Six phase pulse compressed sequence elements are +1, -1, (0.5+j0.866), (0.5-j0.866), (-0.5+j.866), (-0.5-j0.866). The element +1 is transmitted as sinusoidal signal with 0 degree phase shift , the element -1 is transmitted as sinusoidal signal with 60 degree phase shift, the element (0.5+j0.866) is transmitted as sinusoidal signal with 120 degree phase shift, the element (0.5-j0.866) is transmitted as sinusoidal signal with 180 degree phase shift, (-0.5+j0.866) is transmitted as sinu-soidal signal with 240 degree phase shift, and (-0.5-j0.866) is transmitted as sinusoidal signal with 300 degree phase shift. The input is of 3 bits length and ‘+1’ of Six phase pulse compression se-quence is represented by 000, ‘-1’ is represented by 001, (0.5+j.866) is

represented by 010, (0.5-j.866) is represented by 011, (0.5-j.866) is represented by 100 and (-0.5-j.866) is represented by 101.

The phase selector memory consists of data of six phase values corresponding to 0^o, 60^o, 120^o, 180^o, 240^o and 300^o.depending on the input one of the phase values is selected from the phase selec-tor memory. The selected phase value is given to the input of up counter, and then the up counter ge-nerates all the phase values starting from the phase value selected from the memory. When these phase values are given to the sine memory unit, it generates a sine wave starting with the phase value that has been selected from the phase selector memory is generated. Hence the 6-PSK wave is gener-ated. Similarly the other phase coded sequences can be generated.

6. SIMULATION AND SYNTHESIS RESULTS

The waveform window in figure 2 shows the Behavioral simulation results of the Generation of the Binary pulse compression sequence elements '+1' And '-1' .The element '+1' is transmitted as sinu-soidal signal with 00 phase shift. The element '-1' is transmitted as sinusoidal signal with 1800 phase shift.

The waveform window in the figure 3 shows the Behavioral simulation results of the Generation of the Ternary phase pulse compression sequence elements +1, 0, +1 and -1. The element '+1' is transmitted as sinusoidal signal with 00 phase shift. The element '-1' is transmitted as sinusoidal signal with 1800 phase shift and no signal is transmitted during transmission of element '0'.

The waveform window in the figure 4 shows the Behavioral simulation results of the Generation of the Quaternary pulse compression sequence elements -1, +1, +j and -j. The element '+1' is trans-mitted as sinusoidal signal with 00 phase shift. The element '+j' is transmitted as sinusoidal signal with 720 phase shift. The element '-1' is transmitted as sinusoidal signal with 1800 phase shift and the element '-j' is transmitted as sinusoidal signal with 2160 phase shift.

The waveform window in the figure 5 shows the Behavioral simulation results of the Generation of the Quinquenary pulse compression sequence elements 0, +1, -1,-2, +2, and 0. In the figure we can clearly see that the elements 0, +1, -1, -2, +2, and 0 are transmitted with phases 288°, 0°, 144°, 216° and 72°.

The waveform window in the figure 6 shows the Behavioral simulation results of the Generation of the six phase pulse compression sequence elements (0.5+j0.866), (0.5-j0.866) and (-0.5-j0.866), +1 and The waveform window in the figure 7 shows the Behavioral simulation results of the Genera-tion of the six phase pulse compression sequence elements +1, -1, (-0.5+j0.866) and (0.5+j0.866). From the diagrams we can clearly see that the elements +1, -1, (0.5+j0.866), (0.5-j0.866), (-0.5+j.866) and (-0.5-j0.866) are transmitted as sinusoidal signal with phases 0^o, 60^o, 120^o, 180^o, 240^o and 300^o respectively.

6.1. Generation of Binary Pulse Compression sequence

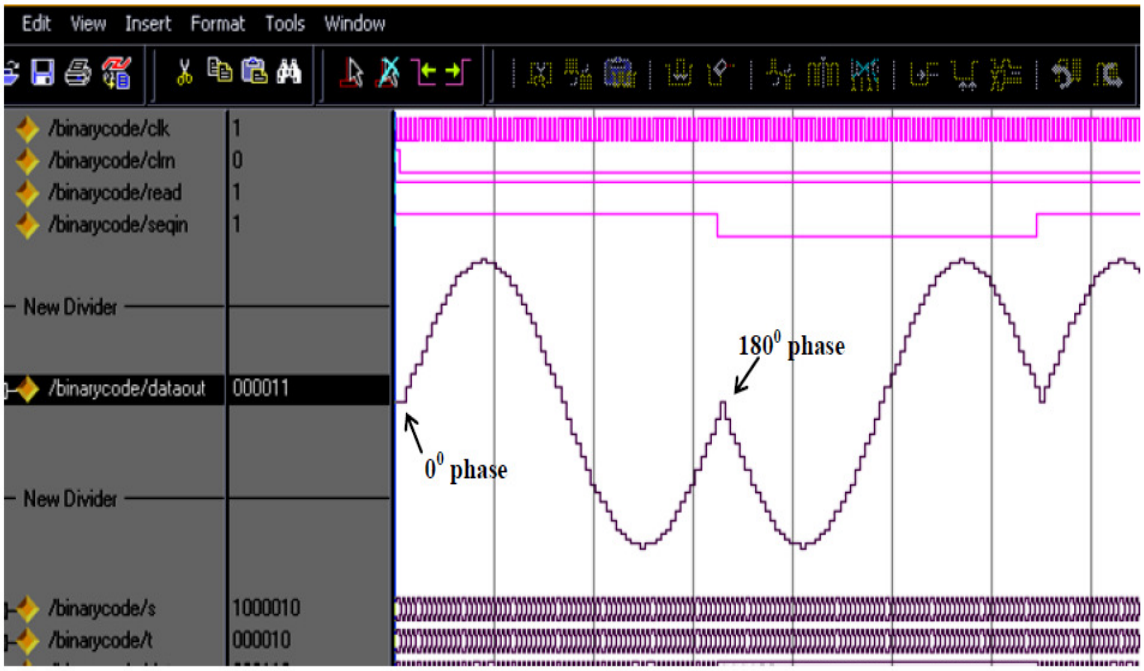

Figure.2. simulation result for generation of Binary pulse compression sequence

6.2. Generation of Ternary Pulse Compression sequence

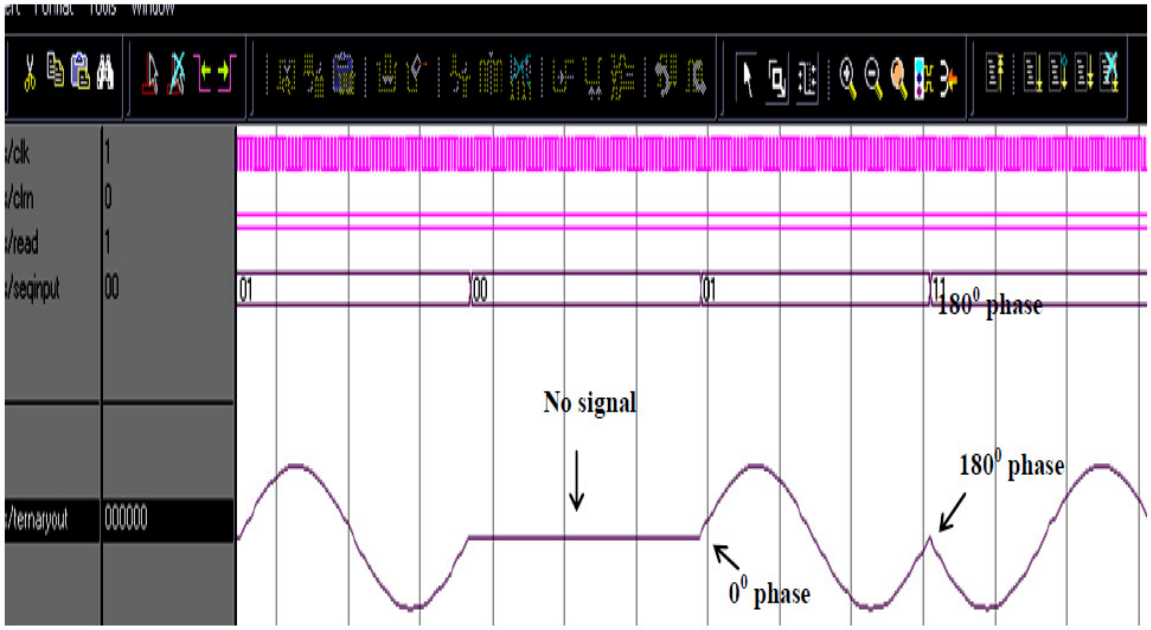

Figure.3. simulation result for generation of Ternary pulse compression sequence

6.3. Generation of Quaternary Pulse Compression sequence

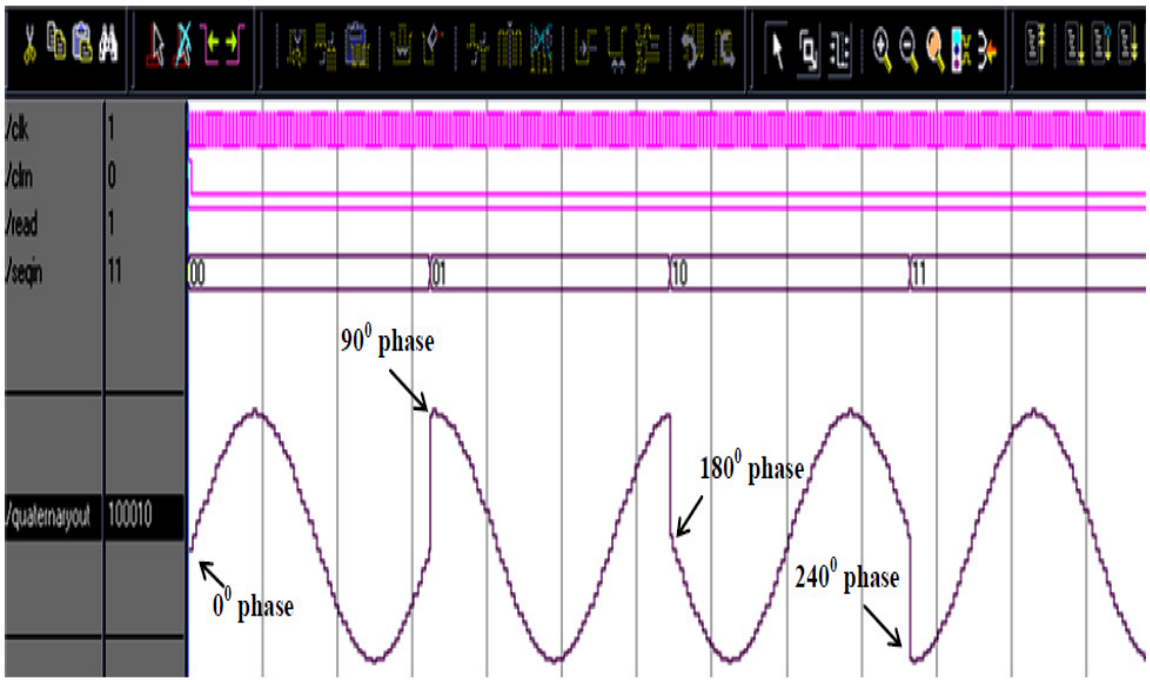

Figure.4. Simulation result for quaternary pulse compression sequence

6.4. Generation of Quinquenary Pulse Compression sequence

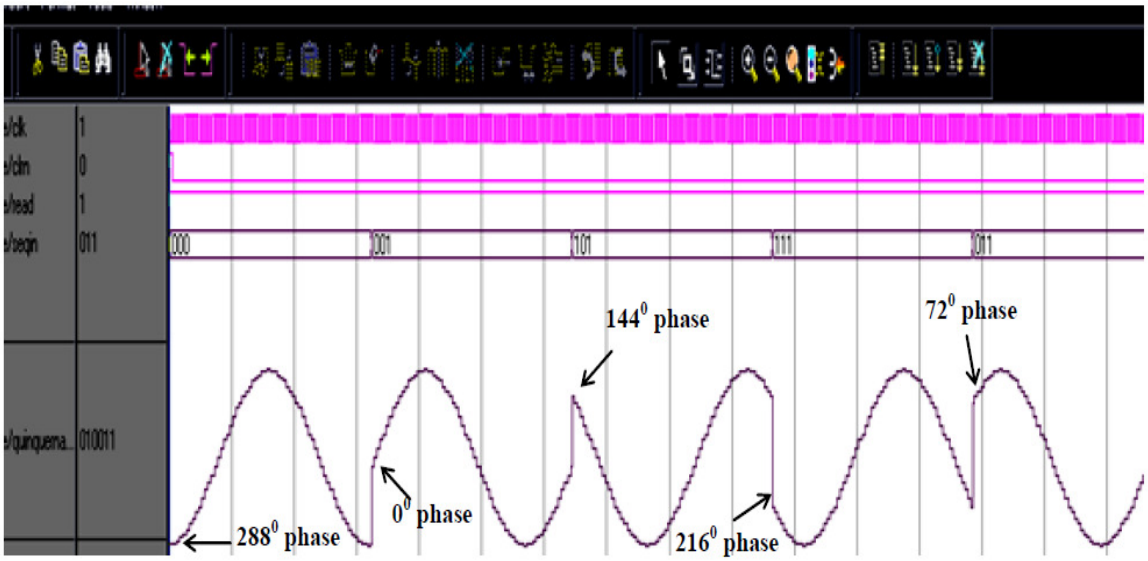

Figure.5. simulation result for generation of Quinquenary pulse compression sequence

6.5. Generation of 6-PSK Pulse Compression sequence

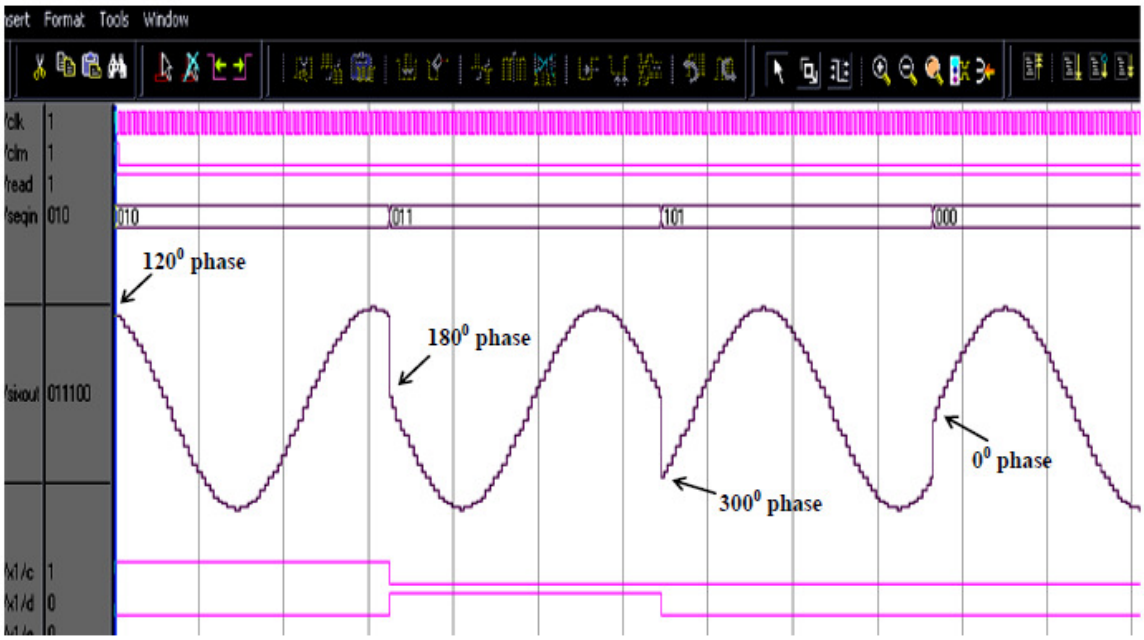

Figure.6. simulation result for generation 6-PSK sequence

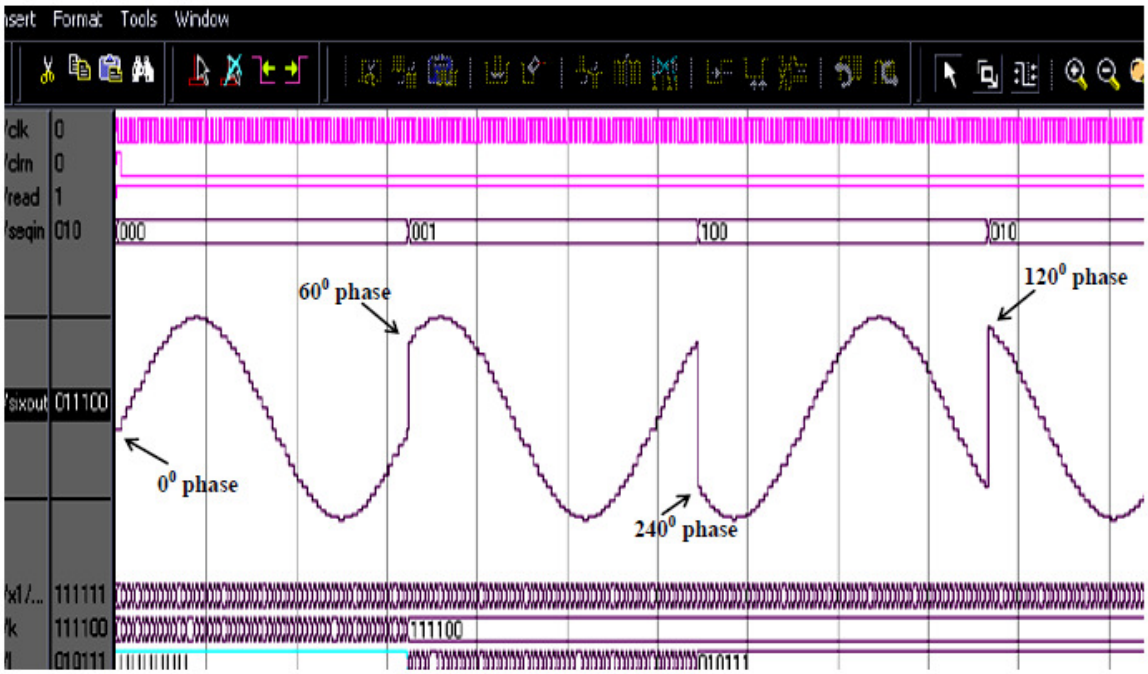

Figure.7. simulation result for generation 6-PSK sequence

6.6. Synthesis Result

Design summary	Binary Pulse Compression		Ternary Pulse Compression		Quinquenary Pulse Compression	
Logic Utilization:						
Number of Slice flipflops:	12 out of 28800	0%	12 out of 28800	0%	12 out of 28800	0%
Number of 4 input LUTs:	40 out of 28800	0%	41 out of 28800	0%	43 out of 28800	0%
Logic Distribution:						
Number of occupied slices:	22 out of 28800	0%	23 out of 2880	0%	26 out of 28800	
Number of slices with related logic:	20 out of 42	45%	21 out of 44	47%	24 out of 48	50%
Number of slices with related logic:	20 out of 42	45%	21 out of 44	47%	24 out of 48	50%
Total number of 4 input LUTs:	42		44		48	
Number with an unused Flip Flop:	21 out of 43	45%	21 out of 44	47%	24 out of 48	50%
Number with an unused LUT:	0 out of 43	0%	0 out of 44	0%	0 out of 48	0%
Number of fully used LUT-FF pairs:	22 out of 43	54%	23 out of 44	52%	24 out of 48	
IO Utilization:						
Number of IOs:	11		12		13	
Number of bonded IOBs:	11 out of 220	5%	12 out of 220	5%	13 out of 220	5%
Specific Feature Utilization:						
Number of BUFG/BUFGCTRLs:	1 out of 32	3%	1 out of 32	3%	1 out of 32	3%
Timing Summary:						
Minimum period:	1.802ns		1.802ns		1.802ns	
Maximum Frequency:	555.001MHz		555.001MHz		555.001MHz	
Minimum input arrival time before clock:	1.630ns		1.641ns		2.164ns	
Maximum output required time after clock:	3.758ns		3.758ns		3.758ns	

Table I. Design implementation summary of binary, ternary and Quinquenary coding techniques

6.7. Comparison with Previous Result for generation 6-psk pulse compression sequences

SYNTHESIS PARAMETER	6-PSK GENERATION LITERATURE MODEL[6]	6-PSK GENERATION PROPOSEDMODEL
Number of 4 input LUTs	237	48
Number of occupied Slices	119	25
Number of bonded IOBs	334	13
Total equivalent gate count for design	1,446	302
Minimum input arrival time before clock	2.917ns	2.164ns
Maximum output required time after clock	8.991ns	3.758ns

Table II. Comparison of 6-psk generation results b/w proposed and literature model

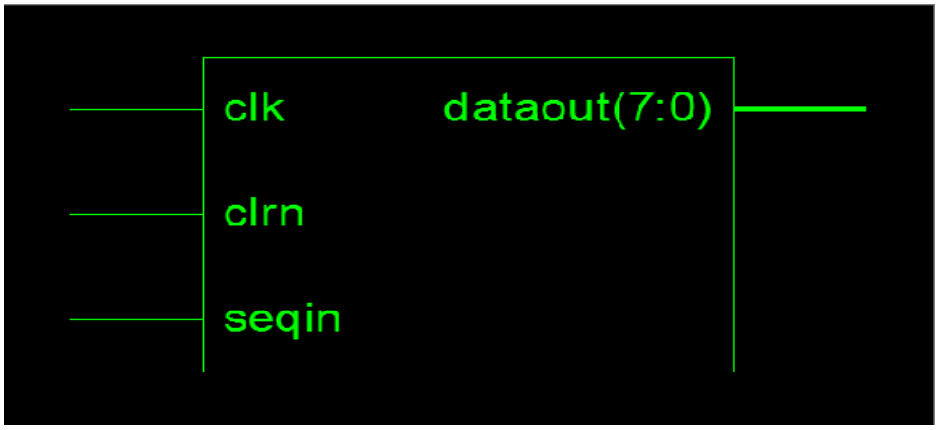

Figure.8. (A) RTL Schematic of the Top module for the proposed architecture

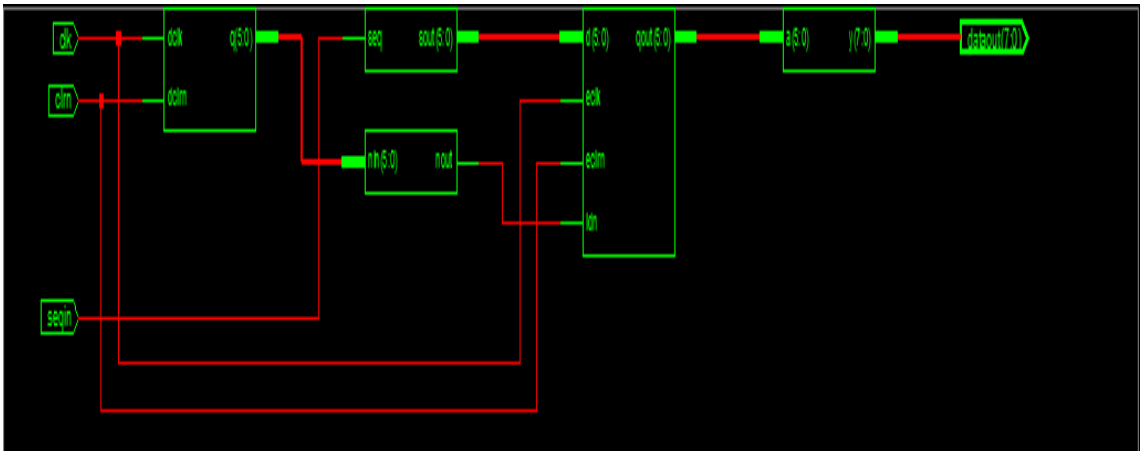

Figure.8. (B) RTL Schematic of the Top module for the proposed architecture

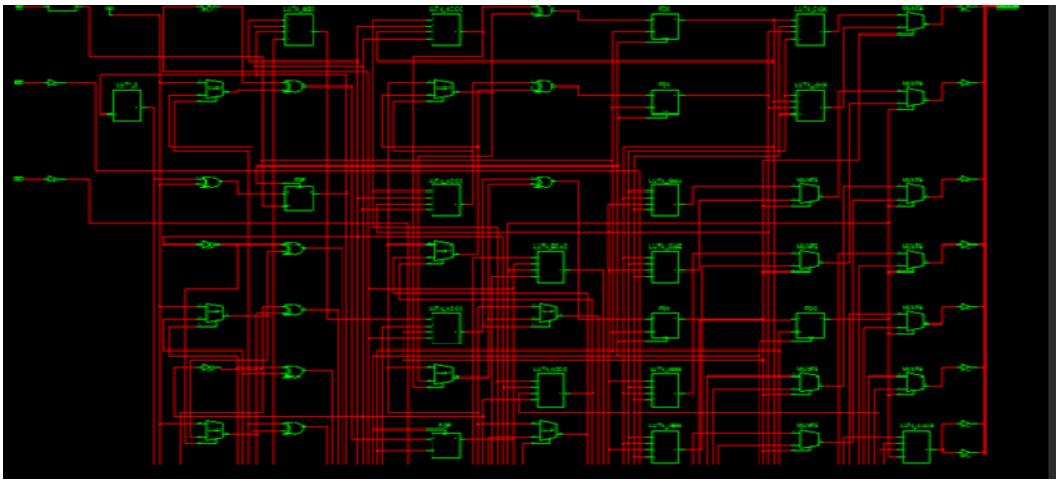

Figure.9.Technological schematic of Top Module Circuit

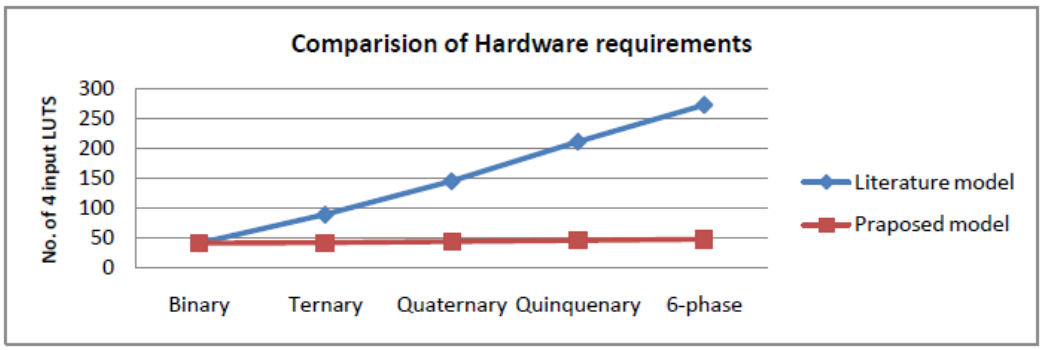

Fig.10. Comparison of the hardware requirements for implementation of literature and proposed model

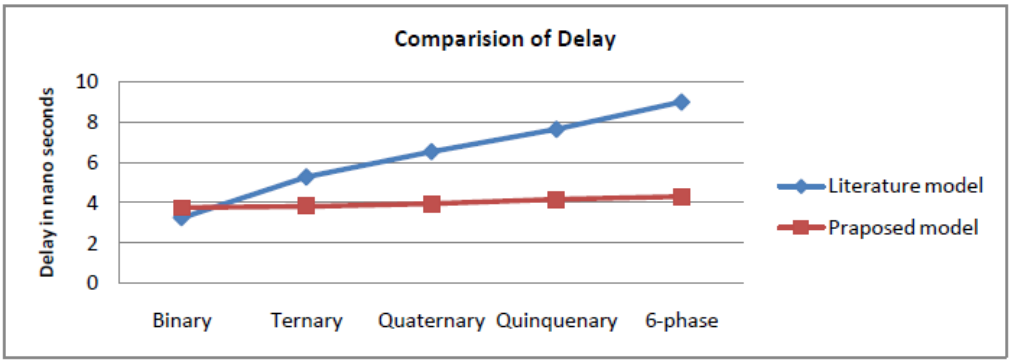

Fig.11. Comparison of Maximum output required time after clock for the literature and proposed model

The RTL and technology Schematics for the proposed architecture are shown in the figure 8 and figure 9.Table I. shows the Design implementation summary of binary, ternary, quaternary and six phase coding techniques. We can see in the table that the number of look up tables and slices required are almost equal for all the pulse compression techniques .Minimum input arrival time before clock and Maximum output required time after clock are also almost equal.Table II. Shows the Comparison of 6-psk generation results b/w proposed and literature model, the table shows that the number of look up tables required for the proposed model is 48, whereas for the literature model[7] it is 237. We can also see an improvement of speed and delay with the pro-posed model compared to the literature model [7]. Hence the proposed model is superior than the model described in literature model [7].

The graph in figure 8 infers the information regarding the number of look up tables used for the proposed model and the literature models.The number of LUTS required is increasing al-most in a linear fashion for the literature models whereas it is constant for the proposed design. Hence the hardware size is reduced for the proposed model. The graph in figure 9 infers the in-formation regarding Maximum output required time after clock for the literature and proposed model. The delay increasing almost in a linear fashion for the literature models whereas it is constant for the proposed design, hence the delay is reduced for the proposed model.

7. CONCLUSION

The proposed architecture shown in figure 1 has been authored in VHDL for Pulse compression sequences and its synthesis was done with Xilinx XST. Xilinx ISE Foundation 10.1 has been used for performing, mapping, placing and routing, for Behavioral simulation modelsim6.0 has been used. The synthesis tool was configured to optimize for area and high effort considerations. The targeted device was Spartan-3 xa3s1500fgg676-4 with detailed specifications at [29].An efficient VLSI architecture for gene-rating the pulse compression codes is proposed and implemented for the design of Binary, ternary, Quadrature and 6-Phase pulse compression sequences. The proposed architecture is a real-time signal processing solution to generate the radar pulse compression sequences like binary, ternary, quaternary, Quinquenary and six phase codes. It has been seen that the proposed VLSI Architecture has occupied less area with minimum signal propagation delay and thus can be used in radar and communication areas. Hence the proposed architecture is superior and efficient while compared to previous architectures mentioned in the literature. The same paper can be implemented with direct digital frequency synthesizer through which resolution of the sine wave can be increased without increasing the area of the design.

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