Reducing power in using different technologies using FSM architecture

Himani Mitta[1], Dinesh Chandra[2], Sampath Kumar[3]

[1,2,3]J.S.S.Academy of Technical Education ,NOIDA,U.P,INDIA
himanimit@yahoo.co.in, dinesshc@gmail.com , sampath_sams@yahoo.com

Abstract:

As in today's date fuel consumption is important in everything from scooters to oil tankers, power consumption is a key parameter in most electronics applications. The most obvious applications for which power consumption is critical are battery-powered applications, such as home thermostats and security systems, in which the battery must last for years. Low power also leads to smaller power supplies, less expensive batteries, and enables products to be powered by signal lines (such as fire alarm wires) lowering the cost of the end-product. As a result, low power consumption has become a key parameter of microcontroller designs . The purpose of this paper is to summarize, mainly by way of examples,what in our experience are the most trustful approaches to lowpower design. In other words, our contribution should not be intended as an exhaustive survey of the existing literature on low-power esign; rather, we would like to provide insights a designer can rely upon when power consumption is a critical constraint.We will focus on the reduction of power consumption on different technologies for different values of oicapacitance and also compare power saving in technologies.

Keywords:

FSM Decomposition [2] ,Mealy and Moore Machines , Capacitance[5], Power saving

1. Introduction

Methods of low power realization of FSMs are of great interest since FSMs are important components of digital systems and power is a design constraint.Power dissipated by FSMs can be controlled by the way the codes are assigned to the states of an FSM.Such attempts are reported in [4] and [6]. In [4], the weighted graph is constructed depending upon the steady state probability distribution, where the states are nodes. A high weight on an edge between a pair of nodes implies that they should be given codes with less Hamming distance, since there is a high probability of transition among them. In [6], a heuristic !- Silicon Automation Systems, India. algorithm is given to embed the state transition graph (STG) in a hypercube such that minimum number of flip-flops will be switched whenever there is a state transition. Recently, attempts using decomposition for low power realization of FSMs were also reported [1,2, 3]. In [2, 3], an STG is partitioned into several pieces, each piece being implemented as a separatemachine with a wait state. In this case, only one of the sub-machines is active and other sub-machines are in the reset state. In CMOS circuits, power is dissipated in a gate when the gate output changes from 0

DOI : 10.5121/vlsic.2011.2320

to 1 or from 1 to 0. Minimization of power dissipation can be considered at algorithmic, architectural, logic, and circuit levels. In sequential circuit design, an effective approach to reduce power dissipation is to "turn off" portions of the circuit, and hence reduce the switching activities in the circuit. In this article we propose a technique that is also based on selectively turning off portions of a circuit. Our approach is motivated by the observation that, for an FSM, active transitions occur only within a subset of states in a period of time. Therefore, if we synthesize an FSM in such a way that only the part of the circuit which computes the state transitions and outputs will be turned on while all other parts will be turned off, power consumption will be reduced. In a CMOS circuit, generally, the switching activity of the gate output contributes most to the total power dissipation. For FSM low power design, partitioning technique proves to be effective for reducing switching activity. That is, partition the original FSM into several smaller sub FSMs and only one of them is active at a time.

Designers should use components that deploy the latest developments in low-power technology. The most effective power savings can be achieved by making the right choices early on during the system and architectural level of abstraction. In addition to using power-conscious hardware design techniques, it is important to save power through careful design of the operating system and application programs.Objective of this paper is

(1) Computing the Power consumption in original FSM
(2) Compute value of Power for different technologies with frequency taken from FSM computation
(3) Take capacitance value for different technologies and from original computaion of FSM find power
(4) Plot graphs for Technologies vs Power .
(5) Plot graphs for Capacitor vs Power

1.2 Dissipation of Power

The sources of energy consumption on a CMOS chip can be classified as static and dynamic power dissipation. The dominant component of energy consumption in CMOS is dynamic power consumption caused by the actual effort of the circuit to switch. A first order approximation of the dynamic power consumption of CMOS circuitry is given by the formula[3]:

$$P = C * V^2 * f \qquad (1)$$

where P is the power, C is the effective switch capacitance, V is the supply voltage, and f is the frequency of operation. The power dissipation arises from the charging and discharging of the circuit node capacitances found on the output of every logic gate. Every low-to-high logic transition in a digital circuit incurs a change of voltage, drawing energy from the power supply.A designer at the technological and architectural level can try to minimize the variables in these equations to minimize the overall energy consumption. However, power minimization is often a complex process of trade-offs between speed, area, and power consumption.

Static energy consumption is caused by short circuit currents, bias, and leakage currents. During the transition on the input of a CMOS gate both p and n channel devices may conduct simultaneously, briefly establishing a short from the supply voltage to ground. While statically-biased gates are usually found in a few specialized circuits such as PLAs, their use has been dramatically reduced. Leakage current is becoming the dominant component of static energy

consumption. Until recently, it was seen as a secondary order effect; however, the total amount of static power consumption doubles with every new process node.

Energy consumption in CMOS circuitry is proportional to capacitance; therefore, a technique that can be used to reduce energy consumption is to minimize the capacitance. This can be achieved at the architectural level of design as well as at the logic and physical implementation level.Connections to external components, such as external memory, typically have much greater capacitance than connections to on-chip resources. As a result, accessing external memory can increase energy consumption. Consequently, a way to reduce capacitance is to reduce external accesses and optimize the system by using on-chip resources such as caches and registers. In addition, use of fewer external outputs and infrequent switching will result in dynamic power savings.

Routing capacitance is the main cause of the limitation in clock frequency. Circuits that are able to run faster can do so because of a lower routing capacitance. Consequently, they dissipate less power at a given clock frequency. So, energy reduction can be achieved by optimizing the clock frequency of the design, even if the resulting performance is far in excess of the requirements

1.3 Methods and Approaches

The key steps in our approach are:

(1) Finding the number of happening states then find the probability Of FSM.

(2) Take different technologies and its related value of voltage.

(3) Find the frequency by using the formula :

$$F = P(1-P)$$

(4) With calculations based on FSM find power savings in different technologies and compare them .

(5) With different value of capacitor find the power savings.

(6) An effective approach to reduce power dissipation is to “turn off” portions of the circuit, and hence reduces the switching activities in the circuit. We synthesize an FSM in such a way that only the part of the circuit which computes the state transitions and outputs will be turned on while all other parts will be turned off.

(7) In general, since the combinational circuit for each submachine is smaller than that for the original machine, power consumption in the decomposed machine will be smaller than that of the original machine

1.4 Basic Principles

Entropy is a measure of the randomness carried by a set of discrete events observed over time. In the studies of the information theory, a method to quantify the information content Ci of an event E_i in this manner is o take logarithmic of the event probability

$$C_i = \log_2 (1/P_i) \qquad (2)$$

Since $0 \leq P_i \leq 1$, the logarithmic term is non negative and we have $C_i > 0$.

The average information contents of the system is the weighted sum of the information content of C_i by its occurrence probability This is also called the entropy[4] of the system.

$$H(X) = \sum_{i=1}^{m-1} p_i \log_2 \frac{1}{p_i} \qquad (3)$$

1.5 Estimated Power

Entropy is a measure of the randomness carried by a set of discrete events observed over time. In the studies of the information theory, a method to quantify the information content Ci of an event E_i in this manner is o take logarithmic of the event probability

$$C_i = \log_2 (1/P_i)$$

Since $0 \leq P_i \leq 1$, the logarithmic term is non negative and we have $C_i > 0$.

The average information contents of the system is the weighted sum of the information content of C_i by its occurrence probability This is also called the entropy of the system.

1.6 Challenges In Physical Design

As technology is directly related to physical size , it is clear that as technology advances power also reduces but there are other constraints that come while designing it at nano level so care should be taken and optimized designing is the demand of the day. Since capacitance, a function of fan out, wire length, and transistor size , reducing capacitance means reducing it physically . But there are challenges in reducing it. The challenge of low-power physical design is to create, optimize, and verify the physical layout so that it meets the power budget along with traditional timing, SI, performance, and area goals. The design tool must find the best tradeoffs when implementing any number of low-power techniques.

While low-power design starts at the architectural level, the low-power design techniques continue through place and route. Physical design tools must interpret the power intent and implement the layout correctly, from placement of special cells to routing and optimization across power domains in the presence of multiple corners, modes, and power states, plus manufacturing variability. While many tools support the more common low-power techniques, such as clock

gating, designers run into difficulty with more advanced techniques, such as the use of multiple voltage domains, which cause the design size and complexity to explode

1.7 Reduction Approach

(1) For a particular technology take its power supply voltage
(2) Take different value of capacitance like 1µF , 0.5 µF , 0.25 µF , 0.1 µF.
(3) By using formula P= CV^2f calculate power dissipation in 180nm , 130nm , 90nm technologies
(4) Compare the results.

1.8 Results

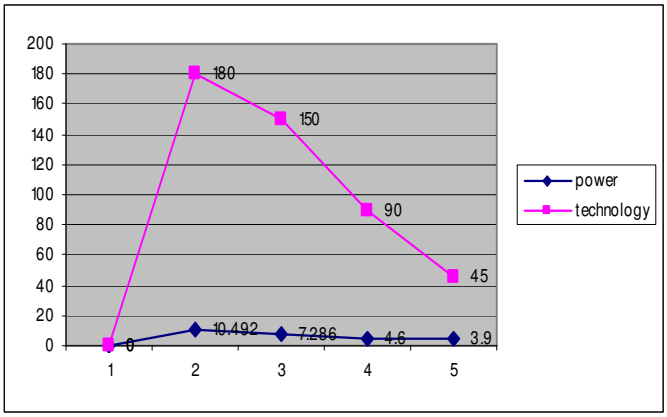

Fig. 1.1 Technology vs Power @ 15 µF

Keeping capacitor constant @ 15(µF) , it is clear from Fig. 1.1 that as technology grows power consumption reduces from 0.49 µW to 3.9 µW. Innovation in technology is being riven by the shrinking size which leads to reduction in capacitor values .

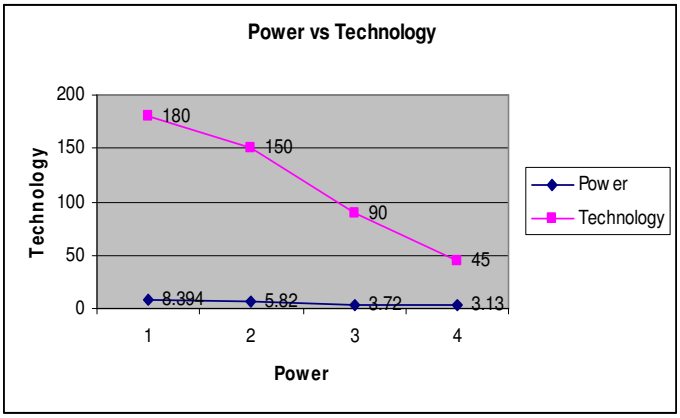

Fig. 1.2 Technology vs Power @ 12 µF

As observed in Fig. 1.1 ,in Fig. 1.2 also keeping capacitor @ 12 µF it is observed that power reduces as technology advances from 8.39 µW to 3.13 µW.

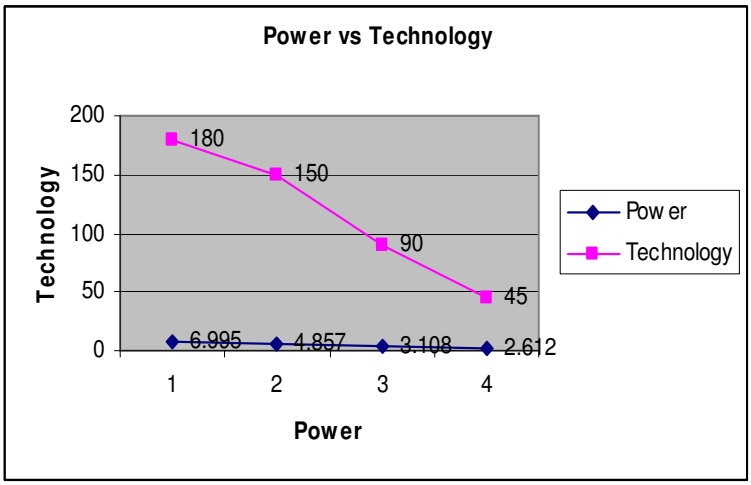

Fig. 1.3 Technology vs Power @ 10 µF

As we move on to advances technology we find that power reduces considerably . As shown in Fig. 1.3 it is shown that by keeping capacitor constant power reduces from 6.995 µW to 2.612 µW as technology grows

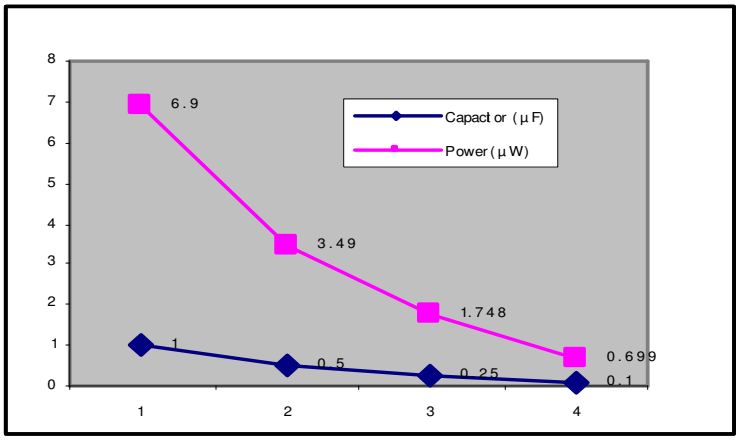

Fig. 2.1 Cap. vs Power in 180nm tech.

As shown in Fig. 2.1, as capacitor value reduces from 1 µF to 0.1 µF, po wer also get reduces from 0.2612 µW to 0.0261 µW. This is called switched capacitance reduction technique. But designer cannot reduce blindfoldly the value of capacitance as it worsens the performance but it should be according to technology library.

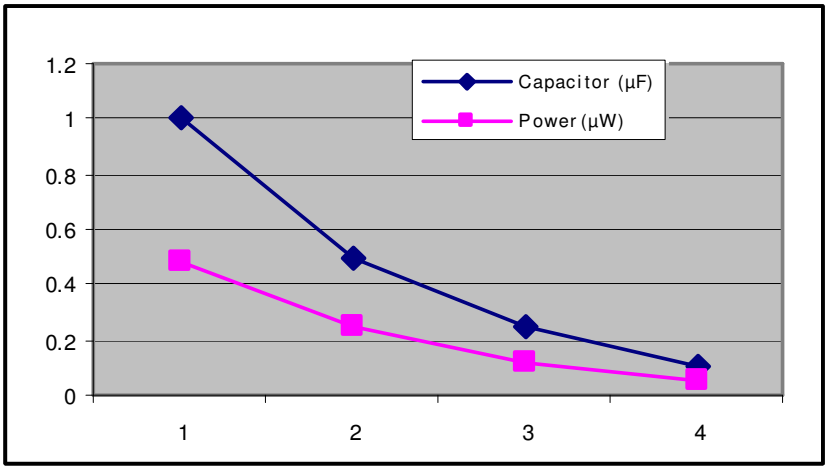

Fig. 2.2 Cap. vs Power in 130nm tech

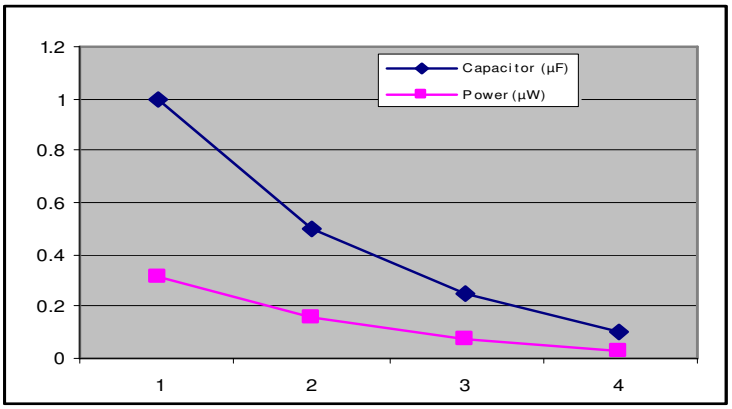

Fig. 2.3 Cap. vs Power in 90nm tech

Power(µW)	Technology(nm)
10.492	180
7.286	150
4.6	90
3.9	45

Table 1.1

Power	Technology
8.394	180
5.82	150
3.72	90
3.13	45

Table 1.2

Power	Technology
6.995	180
4.857	150
3.108	90
2.612	45

Table 1.3

VDD(V)	Frequency(hz)	Capacitor(µF)	Power(µW)
1.8	0.2159	1	6.9
1.8	0.2519	0.5	3.49
1.8	0.2519	0.25	1.748
1.8	0.2519	0.1	0.699

Table 2.1

1.9 Conclusion

saving with decrease in capacitor and with latest technology leads to more power saving . This is power in original FSM . I f we decompose machines in more sub machines then frequency reduces and we can get more reduction in powerThe Decomposed FSM[2] technique leads in a 34.13% average reduction in switching activity of the state variables, and 12% average reduction of the total switching activity of the implemented circuit. Although the solution is heuristic, and does not guarantee the minimum power consumption, these results leads to a reduction in the power consumption in the complete circuit.

References

[1]. Chow, S.-H., Ho, Y.-C., Hwang, T. and LIU, C.L. 1996. "Low power realization of finite state machines- a decomposition approach". ACM Trans, Des. Autom. Electron. Syst. 1,3, 315-340.

[2]. *L. Benini, A. Bogliolo, and G. De Micheli, "A survey of Design Techniques for System-Level Dynamic Power Management, " IEEE Trans . On VLSI Systems, Vol.8, No.3, pp, 299-316, June 2000.

[3]. *L. Benini, G. De Micheli, and E. macii, " Designing Low-Power Circuits : Practical Recipes, " IEEE Circuits and Systems magazine, pp7-25, Vol.1, No.1,2001.

[4]. L. Benini, G. De Michelli, "State assignment for Low Power," IEEE Trans. on Computer Aided Design , vol. 30 No. 3, March 1995, pp. 258-268

[5]. *Benini, L and G. De Micheli, 1995b. "Transformation and synthesis of FSM for low-power gated-clock implementation". IEEE trans. Computer.

[6]. S. J. Wang, M. D. Horng, "State assignment of finite state machine s for low power applications," ELECTRONICS LETTERS, 5th Dec.1996, Vol. 32.

[7]. Designing Low-Power Circuits:Practical Recipes by Luca Benini *Giovanni De MicheliEnrico Macii .