Design of Reversible Sequential Circuit Using Reversible Logic Synthesis

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Abstract

Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. In this paper, we have proposed a new reversible gate. And we have designed RS flip flop and D flip flop by using our proposed gate and Peres gate. The proposed designs are better than the existing proposed ones in terms of number of reversible gates and garbage outputs. So, this realization is more efficient and less costly than other realizations.

Keywords

Reversible logic, Reversible gate, Power dissipation, Flip-Flop, Garbage, BME gate.

1. Introduction

Energy dissipation is an important consideration in VLSI design. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation[1].This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates [2].Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Reversible circuits are also interesting because the loss of bits of information implies energy loss [2]. Younis and Knight [3] showed that some reversible circuits can be made asymptotically energy-lossless if their delay is allowed to be arbitrarily large. However, reversible logic is suffering from two problems. Firstly, there is a lack of technologies with which to build reversible gates. Work is certainly continuing in this area. Secondly, while there is much research into how to design combinational circuits

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using reversible logic, there is little in the area of sequential reversible logic implementations. There is no limitation inherent to reversible logic preventing the design of sequential circuits; in fact when Tommaso Toffoli first characterized reversible logic in his 1980 work Reversible Computing [4] he stated that "Using invertible logic gates, it is ideally possible to build a sequential computer with zero internal power dissipation. "To establish the relevance of reversible and quantum computing it seems appropriate to note that the VLSI industry is moving at high speed towards miniaturization. With miniaturization it faces two issues: i) A considerable amount of energy gets dissipated in VLSI circuits and ii) the size of the transistors are approaching the quantum limits where tunneling and other quantum phenomena are likely to appear. Thus, we need a superior technology that can circumvent these problems.

This paper presents a new 4*4 reversible logic gate that is BME gate. BME gate is a universal in the sense that it can be used to synthesize any arbitrary Boolean function. It is shown that a RS and D Flip-Flop can be realized using proposed reversible logic gate and Peres gate. The presented design reduces the number of gates and the number of garbage outputs.

2. Reversible Logic Synthesis and Others

Definition 2.1

A circuit is reversible if it maps each input vector into a unique output vector and vice versa.

Definition 2.2

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs [5], [10] and [12].

Example 2.1. Let the input vector be I_v, output vector O_v and they are defined as follows, $I_v = (I_i, I_{i+1}, I_{i+2} \ldots I_{k-1}, I_{k)}$ and $O_v = (O_i, O_{i+1}, O_{i+2} \ldots O_{k-1}, O_k)$. For each particular i, there exits the relationship $I_v \leftrightarrow O_v$ [10].

A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [6], [7], [8] and [11].

Definition 2.3

Garbage output refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function [12].

Definition 2.4

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [19]. So, the quantum cost of a 2*2 Feynman gate is 1. Again, the quantum cost of a 3*3 Toffoli, Fredkin, Peres and New gate is 5, 5, 4 and 11 respectively [20][21][22].

Definition 2.5

Flexibility refers to the universality of a reversible logic gate in realizing more functions [12].

Definition 2.6

Gate Level refers to the number of levels in the circuit which are required to realize the given logic functions [12].

Definition 2.7

Hardware Complexity refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit [9] and [12].

3. Major Several Reversible Logic

3.1 Feynman Gate

It is a 2*2 Feynman gate [13]. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Figure 1 shows a 2*2 Feynman gate.

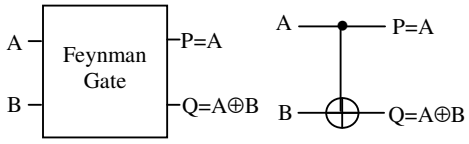

Figure 1: Feynman gate

3.2 Double Feynman Gate (F2G)

It is a 3*3 Double Feynman gate [14].The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

Figure 2 shows a 3*3 Double Feynman gate.

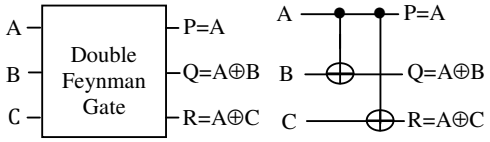

Figure 2: Double Feynman gate

3.3 Toffoli Gate

It is a 3*3 Toffoli gate [6] The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5. Figure 3 shows a 3*3 Toffoli gate.

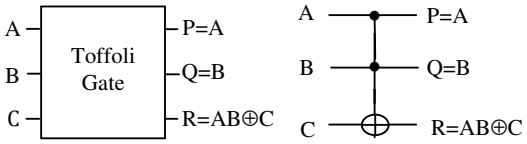

Figure 3: Toffoli gate

3.4 Fredkin Gate

It is a 3*3 Fredkin gate [7]. The input vector is I (A, B, C) and the output vector is O(P, Q, R). The output is defined by P=A, Q= $\bar{A}$B⊕AC and R= $\bar{A}$C⊕AB. Quantum cost of a Fredkin gate is 5. Figure 4 shows a 3*3 Fredkin gate.

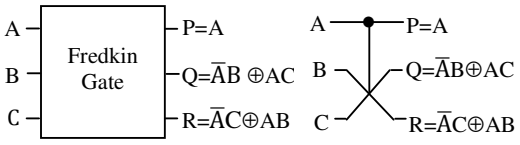

Figure 4: Fredkin gate

3.5 Peres Gate

It is a 3*3 Peres gate [15]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. Figure 5 shows a 3*3 Peres gate.

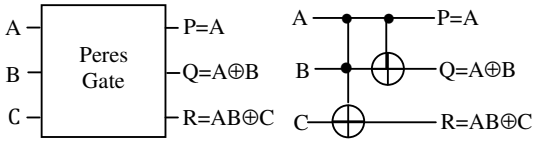

Figure 5: Peres gates

3.6 Double Peres gate

It is a 4*4 Double Peres Gate [16]. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The output is defined by P=A,Q=A⊕B,R=A⊕B⊕D and S=(A⊕B)D⊕AB⊕C.
Figure 6 shows a 4*4 Double Peres gate.

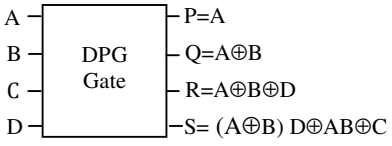

Figure 6: DPG gate

4. Related Work

4.1 RS Flip-Flop Designs

Thapliyal [18] proposed reversible clocked *RS* Flip-Flop which is a direct realization of conventional irreversible circuit realized. His design is costly because it incorporated two New gates whose quantum cost is higher than other reversible gates which is mentioned at Section 2 in Definition 2.4. Moreover, the design contained a single fan-out which is forbidden in strict reversible sense [23].Ashis [17] proposed design perform NAND operations using a single 3*3 Peres gate instead of using Fredkin gate, his design less costly reversible $\overline{RS}$ Flip-Flop using the Peres gate.Since the design of Thapliyal [18] consists of two New gates and the quantum cost of each New gate is 11, so the overall design cost increased. Moreover Ashis [17] realization contained two redundant Feynman gates. But Ashis [17] design is less costly in terms of number of gates, garbage bits and quantum costs than Thapliyal [18] design.

4.2 D Flip-Flop Designs

Thapliyal [18] proposed a reversible clocked *D* Flip-Flop that is also costly because it contained four New gates. Moreover a fanout can be seen in the design. Ashis [17] proposed design of reversible clocked *D* Flip-Flop employs the proposed $\overline{RS}$ latch. The clocked *D* Flip-Flop is efficient to use in designing reversible memory circuits because of its superiority over the existing one [18] in terms of number of gates, garbage bits and quantum cost.

5. Proposed Reversible Logic Gate

We have proposed a new 4*4 reversible logic gate named BME gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The output is defined by P=A, Q=AB⊕C, R=AD⊕C and S= $\bar{A}$B⊕C⊕D. The block diagram of BME gate is shown in Figure 7.

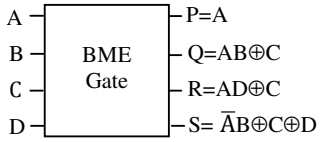

Figure 7: Block diagram of a new reversible BME gate

Table 1: Truth Table of New Reversible BME Gate

A	B	C	D	A	AB⊕C	AD⊕C	$\bar{A}$B⊕C⊕D
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	1

1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	0	0

We can verify our BME gate by the truth table that the output and input vectors have one to one mapping between them which satisfies the condition of reversibility of a gate. We can see that from Table 1 that the 16 different input and output vectors are unique means they have one to one mapping between them. So, BME gate satisfies the condition of reversibility.

6. Proposed Design of Reversible RS Flip-Flop

The RS Flip-Flop can be mapped with one BME and two Peres gate. The BME gate needs E, S, 1 and R inputs respectively in 1st, 2nd, 3rd and 4th input. The output $\overline{E.S}$ and $\overline{E.R}$ are realized by one BME in the 2nd and 3rd outputs. Now, the 2nd output of $\overline{E.S}$ that is $\bar{S}$ can be used as 2nd input of one Peres gate. The 3rd output of $\overline{E.R}$ that is $\bar{R}$ can be used as 2nd input of another Peres gate. Thus, our design needs only 3 reversible logic gates with 4 garbage outputs to design of RS Flip-Flip. The proposed design of RS Flip-Flip is shown in Figure 8.

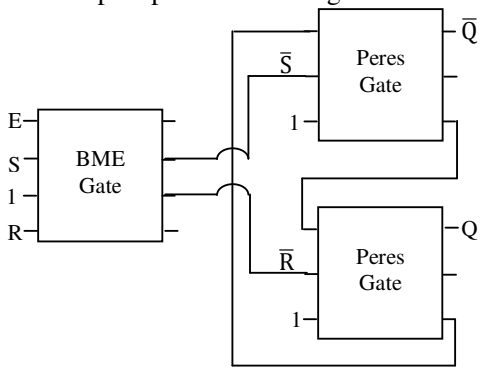

Figure 8: Proposed RS Flip-Flop

6.1. Evaluation of Proposed RS Flip-Flop

Table 2: Comparison of Different RS Flip-Flop

	No of gates	**No of garbage outputs**
Proposed design	3	4
Existing design [17]	5	6
Existing design [18]	6	8

From Table 2 we can see that the design is better than the design [17] and [18].Here, we need only 3 gates and 4 garbage outputs. So, the design is optimized than the design of [17] and [18] in terms of no of gates and garbage outputs.

7. Proposed Design of Reversible D Flip-Flop Using Proposed RS Flip-Flop

The D Flip-Flop can be mapped with one BME and two Peres gate. The BME gate needs D, CLK, 1 and 0 inputs respectively in 1st, 2nd, 3rd and 4th input. The output $\overline{D.CLK}$ and $\overline{\overline{D}.CLK}$ are realized by one BME in the 2nd and 4th outputs. Now, the 2nd output $\overline{D.CLK}$ that is $\bar{S}$ can be used as 2nd input of one Peres gate. The 4th output $\overline{\overline{D}.CLK}$ that is $\bar{R}$ can be used as 2nd input of another Peres gate. Thus, our design needs only 3 reversible logic gates with 4 garbage outputs to design of RS Flip-Flip. The proposed design of D Flip-Flip is shown in Figure 9.

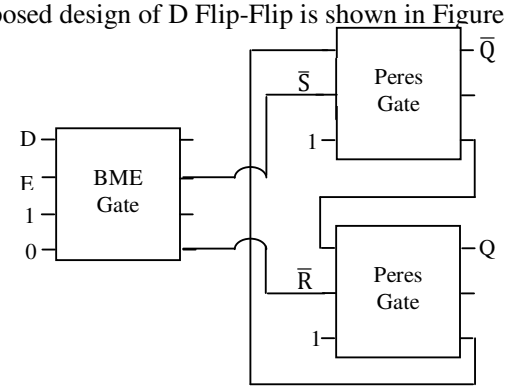

Figure 9: Proposed reversible clocked D Flip-Flop using Proposed RS Flip-Flop

7.1. Evaluation of Proposed design of D Flip-Flop using Proposed RS Flip-Flop

Table 3: Comparison of Different D Flip-Flop

	No of gates	No of garbage outputs
Proposed design	3	4
Existing design [17]	5	5
Existing design [18]	7	8

From Table 3 we can see that the design is better than the design [17] and [18].Here, we need only 3 gates and 4 garbage output. So, the design is optimized than the design of [17] and [18] in terms of no of gates and garbage outputs.

8. Conclusions

The proposed reversible design is utilized for efficiently designing RS and D Flip-Flop. As, Flip-Flips are most important memory elements and used in several circuits like RAM, Logic Blocks of FPGA. We have seen by comparing the existing design with our proposed design that the proposed design is less costly in terms of number of gates and number of garbage outputs. The proposed design is highly optimized. So, this proposed gate can contribute significantly in the reversible logic community. Thus, the resulting reversible sequential circuits are more cost competent.

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