A Novel Approach To Minimize Spare Cell Leakage Power Consumption During Physical Design Implementation

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ABSTRACT

In IC designs leakage power constitutes significant amount power dissipation because CMOS gates are not perfect switches. The leakage power in CMOS gates is dependent on the states of the inputs. This leakage power will get dissipated even when the gates are in idle conditions. Traditionally ECO cells (or) spare cells remain idle in the design and thus contributes to significant state dependent leakage power consumption. In this paper we proposed novel solution to minimize the state dependent leakage power dissipation of the spare cells.

KEYWORDS

Engineering Change Order (ECO), ECO cell, Spare cell, State dependent, leakage power and switching probability.

1. INTRODUCTION

Power minimization in VLSI designs is a major challenge now to get the best performance out of the devices. IC's used to make mobile or portable devices like cell phones or wireless devices which operate on battery, need special attention to minimize the power consumption. Leakage power consumption will happen in CMOS gates even when the circuit is idle as transistors are not perfect switches. There are four main sources of leakage currents in a CMOS gate (Fig 1) [1]

- Sub-threshold Leakage (ISUB): the current which flows from the drain to the source current of a transistor operating in the weak inversion region.

- Gate Leakage (IGATE): the current which flows directly from the gate through the oxide to the substrate due to gate oxide tunneling and hot carrier injection.

- Gate Induced Drain Leakage (IGIDL): the current which flows from the drain to the substrate induced by a high field effect in the MOSFET drain caused by a high VDG.

- Reverse Bias Junction Leakage (IREV): caused by minority carrier drift and generation of electron/hole pairs in the depletion regions.

As technologies scale down, percentage of leakage power to total power is gradually going up with every node. Leak-age is an unwanted by-product and substantially reduces the operational time of the devices thereby rendering such devices uncompetitive. It is, therefore, absolutely necessary to eliminate leakage, wherever it is possible [2]. In this paper we are focusing on leakage elimination in spare cells. Spare cells are redundant cells distributed in the design as back-up cells to implement any ECOs that may be required in the design, at a later stage. Spare cells do not play any active role in the IC operation. While spare cells are used to carry out certain functions, they are not connected to the normally functioning electronic components according to the original circuit design of the IC. Some of the spare cells can be selectively connected to the normally functioning electronic components, during revising or rerouting process of IC. This process is often referred to as an ECO, and the spare cells can be alternatively referred to as ECO cells.
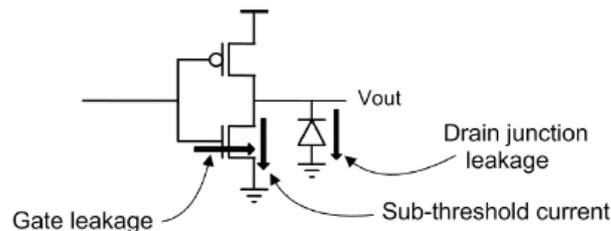
Figure.1 Leakage Currents [1]

1.1 Prior Work

To the best of author's knowledge there is not much published literature on spare cells leakage reduction. However Anubhav Srivastava et al [2] proposed a spare cell architecture for leakage power reduction in power criti-cal System on Chips .The spare cell has a disconnect between the cell structure and the power rail. The cell is connected with the power or ground supplies by using metal layer only which is programmable depending upon the availability. This approach involves making the source connection of the spare cell transistors to power / ground supplies, programmable through only a metal connector. This means that the spare cells are disconnected from supply rails in the first revision of the design and hence do not contribute to the leakage power. This is done by creating a metal open between the transistor source and the supply rails in all spare cells. In any subsequent revision of the IC, whichever spare cells are required to be utilized for implementing any functional changes (ECOs), only those specific cells are connected to the supply rails and others still remain disconnected, as is. But this approach needs maintaining a separate spare cell library and is not suitable for re-spin designs. On the other hand Hou et al [3] in their patent they came up with a dual rail architecture for spare cells which are complement to each other. The spare cells will be connected to one of these rails and will be rerouted to main functional rail during ECO operation. But as this approach needs additional rail it results in additional masks cost.

1.2 Our Contribution

The CMOS gates leakage power consumption would depend on the different states taken by the inputs of the gates [4]. This is referred as state dependent leakage power consumption of the CMOS gates. For a gate which has "n" inputs, there can be 2^n states for which the leakage power consumption is found using the simulation models of the circuit and is stored in a format which can be used by the EDA tools to estimate the state dependent leakage power of those gates. Every cell would contribute to the state dependent leakage power including the spare cells in the design. So by taking the advantage of state dependent leakage tables from timing models we proposed a novel spare cell input connections which results in low power.

This paper is organized in to six different sections. Section 2 discusses about Engineering Change Order (ECO), Spare Cells and their power consumption details. In Section 3 we describe the way state dependent leakage power is calculated for a cell given the state dependent leakage power model available for it. Section 4 describes the generalized dependency of the leakage power consumption of the Spare cells on the states of the inputs of the cell. Also it describes the proposed algorithm for connecting the inputs of the Spare cells to get the least state dependent leakage power consumption. Section 5 describes the results in a comparative tabular format between the proposed flow and the traditional flow run on different designs with varied Spare cell numbers. Section 6 concludes the paper.

2. PROBLEM DESCRIPTION AND MOTIVATION

2.1. Engineering Change Order (ECO) [2]

An engineering change order is the functional/non-functional change which comes as an implementation requirement when the IC is already in execution phase or it has completed the execution phase. Functional changes which we refer here are usually the RTL bugs which were caught after the logical synthesis of the design by the verification and silicon validation teams or some late feature requirement by the customer/marketing team. Once a bug is identified it is fixed in RTL and after verification for the corrected functionality the new RTL is sent to the Back-End team for the implementation of change in GDS. This requires addition/deletion of the standard cells / nets for the logical implementation of changed logic. Once an ECO is logically implemented, the design is eco-placed and eco-routed i.e. incrementally placed and routed for the changed logic only. Non-functional changes which we refer here can be of three types

   i.   Buffer addition / deletion due as timing fixes: - These are the setup/hold timing fixes which come due to the change in constraints which was missed in earlier constraint generation.

   ii.   Restructuring of the glitchy logic: - These types of issues are usually caught in gate level simulations where logic is optimized in such a way that a glitch is getting propagated across the design and causing the functionality failure. For example: - While optimization if one signal and its inverted signal are connected as two inputs to an and gate the structure becomes inherently glitchy.

   iii.   GDS change for the hard macros: - These are the leakage or latch-up etc. type of fixes which do not impact the functionality of the macro but enhances its performance

There can be two implementation stages of an Engineering Change Order in Back-End database.

2.1.1.Pre-Mask ECOs

These are changes which come before the Tape-Out of the chip or before the mask preparations of the chip. In this the implementation team has flexibility of addition/deletion of standard cells while doing the change. These changes are first implemented logically with any type or number of standard cells and then these cells are placed and routed incrementally as part of physical implementation. Pre-mask ECOs do not impact the mask cost for the SoC as all the masks are prepared after database is sent to Fab.

2.1.2.Post-Mask ECOs

The post-mask ECOs are the changes which are required to be done when the SoC is fabricated and issues are caught during its post silicon validation or there comes a very late design change request. These changes directly impact the mask cost for the SoC as all the masks for different layers are already prepared any new change will require re-generation of that mask. These layers are broadly classified in two types metal layers (like M1 , M2 , M3 etc other horizontal and Metal layers above the base layers) and base layers (like Poly , substrate etc.) . The important point here is that the mask generation cost for the base layers is multiple times the mask generation cost for the metal layers. Addition / Deletion or movement of any standard cell requires the base layer change hence any of such activity is avoided while the implementation of a post-mask ECO. The other challenge which comes with a post-mask ECO is the implementation of the change in minimum number of metal layers so that cost of an additional mask can be saved. Since the addition or deletion of the standard cells is prohibited while the post ECOs some extra / unused standard cells are added in the design for this purpose known as Spare-Cells.

2.2. Spare Cells

Spare cells are the dummy cells or extra cells which are added in design in order to take care of post-mask ECOs. We should not leave inputs of the spare cells floating, because the problem with floating or unused CMOS inputs as a general rule is that gradual charging of the gate input capacitance may cause the following:

i.   There may be a static current flowing through the input stage, causing unnecessary excessive power dissipation.

ii. When the input voltage reaches the threshold level, the device may start high frequency oscillations causing heat generation that may eventually damage the part.

Therefore, as a standard solution, all unused (open or floating) inputs are simply connected to GND or VCC to prevent these adverse effects. But this method of always tying inputs of spare cells to GND or VCC will not ensure less leakage as the leakage power is also dependent on state of the inputs.

2.3. Power Consumption of Spare Cells and motivation for improvement

To enable Post-Mask ECOs, spare cells, which are standard cells not connected to any circuit, are often evenly placed on the chip layout; the type and number of spare cells vary from different chip designs and are usually determined by designers empirically. It is desirable to sprinkle more spare cells for metal-only ECO; however, more spare cells not only occupy more chip areas but also consume more leakage power [5].

The spare cells occupy approximately five to ten percent of the total cell count in a typical IC. Spare cells which are introduced in the design to achieve late functional changes in the design would usually have their inputs tied to ground to avoid ground bounce and unnecessary power dissipation. As a result a significant amount of power would leak through these spare cells. For example, the spare cells typically account for approximately to fifteen percent of leakage power of an IC manufactured using 90nm semiconductor processing technology [6].

This leakage power issue becomes more severe when the semiconductor processing technology advances and IC continues to shrink in size. The irony is that though some spare cells may eventually get used in the later revisions and become part of the design logic, yet, the number of un-used spare cells 6 Programmable Spare Cells For Leakage Reduction that remain, as is, in designs, is quite high {99.2% of spare cells were left unused in Andorra metal revision} [2]. This huge number is a big contributor to leakage power. The cells, though not part of the logic, are continuously leaking power and continue to do so throughout the life time of the IC. This is a huge overhead and needs to be eliminated.

Till now there are have been some techniques developed to reduce leakage in the circuit level, like programmable spare cells which will separate power rail from cell structure proposed by Anubhav Srivastava et al [2] and spare cell with two power supply rails proposed by Hou et al [3]. The main drawbacks in using these approaches is altering design cells layout (or) creating new library. This method is not flexible for re-spin designs. Engineering change order (ECO) due to frequency push and design/market requirement change is very important for producing high-end and high-volume main stream products in the semiconductor industry. It is a highly constrained design optimization based on an existing design with tight design scheduling due to time-to-market consideration [5]. So there is a need for a different approach with minimum changes to existing design flows to address this need for time to market. In the proposed approach we demonstrated the use of existing state dependent leakage numbers form .lib (Synopsys liberty format) and tying the spare cells inputs to the condition which gives minimum state dependent leakage during physical implementation stage to achieve low spare cell leakage numbers.

3. STATE DEPENDENT LEAKAGE POWER

Leakage power which is usually a constant contributor to the power consumption of the cell comes from the reverse biased PN junction diodes and the sub-threshold leakage from the source to the drain. The value is decided from the modelling of the devices. Usually the value is constant but it can be state-dependent, too [7].

Following is an example of how state dependent leakage power values are specified in the .lib file:

cell_leakage_power : 4953.7;
leakage_power(){
value : 8.52e+10;
*when : "!IO*RES+IO*!RES";*
}
leakage_power(){
value : 4953.45;
when : "!IO!RES+IO*RES";*
}

Here the default value is defined by the "cell_leakage_power" statement which is 4953.7 power units. The "leakage_power" statement defines the different leakage power groups for the same

cell. There power groups are state dependent and are controlled by the Boolean statement associated with the "when" statement.

The EDA tools will calculate the total leakage power consumption using above power models. In the above power model example there are two "when" conditions; each "when" condition will be evaluated and multiplied with its probability. (Here the probability refers to the chances that the net "IO" and "RES" would be in such a state that the Boolean condition is satisfied). So the total leakage power would be the summation of all these "when" conditions multiplied with their probability.

Here the total leakage power would be like [7]:

$$Pr(when_1)*Val_1 + Pr(when_2)*Val_2 + [1 - Pr(when_1) - Pr(when_2)]*Total\_Val \qquad (1)$$

Where
$$Val_1 = 8.52e+10$$
$$Val_2 = 4953.45,$$
$$Total\_Val = 4953.7.$$

Pr ($when_1$): Indicates the probability that the first condition will occur (that is, "!IO*RES+IO*!RES" will be true).

Pr ($when_2$): Indicates the probability that the second condition will occur (that is, "!IO*RES+IO*RES" will be true).

For calculating the probability, the following formulas are used:

$$Pr (A + B) = 1 - Pr(A) * Pr (B) \qquad\qquad (2)$$
$$Pr (AB) = Pr(A) * Pr(B) \qquad\qquad (3)$$

So for the first condition:

$$Pr(!IO*RES+IO*!RES) = 1 - Pr (!IO * RES) * Pr (IO * !RES) = 1 - [Pr (!IO) * Pr (RES) * Pr(IO) * Pr (!RES)] \qquad (4)$$

Similarly for the second condition:

$$Pr (!IO*RES+IO*RES) = 1 - [Pr (!IO) * Pr(RES) * Pr(IO) * Pr(RES)] \qquad (5)$$

The signal probability values (Pr(IO), Pr(RES), and so on) will be obtained from the net switching activity file provided as the input to the tool. The default signal probability that is taken by the tool for this calculation is 50%.

General formula for calculation of state dependent leakage power:

$$Pr(when_1)*Val_1 + Pr(when_2)*Val_2 + \ldots Pr(when_2{}^n)*Val_2{}^n +[1-Pr(when_1)-Pr(when_2)-\ldots Pr(when_2{}^n)]*Total\_Val \qquad\qquad (6)$$

Where "n" stands for the no of inputs of the gate and

$$Total\_Val = Val_1+Val_2+\ldots+Val_2{}^n \qquad\qquad (7)$$

4. PROPOSED FLOW FOR LEAKAGE MINIMIZATION OF SPARE CELLS

Spare cells insertion is a well known technique to reduce the cost of functional fixes, limiting the changes to a few metal masks. Common practice is to tie to ground input spare cell's pins, re-connecting them later in the flow, as required by the functional ECOs.

For illustration let's take an example of an AND gate spare master which has 2 inputs A1 and A2. This gate can have 4 different combinations of the A1 and A2 and hence four different state dependent leakage power values .If the state dependent leakage power table of this AND gate would be summarized as shown in Table 1 below:

Table 1. State Dependent Leakage Power for 2-input AND gate

When Condition/State of Inputs	Leakage Value
C_1 (A1. A2)	V_1
C_2 (A1!. A2)	V_2
C_3 (A1. A2!)	V_3
C_4 (A1!. A2!)	V_4

Where C_1, C_2, C_3 and C_4 represent the 4 different input combinations that the AND gate's inputs A1and A2 can take. So if the A1 and A2 inputs of the AND gate are tied to ground as per the traditional flow then the state dependent condition C_4 would be evaluated to be true and the leakage value would be V_4 as per the table as the probability of occurrence of other conditions C_1, C2 and C_3 is zero. So this can be described as with reference to equation (6):

P_{sdlp} *of AND gate == Pr(whenC$_1$)*V$_1$ + Pr(when C$_2$)*V$_2$+Pr(when C$_3$)*V$_3$+Pr(whenC$_4$)*V$_4$ + [1-Pr(whenC$_1$)-Pr(whenC$_2$)-Pr(whenC$_3$)-Pr(whenC$_4$)] *Total_Val* (8)

Where P_{sdlp} is total leakage power consumption of the AND gate

$Total\_Val= V_1+V_2+V_3+V_4$ (9)

Now $Pr(C_1)$, $Pr(C_2)$, $Pr(C_3)$ are all zero as A1 and A2 of the AND gate is tied to ground . So the above equation simplifies to :

P_{sdlp} *of AND gate == Pr(whenC$_4$)*V$_4$ == 1*V$_4$== V$_4$* (10)

Pr(whenC4) = 1 as the inputs are tied to ground and hence this when condition will be evaluated to be true. But the leakage value V4 may not be the lowest value of power in the table .

So we can generalize that :

P_{sdlp} of a Spare gate == $Pr(whenC_x)*V_x$ (given that the inputs of spare cell are tied to evaluate condition C_x)

So the inputs of the spare gate are tied in such a way that , they evaluate to the when condition C_x. To reduce the leakage power consumption of the idle spare cells we need to tie the inputs of the spare gate in such a way which yields or maps to the lowest leakage value in the power model . In the proposed algorithm or flow we would be finding out the lowest leakage value V_{minx} for the spare gate and find the corresponding condition C_{minx}. This can be represented in the general form as :

If a spare master gate "spareN" has n input pins , then there can be 2^n when conditions or states in the power model and 2^n values of the leakage power values .

Input conditions for each values:

$$C_1, C_2, C_3 ....., C_{minx} .... C_2^{n-1}, C_2^n \qquad (11)$$

If corresponding leakage power values are :

$$V_1, V_2, V_3 ...., V_{minx} .... V_2^{n-1}, V_2^n \qquad (12)$$

Where min $[V_1, V_2, V_3 ...... V_{minx} ..... V_2^{n-1}, V_2^n] = V_{minx}$

The proposed flow would find the lowest leakage value V_{minx} for the spare master and would connect all the "n" inputs of the spare cell master "spareN" corresponding to the condition C_{minx} . So the minimum leakage power of the spare master as per the proposed flow would be :-

$$P_{[minsdlp, spareN]} = Pr(when C_{minx}) * V_{minx} \qquad (13)$$

$P_{[minsdlp, spareN]}$ = Minimum state dependent leakage power value of the spare gate master spareN

C_{minx} == Condition or state of the inputs of the spare master gate spareN which has the lowest state dependent leakage value V_{minx}

But the $Pr(when C_{minx}) = 1$ as the inputs of the spare master "spareN" are tied to always evaluate condition C_{minx}

So $P_{[minsdlp, spareN]} = V_{minx}$ for the spare master spareN .

If there are "m" instances of this spare master "spareN" in the design then as per the proposed flow the total state dependent leakage power consumption would be :-

$$Total\ P_{[sdlp, spareN]} = m * P_{[minsdlp, spareN]} \qquad (14)$$

as the inputs of all the "m"instances of the spareN master would be tied to values which would evaluate when condition C_{minx}

The proposed state dependent leakage power minimization flow for the spare cell is described in the below flow chart (Figure2).
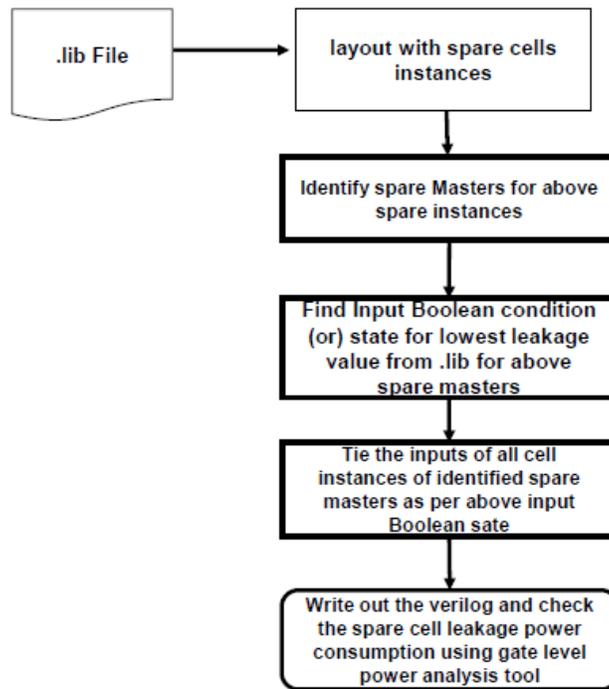
Figure.2 Proposed leakage minimization flow for spare cells

5. EXPERIMENTAL RESULTS

We tested the proposed flow in two different technology nodes (65nm and 45nm) using Synopsys's IC Compiler® for spare cell insertion in post placed design and PT-PX® to report state dependent leakage power of the spare cells. The results in Table 2 shows the comparison between the leakage power consumption of the spare cells in the traditional flow in which all inputs of the spare cells are tied to ground and the proposed flow in which the inputs of the spare cells are tied to the condition which gives minimum state dependent leakage. The spare cells distribution of design-B is shown in Figure 3. After this we routed these designs in IC Compiler®. The input connections made by the tool as per the proposed method for the spare cells OR and XNOR is shown in Figure 4.

Table2. State Dependent Leakage Power for 2-input AND gate

S.No	Design	Total Cell Count	Spare Cells Count (%)	Spare Cell Leakage (Traditional Flow)	Spare Cell Leakage (Proposed Flow)	% Reduction in spare cells leakage
1	A(65 nm)	165830	880 (5.3 %)	19.47 µW	15.8 µW	18.84 %
2	B (45nm)	1549	140 (9%)	2.993 µW	2.328 µW	22.21 %
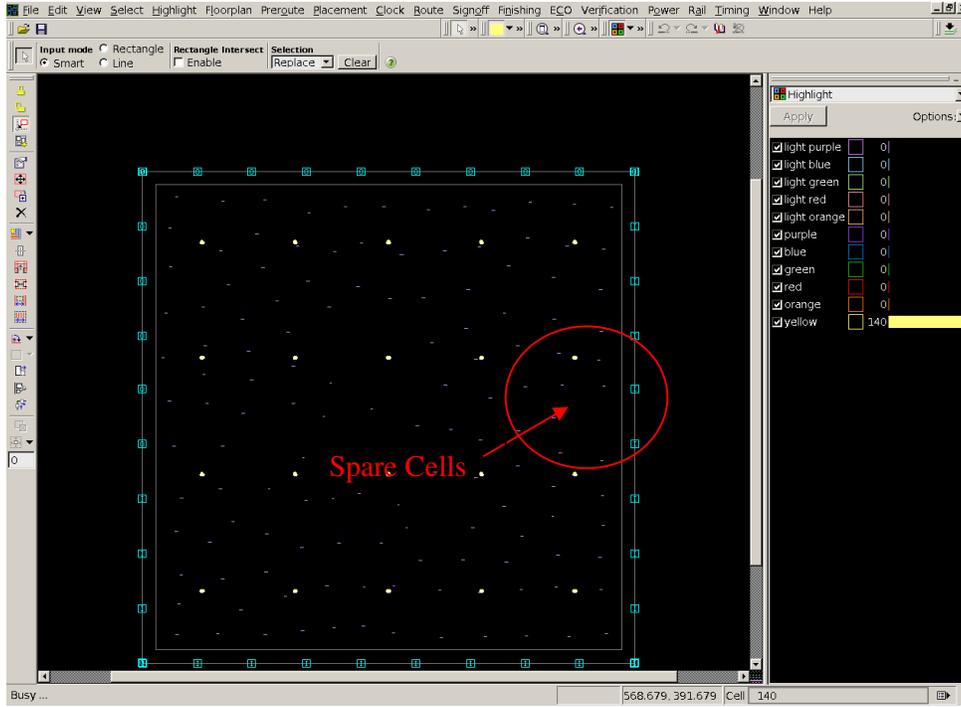
Figure.3 Spare cells present in Design-B (LVDS design, highlighted in yellow)
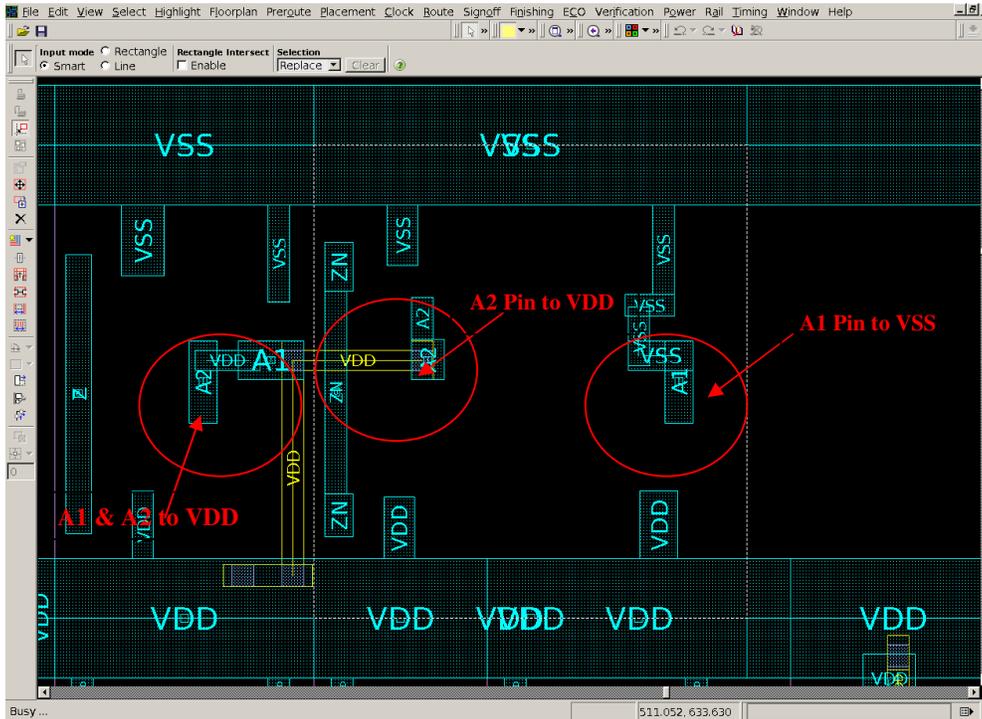
Figure.4 Spare cells OR and XNOR gates connections after routing as per state dependent leakage tables

6. CONCLUSIONS

In Deep sub micron nodes there is a need for minimizing leakage power as much as possible. The traditional way of connecting spare cells to power or ground rails may not guarantee less leakage power, as it is state dependent. In this paper we proposed a new method to minimize the leakage power of the idle spare cells in the layout by connecting their inputs to a state which guarantees less leakage. This proposed method was tested on post placed layouts and result shows that there a reduction of 22% leakage in 45nm and reduction of 19% in 65 nm design for spare cells. The future challenges in this direction includes taking care of multi voltage and multi corner designs, handling physical design challenges in the area of routing which will ensure minimum changes to the mask.

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