VLSI Design of Low Power High Speed 4 Bit Resolution Pipeline ADC In Submicron CMOS Technology

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Abstract

Analog-to-digital converters (ADCs) are key design blocks and are currently adopted in many application fields to improve digital systems, which achieve superior performances with respect to analog solutions. Application such as wireless communication and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. Widespread usage confers great importance to the design activities, which nowadays largely contributes to the production cost in integrated circuit devices (ICs). Various examples of ADC applications can be found in data acquisition systems, measurement systems and digital communication systems also imaging, instrumentation systems. Since the ADC has a continuous, infinite –valued signal as its input, the important analog points on the transfer curve x-axis for an ADC are the ones that corresponding to changes in the digital output word. These input transitions determine the amount of INL and DNL associated with the converter. Hence, we have to considered all the parameters and improving the associated performance may significantly reduce the industrial cost of an ADC manufacturing process and improved the resolution and design specially power consumption . The paper presents a design of 4 bit Pipeline ADC with low power dissipation implemented in <0.18μm.

Keyword

ADC, PIPELINE, CMOS

1. Introduction

ADC is the key components in communication and video system. With development of these electronics system, high resolution and high-speed ADCs are becoming more and more important. High-speed low-power Analog-to-Digital converters (ADCs) are the critical building blocks for modern communication and signal processing systems. They are the interface between the analog and digital signal processing. Since the mid-1970s. ADCs have been widely designed using integrating, successive approximation, flash, and delta-sigma techniques. More recently, there has appeared a new class of ADC with an architecture known as pipeline, which offered an attractive combination of high speed, high resolution, low power dissipation and small die size.

The pipeline ADC, therefore, became the optimum solution for present low power applications, such as a wireless communication system. A continued search for circuit architectures and

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techniques enabling ADCs to obtain higher speed and resolution with smaller chip area and lower power dissipation, therefore, is necessary.

The pipeline analog-to-digital converter (ADC) is a promising topology for high-speed data conversion with compact area and efficient power dissipation. Its speed of operation far surpasses that of serial-based structures, such as successive approximation or cyclic converters, while its die area and power dissipation favorably compare to that of flash and other more parallelized architectures. Pipelined ADCs are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, studio cameras, ultrasound monitors, and many other high speed applications.

An analog-to-digital converter (ADC) acts as a bridge between the analog and digital worlds. It is a necessary component whenever data from the analog domain, through sensors or transducers, should be digitally processed or when transmitting data between chips through either long-range wireless radio links or high-speed transmission between chips on the same printed circuit board.

As IC fabrication technology has advanced, more analog signal processing functions have been replaced by digital blocks ,analog-to-digital converters (ADCs) retain an important role in most modern electronic systems because most signals of interest are analog in nature and must to be converted to digital signals for further signal processing in the digital domain. With the continued proliferation of mixed analog and digital VLSI systems supporting diverse chip functionalities, the need for small sized, low-power and high-speed analog-to-digital converters using conventional CMOS process has increased. There is a wide variety of different ADC architectures available depending on there requirements of the application. They can range from high-speed, low resolution flash converters to the high-resolution, low-speed oversampled noise-shaping sigma-delta converters. Pipeline ADCs are one of the best examples. It typically generate one bit per clock cycle, the benefits are the low area needed for the implementation. This type of Pipeline ADC is fast, has a high resolution, and only requires a small die size compared to the merits of the successive approximation and flash ADCs.

2. Review Of Work

The first documented example of an ADC was a 5-bit, electro-optical and mechanical flash-type converter patented by Paul Rainey in 1921, used to transmit facsimile over telegraph lines with 5-bit pulse-coded modulation (PCM) .The first all electrical implementation came in 1937 by Alec Harvey Reeves, this also had a 5-bit resolution. Following the development of the transistor in 1947 and the integrated circuit in 1958, the ADC development continued in the1960's with for example an 8-bit, 10 MS/s converter that was used in misile-defense programs in the United States. First commercial converter, 1954 "DATRAC" 11-Bit, 50-kSPSSAR ADC Designed by Bernard M. Gordon at EPSCO.

In the recent years there has been a trend in ADC research to use low accuracy analog components which are compensated for through the use of digital error correction .Because of their popularity, pipeline ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. Many Pipeline ADCs now offer on-chip input multiplexers, making them the ideal choice for multichannel data acquisition system. An example of modern charge redistribution successive approximation ADCs is Analog Devices' PulSAR® series. The AD7641 is a 18-bit, 2-MSPS, fully differential, ADC that operates from a single 2.5 V power supply. The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, error correction circuits, internal reference, and both serial and parallel system interface ports. The AD7641 is hardware factory calibrated and comprehensively tested to ensure such ac

parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

The motivation behind this is that analog design have not been able to benefit from process scaling in the same way as digital logic and therefore the relatively area-cheap digital logic is used to compensate for the shortcomings of expensive analog circuits. For device reliability reasons, the supply voltage needs to be reduced to ensure gate oxide integrity over time and prevent p-n junction from breakdown. Present-day CMOS processes are making the transition from3.3 V to 1.8 V supplies. The converter should operate with high sampling rate from an operating supply as low as possible, to facilitate integration with low-voltage, power efficient digital circuits.

3. Pipeline ADC Design

Figure1. Shows the block diagram of pipeline ADC, All of the pipeline stages are identical in architecture, but sampling capacitances are scaled down along stages. Pipeline analog-to-digital converters use a technique similar to digital circuit pipelining to trade latency for throughput. In a pipeline converter only a few bits are resolved at a time. This approach increases the throughput and reduces the required number of comparators compared to a flash or half-flash converter.

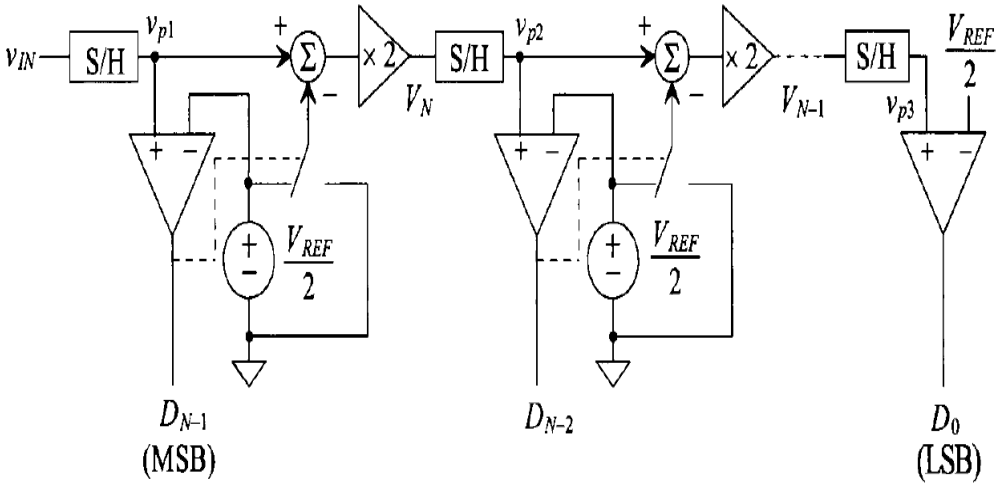

Figure 1. Pipeline ADC

A pipeline ADC (also called subranging quantizer) uses two or more steps of subranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits (for example, four bits) rather than just the next-most-significant bit.

The pipeline ADC is an N-step converter, with 1 bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N stages connected in series (Figure.1).

The required pipelined data converter has a resolution of 4 Bits, each stage with an ADC of 1 Bit - therefore the design it will contain:

• 1-bit ADC (a comparator)
• A sample-and-hold
• A summer
• A gain of two amplifiers.

Each stage of the converter performs the following operation:

1. After the input signal has been sampled, compare it to vref/2. The output of each comparator is the bit conversion for that stage.

2. If vm > vref/2 (comparator output is 1), vref/2 is subtracted from the held signal and pass the result to the amplifier. If VIN < vref/2 (comparator output is 0), then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the residue.

3. Multiply the result of the summation by 2 and pass the result to the sample and- hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial latency of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on the next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions. The disadvantage is having the initial N clock cycle delay before the first digital output appears. The severity of this disadvantage depends, of course, on the application. One interesting aspect of this converter is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

The Pipelined ADC can be thought of as an amplitude- interleaved topology where errors from one stage are correlated with errors from previous stage. The basic block diagram implementation of an N-bit Pipelined ADC using the cyclic stages is as shown in Figure 2.

Instead of cycling the analog output of the 1 bit/stage section back to its input, we feed the output into next stage. The stages are clocked with opposite phases of the master clock signal. The comparator outputs are labeled digital in figure.

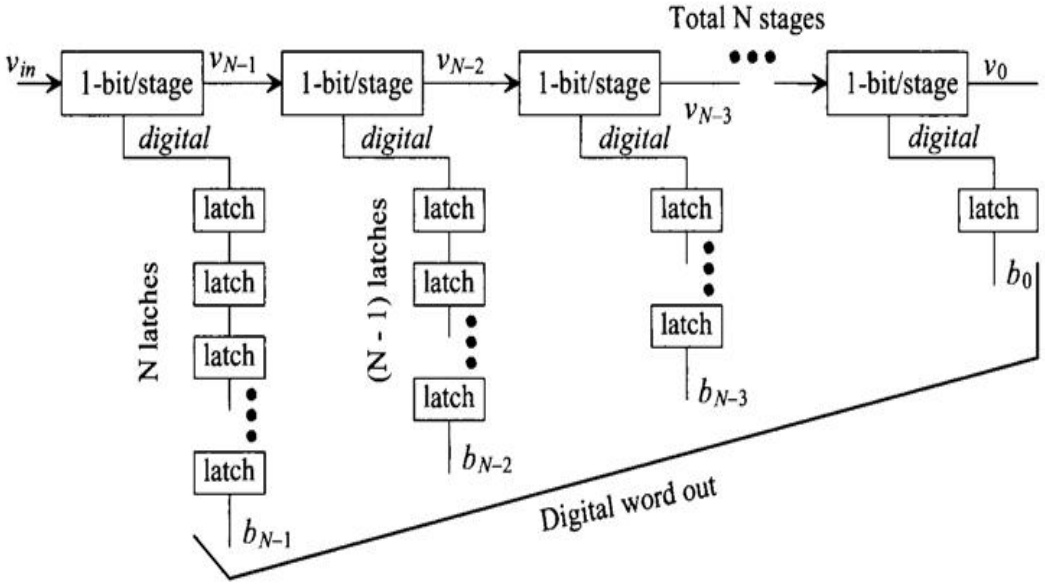

Figure 2. Pipeline ADC based on cyclic stages

The digital comparator outputs are delayed through latches so that the final digital output word corresponds to the input signal sampled N clock cycles earlier. The first stage in figure must be N-bit accurate. It must amplify its analog output voltage, V_{N-1} to within 1 LSB of the ideal value. The second stage output, V_{N-2} must be an analog voltage within 2 LSB of its ideal value. The third stage output, V_{N-3} must be an analog voltage within 4 LSB of its ideal value.

4. Circuit Implementation

A mathematical model of a 4-bit pipeline ADC is presented in this paper. This section mainly focuses on the design and implementation of the principle circuit of pipeline ADC, such as S/H, Comparator and Residue amplifier, and puts forward specific circuits accordingly.

The design consists of three main blocks:

4.1 Sample and hold circuit

SHC is an important building block in the pipeline ADC architecture and other data-converter systems since the system throughput and accuracy are limited by the speed and precision at which the input and residue analog voltages are sampled and held. Figure 2 depicts the schematic diagram of SHC architecture utilised in the proposed pipeline ADC. It employs the series sampling technique, and the output is feedback to the first OPAM. The main advantages of this architecture are that the charge injection error and the clock feedthrough error are effectively removed. This type of SHC, therefore, obtains a very high-accuracy characteristic.

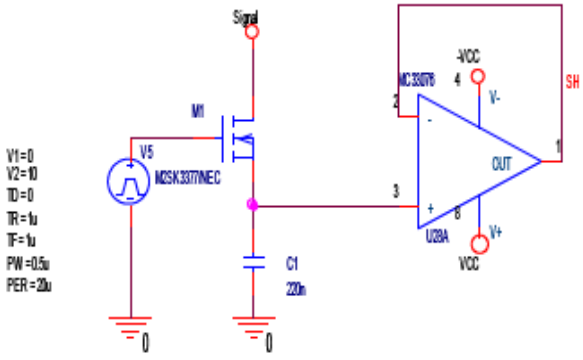

Figure 3. Sample & Hold @ 50 KHz.

4.2 Bit coarse ADC (Comparator).

Flash ADCs are typically employed as coarse and fine ADCs in pipeline ADC architecture. However, the major disadvantages of the full flash ADC architectures are high device power consumption, high device complexity and high device input capacitance. The modified flash ADC, which utilised an optimised latched-type comparator**,** can perform the Analog-to-Digital *(A/D)* conversion in one clock cycle (like a full flash ADC). The main advantage of the modified flash ADC approach is the great reduction in the number of comparators. Therefore the device obtains a great power saving and size reduction.

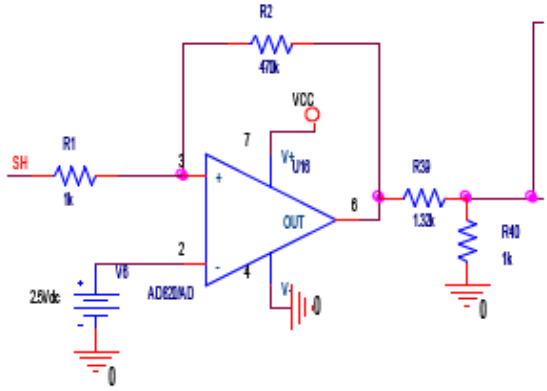

Figure 4. Comparator.

4.3 Adder and Amplifier

The residue amplifier is the most important circuit and affects the performance of MDAC directly. Since residue amplifier operates in close-loop state, its open-loop gain and unity-gain bandwidth (GWB) must satisfy the follow functions.

$$A0 > 2^{N+1} / f$$

$$GBW > \frac{3k\,(N+1)\ln 2}{2\pi\, Tf}$$

Where N=4, f represents the feedback factor and its ideal value is 0.5, k is similar to 1 and related to parasitic capacitance, sample capacitance and load capacitance, T is the clock period and is equal to 12.5ns as for a 4 bits pipeline ADC . Considering enough margins the open-loop gain of residue amplifier must exceed 90dB, GBW is greater than 760MHz, and its setting time must below 10ns.

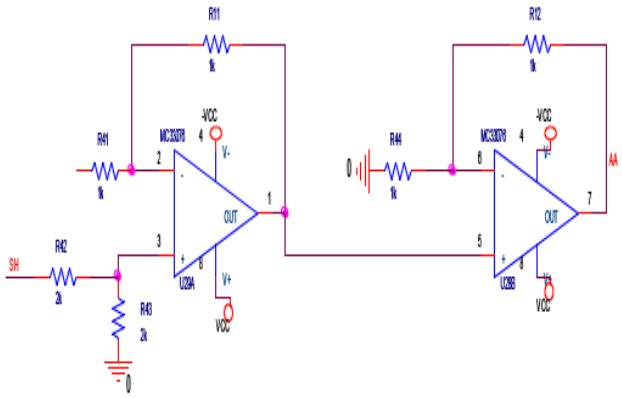

Figure 5. Adder and Amplifier.

The description of each stage is as follows.

According to the block diagram from Figure. 1, we first need to pass the signal by a comparator, to do so the original analog signal must be sampled and held so the comparator is fed a stable signal. After the first bit is obtained, it needs to be subtracted from the original signal to obtain

the residue that will be entering the next conversion stage. The residue will also be amplified to remain in the full-scale range of the comparator to reduce loss of resolution. Each portion of the comparator outputs a bit of the data converter and every single output will contain a latch.

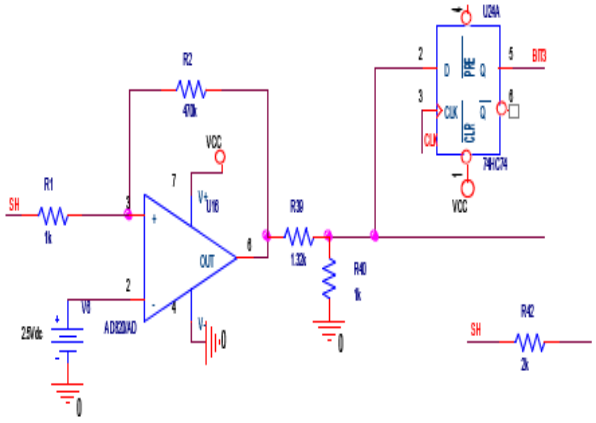

Figure 6. Latch shown on the top right.

Manufacturers have recently introduced high-performance analog-to-digital converters (ADCs) that feature outstanding static and dynamic performance. The following discussion should shed some light on techniques for testing two of the accuracy parameters important for ADCs: integral nonlinearity (INL) and differential nonlinearity (DNL).

Resolution:

The resolution of the pipeline ADC expresses the number of discrete values which can produce over the range of analog values. Electronically values are usually stored in the binary form, in order to express the resolution in the form of bits. In consequence, the number of discrete values available, or "levels", is a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Number of quantization levels = 2^n

Integral Nonlinearity:

Integral nonlinearity (INL) is defined similarly to that for a DAC. Again, a "best-fit" straight line is drawn through the end points of the first and last code transition, with INL being defined as the difference between the data converter code transition points and the straight line with all other errors set to zero. Missing codes it is of interest to note the consequences of having a DNL that is equal to -1 LSB straight line drawn through the first and last output values, INL defines the linearity of the overall transfer curve and can be described as

INLn = Output value for input code *n* Output value of the reference line at that point.

The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

$INL = | [(V_D - V_{ZERO})/V_{LSB\text{-}IDEAL}] - D |$, where $0 < D < 2^N-1$.

V_D is the analog value represented by the digital output code D, N is the ADC's resolution, V_{ZERO} is the minimum analog input corresponding to an all-zero output code, and $V_{LSB-IDEAL}$ is the ideal spacing for two adjacent output codes.

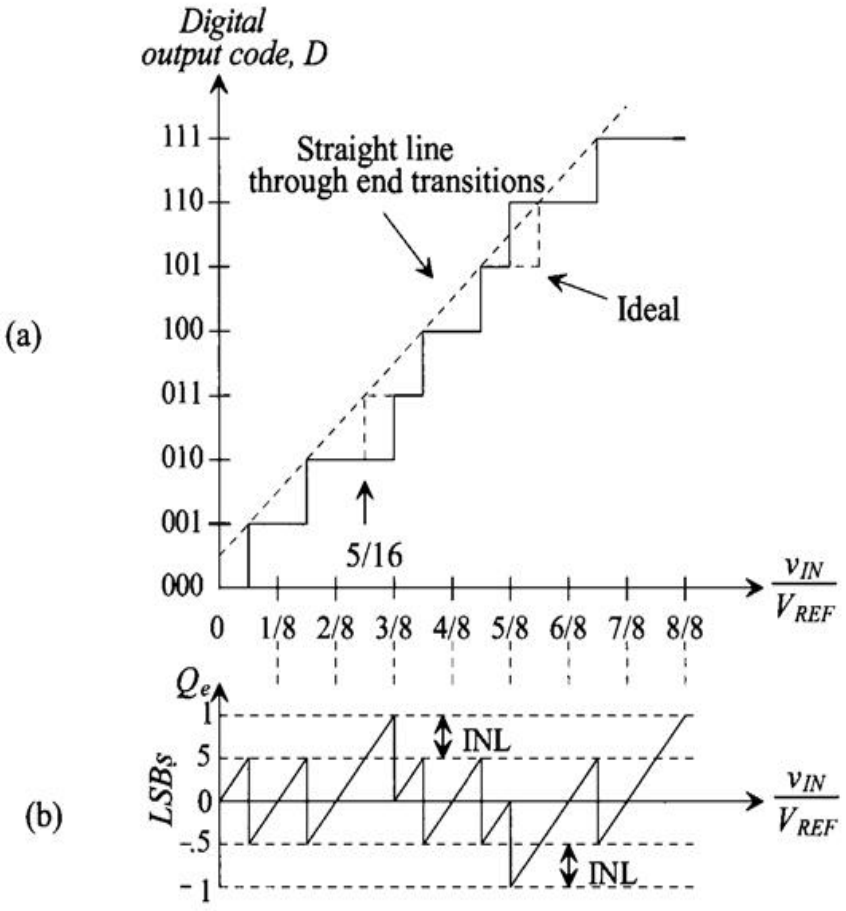

Figure 7. (a) Transfer curve for nonideal ADC
(b) Quantization error illustrating INL

Differential Nonlinearity:

DNL is the difference between the actual code width of a nonideal converter and the ideal case. Nonideal components cause the analog increments to differ from their ideal values. The difference between the ideal and the nonideal values is knows as Differential Nonlinearity or DNL and is defined as

DNL = Actual step width - Ideal step width

For an ideal ADC, in which the differential nonlinearity coincides with DNL = 0LSB, each analog step equals 1LSB (1LSB = $V_{FSR}/2^N$), where V_{FSR} is the full-scale range and N is the resolution of the ADC and the transition values are spaced exactly 1LSB apart.

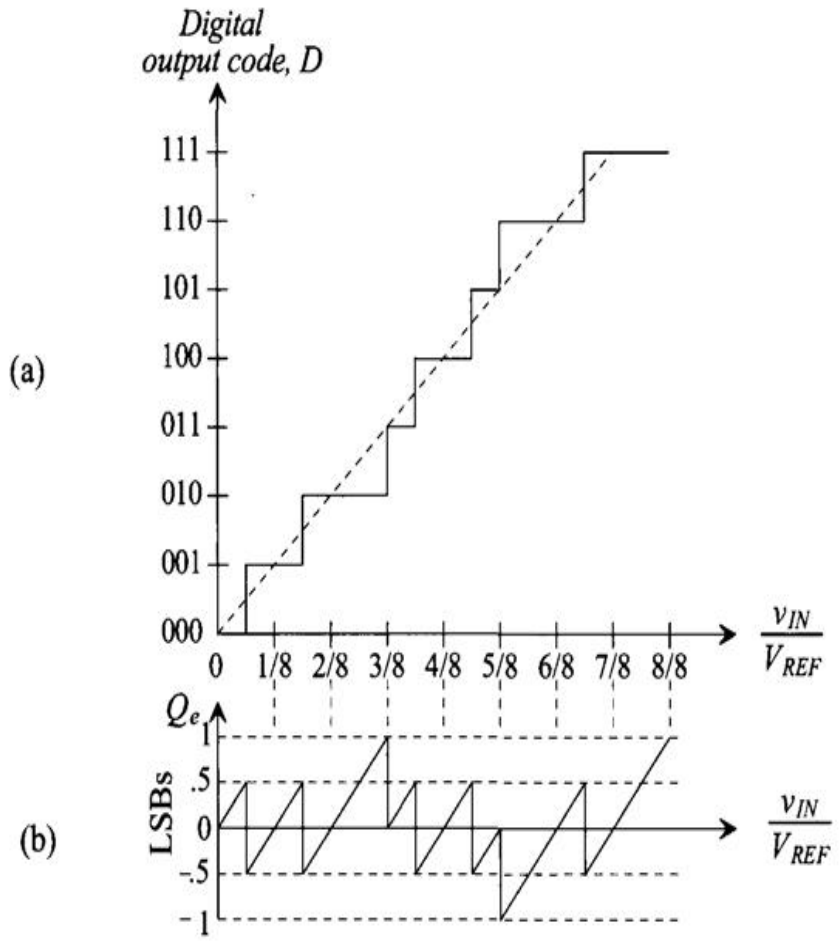

Figure 8. (a) Transfer curve for nonideal ADC
(b) Quantization error illustrating DNL

5. Pipeline ADC versus Other ADCs

Power dissipation of Pipeline ADCs varies with the sampling rate unlike Flash and SAR architectures. Hence find applications in PDAs.

The main advantages of SAR ADC's are low power consumption, high resolution, and accuracy. In a SAR ADC, increased resolution comes with the increased cost of more-accurate internal components.

Flash ADC is much faster, less accurate and takes more silicon area due to the number of comparators 2N for N bit resolution.

Oversampled/Σ-J ADCs have low conversion rates, high precision, averaging noise and no requirement for trimming or calibration even up to 16 bits of resolution.

Types of ADCs

A survey of the field of current A/D converter research reveals that a majority of effort has been directed to four different types of architecture : Pipeline, Flash type, Successive-approximation

and oversampled ADC. Each has benefits that are unique to that architecture and span the spectrum of high speed and resolution.

5.1 Successive-approximation ADCs

The method of addressing the digital ramp ADC's shortcomings is the so-called successive-approximation ADC. The only change in this design is a very special counter circuit known as a successive-approximation register. Successive approximation converter performs basically a binary search through all possible quantization levels before converging on the final digital answer. The block diagram is shown in figure 9.

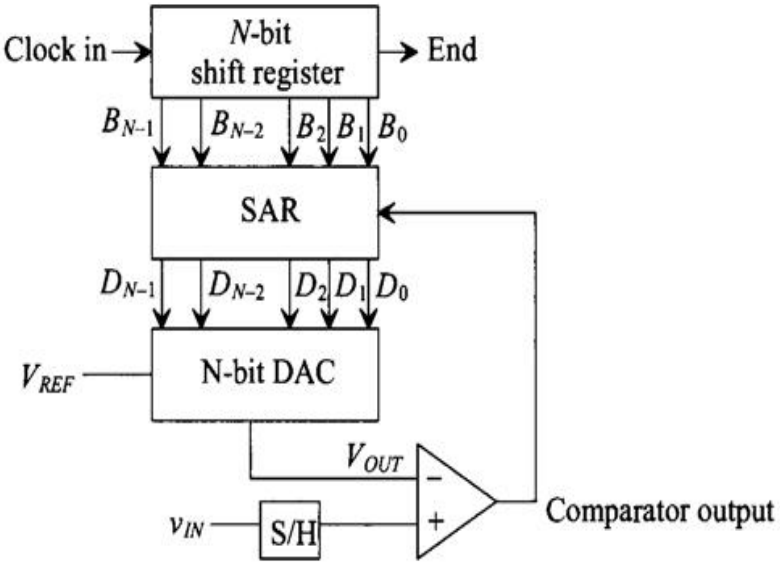

Figure 9. Block diagram of SAR ADC

An N-bit register controls the timing of the conversion where N is the resolution of the ADC. V_{IN} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search and the output of the successive approximation register (SAR) is the actual digital conversion.

5.2 Direct-conversion ADCs

Flash or parallel converters have the highest speed of any type of ADC. As shown in figure 10 Flash ADC uses one comparator per quantization level (2^N-1) and 2^N resistors. The reference voltage is divided into 2^N values, each of which is fed into comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code exhibits all zeros for each resistor level if the value of V_{IN} is less than the value on the resistor string, and ones if V_{IN} greater than or equal to voltage on the resistor string. A simple 2^N-1: N digital thermometer decoder circuit converts the compared data into an N-bit digital word.

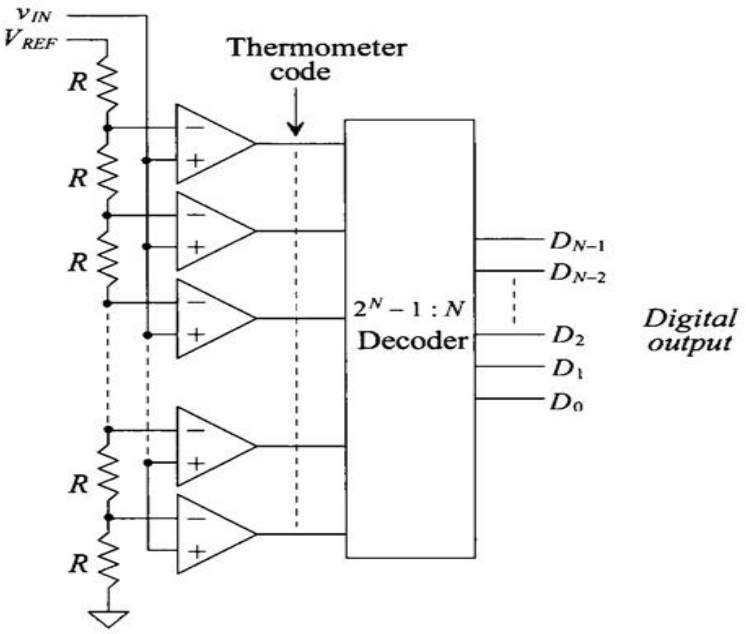

Figure 10. Block diagram of Flash ADC

The advantage of this converter is the speed with which one conversion can take place. The disadvantage of the Flash ADC is the area and power requirements of the 2^N-1 comparators. The speed is limited by the switching of the comparators and the digital logic.

5.3 Sigma-delta ADCs

The oversampling ADC is able to achieve much higher resolution than the Nyquist rate converters. This is because digital signal processing techniques are used in place of complex and precise analog components. The accuracy of this converter does not depend on the component matching, precise sample and hold circuitry or trimming and only a small amount of analog circuitry is required. The block diagram of Sigma-delta ADC is shown in figure 11.

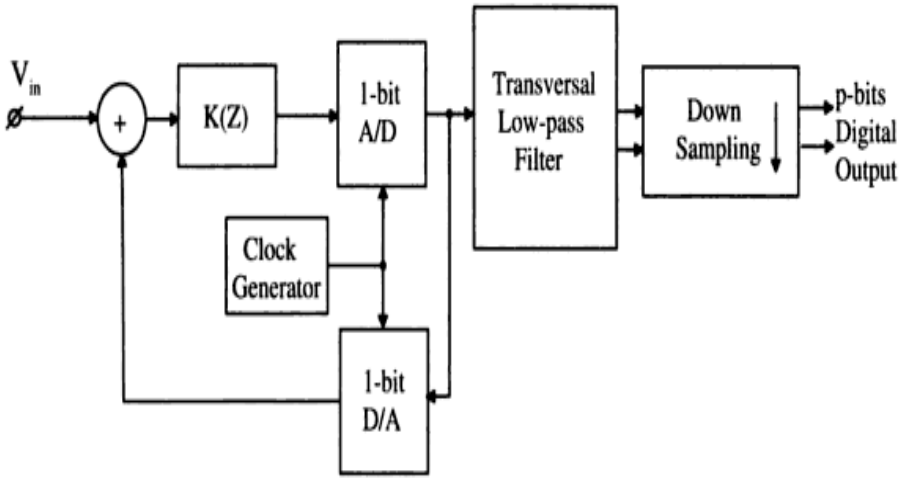

Figure 11. Block diagram of Sigma-delta ADC

From the input signal, the output signal of the 1-bit D/A converter is subtracted. The difference of these two signals is filtered by the loop filter and the output signal of the loop filter is applied to the 1-bit quantizer or A/D converter. The clock frequency of the system is high compared to the maximum analog input frequency. Noise-shaping filters can be recalculated into sigma-delta filters showing nearly identical performance. In this way an identical analysis can be performed. The output of the 1-bit A/D converter is usually applied to a digital low-pass which rejects signals above the signal band of interest. Then sub-sampling or decimation is applied to obtain multi-bit output code. The whole operation results in a binary- weighted digital output signal that can have a minimum sampling ratio equal to twice the signal bandwidth.

6. Simulation Result

The designed pipeline ADC employing the modified flash ADC topology and the pipeline ADC employing the full flash ADC approach have been both implemented and simulated in cad Analog Environment, and comparison of their performance has been made. Figure (7) and Figure (8) presents the plots of transfer curve of nonideal ADC and differential nonlinearity (DNL) and integral nonlinearity (INL) quantization errors of the designed pipeline ADC. From this analysis, we can conclude the advantages of the pipeline ADC employing a modified flash ADC architecture, which include less components therefore smaller size, and lower power consumption. These characteristics make this new device better candidate for many applications where power and size are the major factors.

7. Conclusion

This paper studied the design of 4 bit Pipeline ADC in < 0.18 μm CMOS technology. Pipeline ADC is the key design Block in modern microelectronics digital communication system. With the fast advancement of CMOS fabrication technology and continued proliferation of mixed analog and digital VLSI systems, the need for small sized, low-power and high-speed analog-to-digital converters has increased. Therefore the Pipeline ADC architecture is very popular in CMOS technology. A high resolution at a high sampling frequency is possible using the pipeline architecture. Sharing of amplifier in a Pipeline converter is possible. This reduces power consumption and reduces die size.

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