USING CMOS SUB-MICRON TECHNOLOGY VLSI IMPLEMENTATION OF LOW POWER, HIGH SPEED SRAM CELL AND DRAM CELL

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ABSTRACT

Abstract This paper deals with the design and analysis of high speed Static Random Access Memory (SRAM) cell and Dynamic Random Access Memory (DRAM) cell to develop low power consumption. SRAM and DRAM cells have been the predominant technologies used to implement memory cells in computer systems, each one having its advantages and shortcomings. SRAM cells are faster and require no refresh since reads are not destructive. In contrast, DRAM cells provide higher density and minimal leakage energy. Here we use 12-transistor SRAM cell built from a simple static latch and tri state inverter. The reading action itself refreshes the content of memory. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). The decoder which constitutes the path from address input to the word line rise is implemented as a binary structure by implementing a multi-stage path. The key to low power operation in the SRAM data path is to reduce the signal swings on the high capacitance nodes like the bit lines and the data lines.

KEYWORDS

Keywords SRAM, DRAM, Low power, 12-T SRAM cell

1. INTRODUCTION

Static Random Access Memories (SRAM) and dynamic RAM (DRAM) have been the predominant technologies used to implement memory cells in computer systems. SRAM cells, typically implemented with six transistors (6T cells) have been usually designed for speed, while DRAM cells, implemented with only one capacitor and the corresponding pass transistor (1T1C cells) have been generally designed for density. Because of this reason, the former technology has been used to implement cache memories and the latter for main memory storage. Cache memories occupy an important percentage of the overall die area. A major drawback of these memories is the amount of dissipated static energy or leakage, which is proportional to the number of transistors used to implement these structures. However, although leakage currents are reduced, they still persist. In contrast, dynamic 1T1C cells avoid this drawback by design, since the power

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supply is removed after accessing the memory cells. Typically, 1T1C DRAM cells were too slow to implement processor caches. However, technology advances have recently allowed embedding DRAM cells using CMOS technology. Despite technology advances, an important drawback of DRAM cells is that reads are destructive, that is, the capacitor loses its state when it is read. Table1 summarizes the main design characteristics of the discussed cells. In addition, capacitors lose their charge a long time, thus they must be recharged or refreshed. To refresh memory cells, extra refresh logic is required which in turn results not only in additional power consumption but also in availability overhead.

Technology	SRAM (6T)	DRAM (1T1C)	eDRAM
Access time	fast	slow	slow
Density	low	high	high
Leakage	high	low	low
Refresh	no	yes	yes
Destructive reads	no	yes	yes

Table1: Memory Cell Characteristics

1.1 An Introduction to SRAM

The fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. Fig (1) shows a 12-transistor SRAM cell built from a simple static latch and tri-state inverter. The cell has a single bit line. True and complementary read and write signals are used in place of a single word line. A representative layout in Fig (3) has an area of 46 x 75 X. The power and ground lines can be shared between mirrored adjacent cells, but the area is still limited by the wires and is undesirably large. However, the cell is easy to design because all nodes swing rail-to-rail and it is fast when used in small RAMs and register files. Fig (2) shows a 6-transistor (6T) SRAM commonly used in practice. Such a cell uses a single word line and both true and complementary bid lines. The complementary bit- line is often called bit or bit. The cell contains a pair of cross-coupled inverters and an access transistor for each bit line. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to VDD or GND. The word line is asserted to read or write the cell.

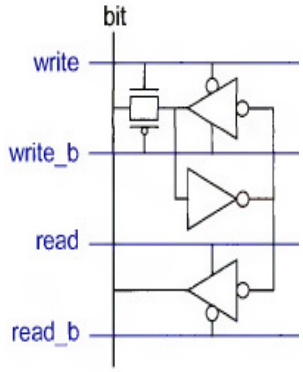


Fig 1: 12-transistor SRAM cell

Two types of SRAM cells will be considered in this paper. (i) Conventional Twelve-transistor (12T) SRAM cell, as shown in Figure 1. (ii) Load less six-transistor (6T) SRAM Cell, as shown in Figure 2. They will be designed and analyzed in various configurations with respect to functionality, power dissipation, area occupancy, stability and access time. True and complementary versions of the data are stored on the cross-coupled inverters.

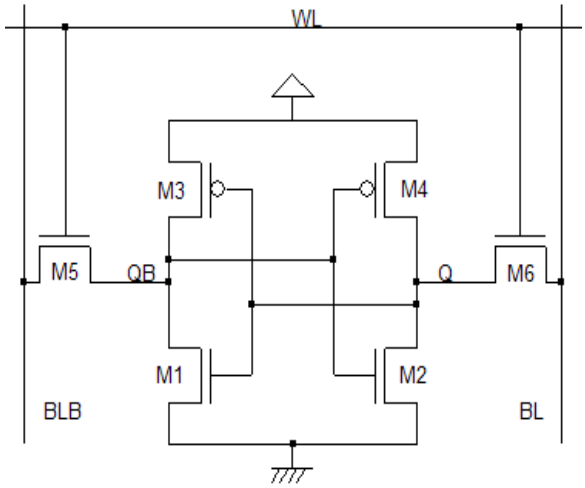


Fig 2: Conventional 6T SRAM Cell

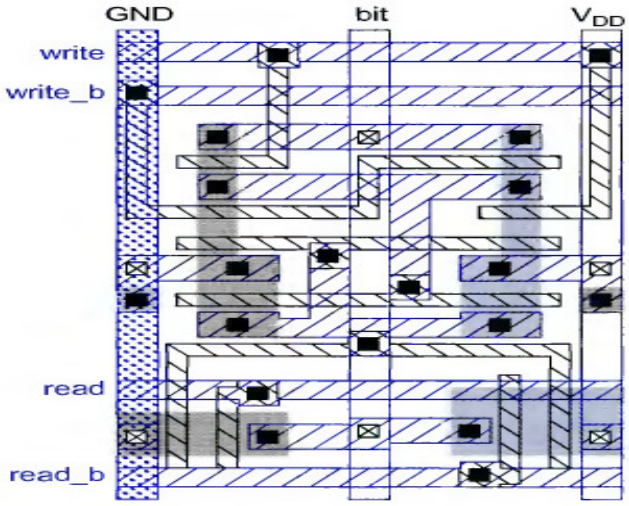


Fig 3: Representative layout of 46 x 75 X

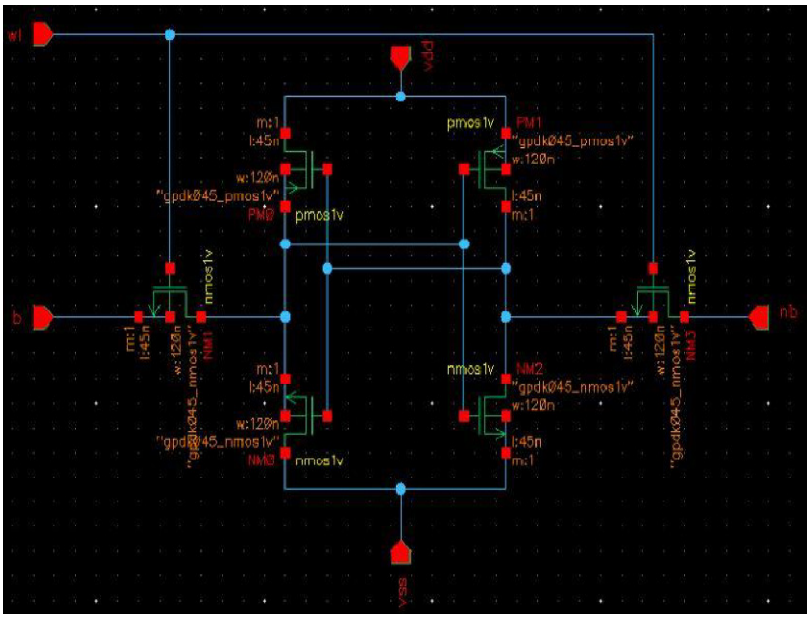
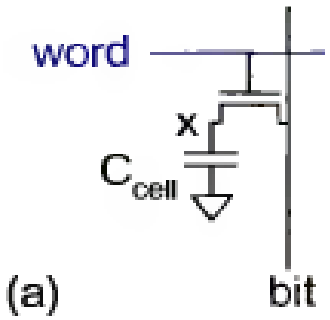


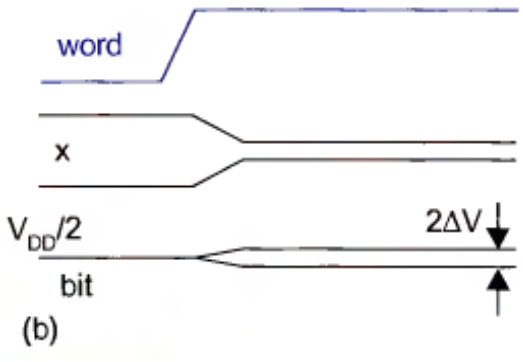
Fig 4: Schematic of SRAM cell

1.2 An Introduction to DRAM

Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (GB) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive. Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology. In most cases, advances in one have enabled advances in the other. Dynamic RAMs (DRAMs) store their contents as charge on a capacitor rather than in a feedback loop. Thus, the basic cell is substantially smaller than SRAM, but the cell must be periodically read and refreshed so that its contents do not leak away. Commercial DRAMs are built in specialized processes optimized for dense capacitor structures. They offer an order of magnitude greater density (bits/cm2) than high-performance SRAM built in a standard logic process, but they also have much higher latency. DRAM circuit design is a very specialized art. This section provides an overview of the general technique.



A 1-transistor (IT) dynamic RAM cell consists of a transistor and a capacitor, as shown in Figure (a). Like SRAM, the cell is accessed by asserting the word line to connect the capacitor to the bit line. On a read, the bit line is first pre charged to VDD/2. When the word line rises, the capacitor shares its charge with the bit line, causing a voltage change A V that can be sensed, as shown in Figure (b).



The read disturbs the cell contents at x, so the cell must be rewritten after each read. On a write, the bit line is driven high or low and the voltage is forced onto the capacitor. Some DRAMs drive the word line to VDDP = VDD + Vt to avoid a degraded level when writing a '1.' The DRAM capacitor must be as physically small as possible to achieve good density. However, the bit line is contacted to many DRAM cells and has a relatively large capacitance C bit. Therefore, the cell capacitance is typically much smaller than the bit line capacitance.

2. MEMORY ARCHITECTURE

The preferred organization for Random access memories is shown in Fig 5. This organization is random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bit lines.

A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. Memories may simultaneously select 4, 8, 16, 32, or 64columns in one row depending on the application. The row and column (or groups of columns) to be selected are determined by decoding binary address information. In this design, the number of rows and columns, both are equal to 64 for 4Mb memory cut. Using two such memory cuts, a 8Mb SRAM memory is designed.

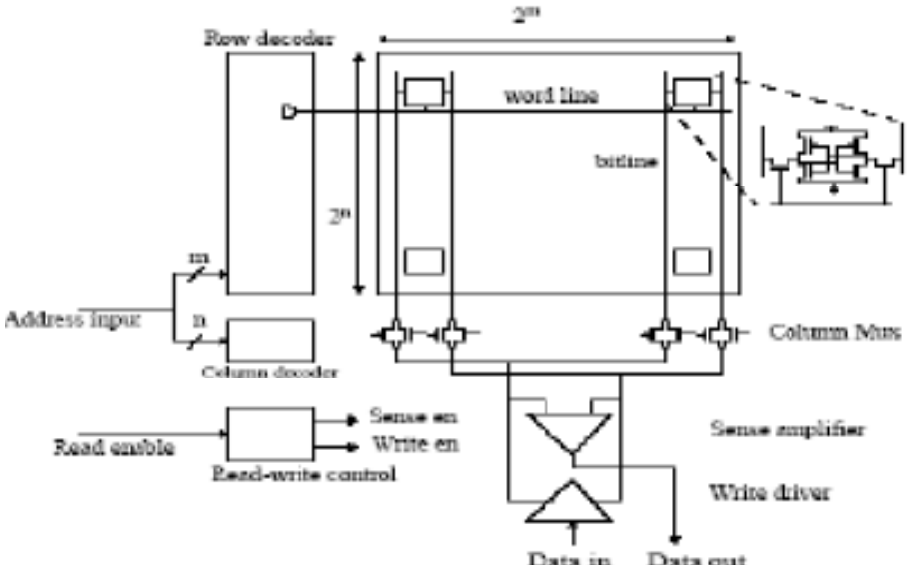


Fig 5: SRAM Memory Architecture

3. SENSE AMPLIFIER

The sense amplifiers have to amplify the data which is present on the bit lines during the read operation. The memory cells are small in size, and hence cannot the discharge the bit lines fast enough. Also, the bit lines continue to slew till a large differential voltage is formed between them. This causes significant power dissipation since the bit lines have large capacitances.

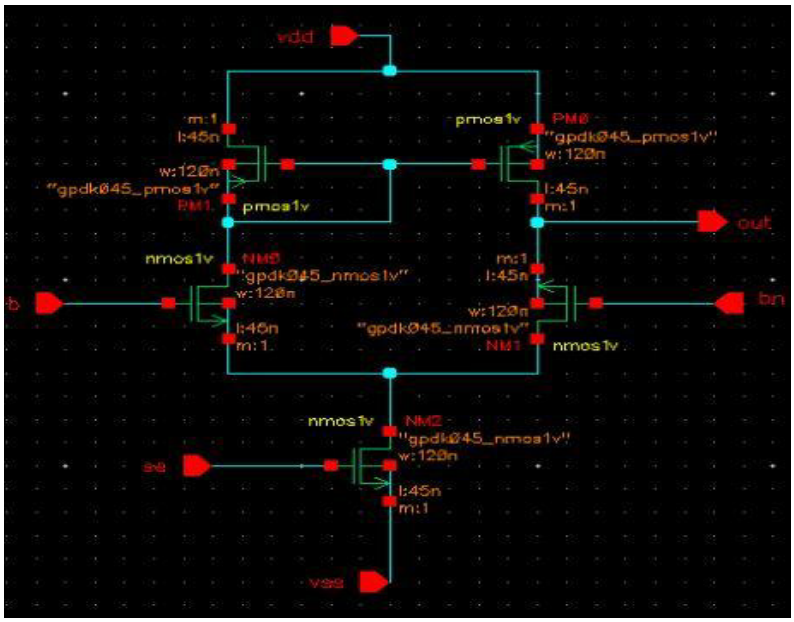


Fig 6: Schematic of sense amplifier

Hence, by limiting the word line pulse width we can control the amount of charge pulled down by the bit lines and hence limit power dissipation. The schematic and symbol are as shown below. It consists of two cross coupled gain stages which are enabled by the sense clock signal. The cross coupled stage ensures a full amplification of the input signal. This type of amplifier consumes least amount of power, however they can potentially be slower since some timing margin is needed for the generation of the sense clock signal. If the sense amplifiers enabled before sufficient differential voltage is formed, it could lead to a wrong output. Thus, the timing of the sense clock signal needs to be such that the sense amplifier can operate over various process corners and temperature ranges.

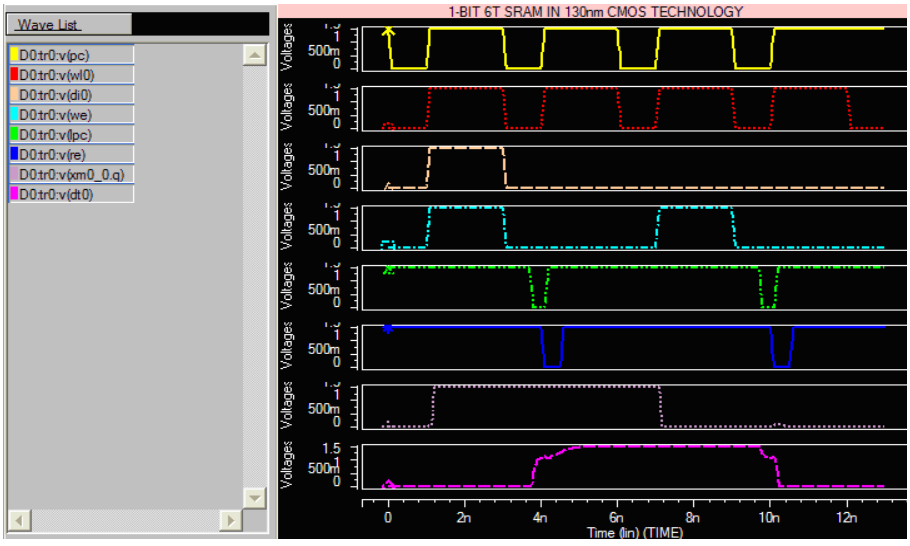
In this sense amplifier Bit lines have many cells attached. If we take example of that
Ex: 32-kbit SRAM has 256 rows x 128 cols. On each bit line 128 cells are present.

Sense amplifiers are triggered on small voltage swing (reduce ΔV).Even with shared diffusion contacts, 64C of diffusion capacitance are there. Discharged slowly through small transistors.

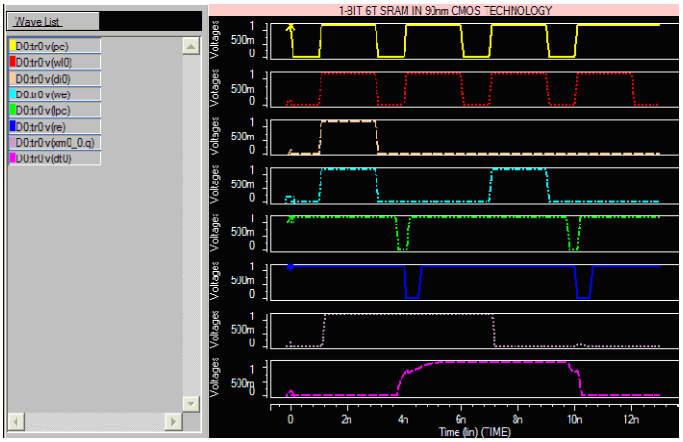
4. SIMULATION ENVIRONMENT AND RESULTS

The following configuration of SRAM arrays were designed and analyzed using the conventional 6T SRAM Cell: (a) 1*1 (b) 16*16 (c) 32*32. The various configurations were simulated using HSPICE using the Nominal Predictive Technology Model (PTM) in 130nm, 90nm and 65nm CMOS technologies. The functionality of 1*1 6T SRAM cell is shown in Figure. 7 The For 1K-bit (32*32) configuration along with the relevant input control signals, only the signals for three input data bits (0th, 16th and 31st), three output data bits (0th,16th and 31st), and the corresponding storage nodes of the appropriate cell is presented.

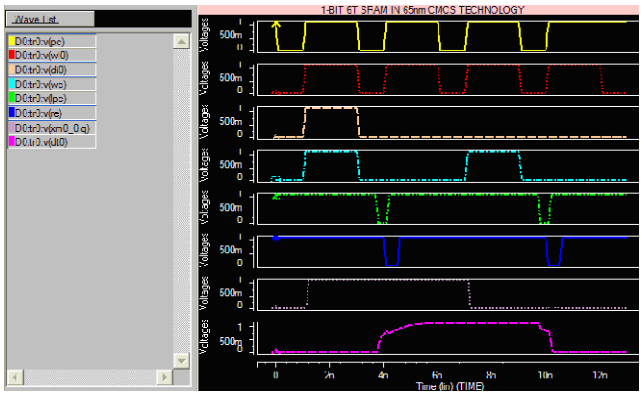
Cadence simulation of transient analysis and DC analysis gave good results. The results are shown in the timing diagram. The noise margins are very good and the output is stable.



(a)



(b



(c)

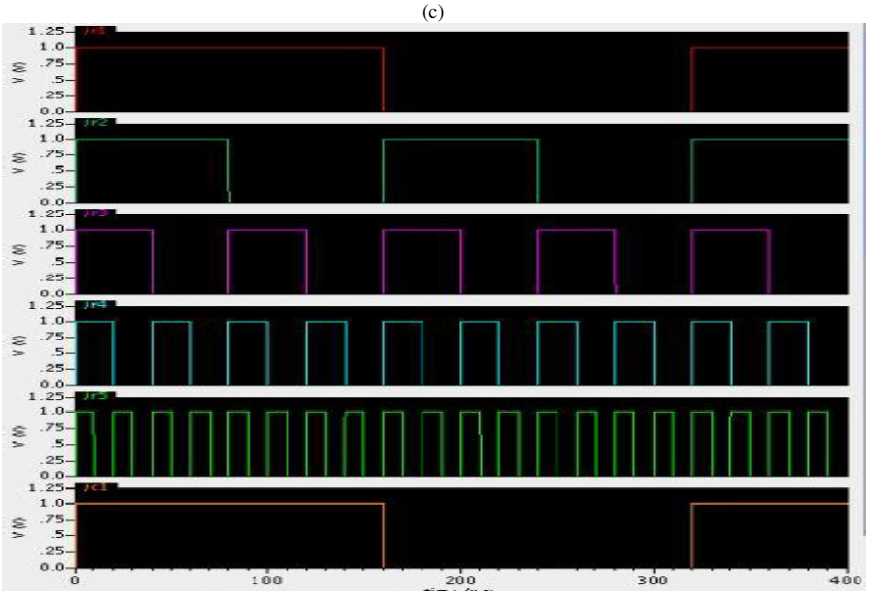


Fig 8: Timing Diagram

5. DESIGN FLOW

Cadence design Systems is electronic design automation software and engineering Services Company that offers various types of design and verification tasks that include:

Virtuoso Platform - Tools for designing full-custom integrated circuits, includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation.

Encounter Platform - Tools for creation of digital integrated circuits. This includes floor planning, synthesis, test, and place and route.

Incisive Platform - Tools for simulation and functional verification of RTL including Verilog, VHDL and System C based models. Includes formal verification, formal equivalence checking, hardware acceleration, and emulation.

The proposed work is done in Virtuoso platform using gpdk45 nm technology. The flow of design is as shown below.

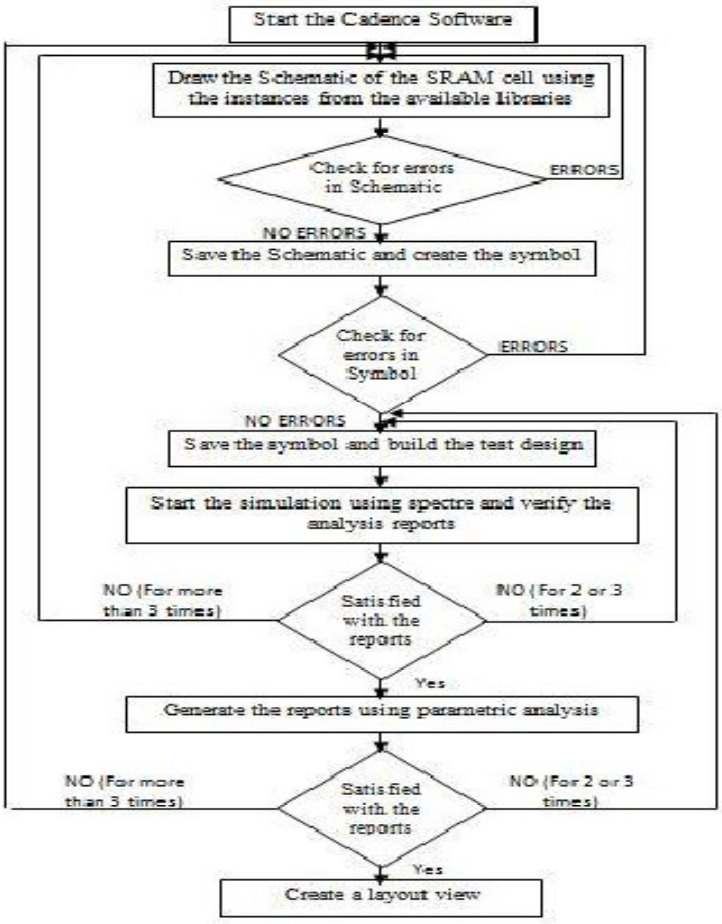


Fig 9: Design Flow

6. CONCLUSION

The New Load less 6T-SRAM cell is designed and analyzed in deep submicron (130nm, 90nm and 65nm) CMOS technologies, which establish the technology independence of the New Load less 4T SRAM cell and its consistent performance with respect to Conventional 6T SRAM cell in deep sub-micron regime. The New Load less 6T SRAM array consumes low power with low area. The most significant feature of this new load less 4T SRAM Cell is that there is no need to modify any of the fabrication process. Thus it can be used for on-chip caches in embedded microprocessors, high density SRAMs embedded in any logic devices, as well as for stand-alone SRAM applications.

This paper presents the design of SRAM array in 45 nm having very low power consumption. The low power design of SRAM is investigated and 6T SRAM architecture is chosen for memory bit cell and an array is designed with that bit cell. Transient and parametric analyses were carried out in the simulation process and the power consumption is estimated. As stated earlier, the power consumption can further be reduced by partitioning the array and by using DWL scheme.

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