DESIGN OF LOW WRITE-POWER CONSUMPTION SRAM CELL BASED ON CNTFET AT 32nm TECHNOLOGY

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ABSTRACT

The SRAM which functions as the cache for system-on-chip is vital in the electronic industry. Carbon Nanotube Field Effect Transistor (CNFET) is used for high performance, high stability and low-power circuit designs as an alternative material to silicon in recent years. Therefore Design of SRAM Cell based on CNTFET is important for Low-power cache memory. In cells, the bit-lines are the most power consuming components because of larger power dissipation in driving long bit-line with large capacitance. The cache write consumes considerable large power due to full voltage swing on the bit-line. This Paper proposes a novel 7T SRAM cell based on CNTFET that only depends on one of bit lines for Write operation and reduce the write-power consumption. The read cycle also improved because of careful transistor sizing. HSPICE simulations of this circuit using Stanford CNFET model shows that 37.2% write power saving, read cycle improvement of 38.6%.

KEYWORDS

SRAM Cell, CNTFET, 32nm Technology, HSPICE, Low-Power

1. INTRODUCTION

The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases [1- 2]. The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using SRAM cells. The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation [3]. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines [4-6]. Especially for modern VLSI processor design, SRAM takes large part of power consumption portion and area overhead.

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Since the first CNTFET was reported in 1998, great progress has been made during the past years in all the areas of CNTFET science and technology, including materials, devices, and circuits [7]. On the other hand, as the feature size of silicon semiconductor devices scales down to nanometer range, planar bulk CMOS design and fabrication encounter significant challenges [8]. CNTFET among other new materials is promising due to the unique one-dimensional band-structure which reduces backscattering and makes near-ballistic operation. Exceptional electrical properties such as high speed, high-K compatibility, chemical stability, low SCEs have provided CNFETs with excellent characteristics which exceed those of the state of the art Si-based MOSFETs. Several researches have been done to estimate the performance of CNTFET at a single device level in the presence of process related non-idealities and imperfections at the 32 nm technology node using compact CNFET SPICE model [9][10].

While seeking for solutions with higher integration, performance, stability, and lower power, carbon nanotube (CNT) has been presented for next-generation SRAM design as an alternative material in recent years [11]-[15].This paper proposes a novel 7T SRAM cell based on CNTFET to reduce dynamic write-power and to improve the read cycle at the cost of minimal increase of cell area.

2. THE CARBON NANOTUBE FET

Figure 1 illustrates a conceptual layout of a CNT transistor based on Stanford CNFET model. Ideally, several semiconducting CNTs grow on quartz or Si substrate in an exactly straight and parallel pattern. Those segments which are covered by gate are intrinsic CNT regions, whose conductivity is controlled by the gate. Drain and source segments of CNTs are heavily doped to form Ptype or N-type transistor. The drain, gate and source metal contacts and interconnects are defined by conventional lithography. Pitch size, namely the inter-CNT distance, is determined by CNT syntheses process since CNTs are grown in a self-assembly way. Gate width is determined by CNT tube number and pitch.

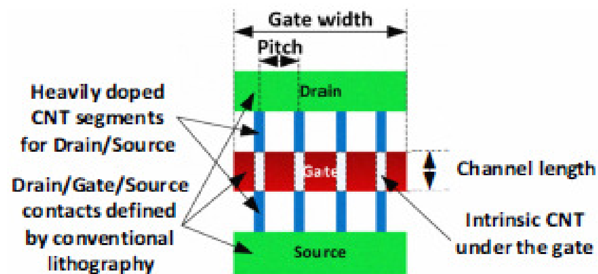


Figure 1. The CNTFET layout

CNTFET refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. It is a three-terminal device consisting of a semiconducting nanotube bringing two contacts (source and drain), and acting as a carrier channel, which is turned on or off electrically via the third contact (gate).

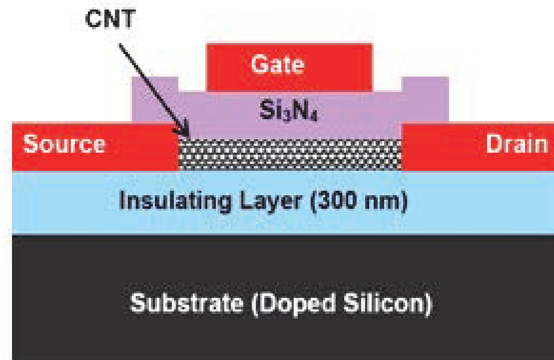
A single-wall carbon nanotube (SWCNT) is a tube formed by rolling a single sheet of graphene. It can either be metallic or semiconducting depends on the chirality vector (m, n), i.e. the direction in that the graphene sheet is rolled. For CNFETs, the threshold voltage of the transistor

is defined by the diameter of the carbon nanotubes, which is related to the chirality vector as follows:

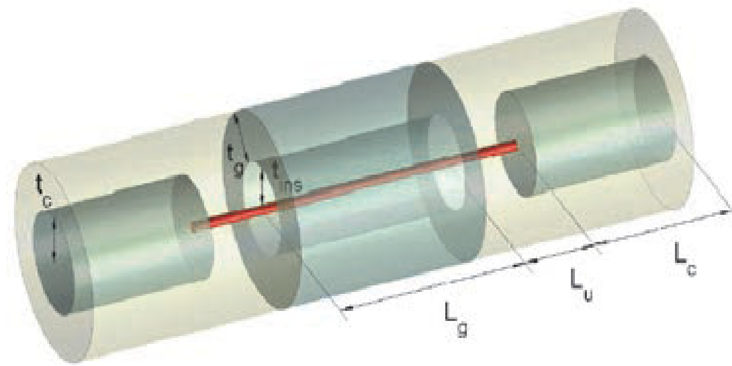
$$D_{CNT} = \frac{a}{\pi}\sqrt{m^2 + n^2 + mn} \quad (1)$$

$$V_{TH} = \frac{aV_\pi}{\sqrt{3} * qD_{CNT}} \quad (2)$$

where q is the charge of an electron, a = 2.49Å is the CNT atomic distance and V_π= 3.033eV is the carbon π to π bond energy. The sizing of a CNFET is equivalent to adjusting the number of tubes. Since the mobility of n-type and the mobility of p-type carriers inside CNTs are identical, the minimum size is 1 for both P-CNFET and N-CNFET. Semiconducting nanotubes have attracted widespread attention of the electron device and circuit designers as a promising channel material for high-performance transistors. A typical structure of a MOSFET-like CNTFET in planar and co-axial form is illustrated in Figure 2 [16]-[18].



(a)



(b)

Figure 2. The CNTFET Structures: a) planar, b) coaxial

3. The Conventional 6T SRAM Cell

Static Random Access Memory (SRAM) is a type of semiconductor memory. SRAMs are a major component of digital systems such as Embedded systems, microprocessors, reconfigurable

hardware, field programmable gate arrays just to name a few. Fast memory access times and design for density have been two of the most important target design criteria for many years, however with device scaling to achieve even faster designs; power supply voltages and device threshold voltages have scaled as well leading to degradation of standby power and static noise margins of memories.

Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote “0” and “1”. Two additional access transistors help controlling the access to the cross coupled unit formed by the inverters during read and write operations. So typically it takes six transistors to store one memory bit. The design of a basic SRAM cell is shown in Figure 2. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6 which allow the access of the memory cell to the bit lines: ‘BL’ and ‘BLbar’. They are used to transfer data for both read and write operations. The presence of dual bit lines i.e. ‘BL’ and ‘BLbar’ improves noise margins over a single bit line. The symmetric circuit structure allows for accessing a memory location much faster than in a DRAM. Also the faster operation of an SRAM over DRAM can be attributed to the fact that it accepts all address bits at a time where as DRAMs typically have the address multiplexed in two halves, i.e. higher bits followed by lower bits.

The SRAM is operated in one of the three modes namely WRITE, READ and IDLE operations. The start of a write cycle begins by applying the value to be written and its complement to the bit lines. In order to write a ‘0’, we would apply a ‘0’ to the bit line ‘BL’ and its complement ‘1’ to the ‘BLbar’. A ‘1’ is written by inverting the values of the bit lines i.e by setting ‘BL’ to ‘1’ and ‘BLbar’ to ‘0’. ‘WL’ is then made high and the value that is to be stored is latched in. The input-drivers of the bit lines are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Proper operation of an SRAM cell however needs careful sizing of the transistors in the unit. The read cycle is started by asserting the word line ‘WL’, enabling both the access transistors M5 and M6. The second step occurs when the values stored in ‘Q’ and ‘Qbar’ are transferred to the bit lines ‘BL’ and ‘BLbar’ through M1 and M6. On the BL side, the transistors M4 and M5 pull the bit line towards V_{DD} (when a “1” is stored at Q). If the content of the memory was a 0, the reverse would happen and ‘BLbar’ would be pulled towards 1 and ‘BL’ towards 0. For the idle state, the word line is not asserted and the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters INV1 and INV2 formed by M1, M2 and M3 M4 will continue to reinforce each other as long as they are disconnected from any external circuits [19].
The operation of CNFETs based memories is very similar to that of CMOS except for minor differences in device orientation. One such difference being that the source and drain terminals of a CNFET are not interchangeable as is the case with MOSFET devices. Care must therefore be taken to orient the transistors in a memory cell in a manner that will ensure correct transmission of logic levels.

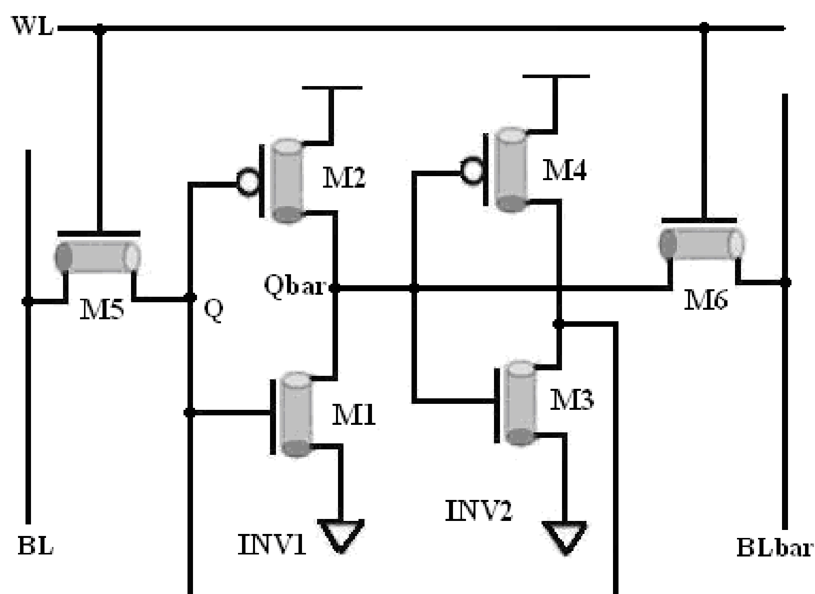


Figure 3. The basic 6T CNTFET SRAM Cell

4. The Proposed CNTFET SRAM Cell

Authors in [20] proposed a 7T cell to reduce the activity factor α for reduction of dynamic power while writing to a cell. The 7-transistor SRAM cell based on CNTFETs has been designed to improve the read cycle and reduce dynamic power. The transistor level schematic of this cell appears in Figure 3. It adds a transistor M7 in the feedback loop and a separate read line 'ReadBit' from the word line 'WriteBit' of the 6-transistor cell.

The four transistors M1, M2 and M3, M4 in the centre form two cross-coupled inverters INV1 and INV2. Due to the feedback structure, a low input value on the first inverter INV1 will generate a high value on the second inverter INV2, which amplifies and stores the low value on the second inverter INV2. Similarly, a high input value on the first inverter INV1 will generate a low input value on the second inverter INV2, which feeds back the high input value onto the first inverter INV1. Therefore, the two inverters INV1 and INV2 will store their current logical value, whatever value that is. But in this circuit feedback connection is established through an extra nMOS transistor M7. The circuit stores data at a node 'Q' and its complement at a node 'Qbar'. This circuit uses two separate transistors M5 and M6 to write and read data from memory cell. To write data into cell 'WriteSelect' signal is used. To read data from the cell 'ReadSelect' signal is used.

This proposed 7T CNTFET SRAM cell depends on cutting off the feed back connection between the two inverters, INV1 and INV2, before a write operation. The feedback connection and disconnection is performed through an extra nMOS transistor M7. During write operation M7 is OFF and during read operation it is ON. The cell depends only on 'WriteBit' to perform a write operation as shown in Figure 3.

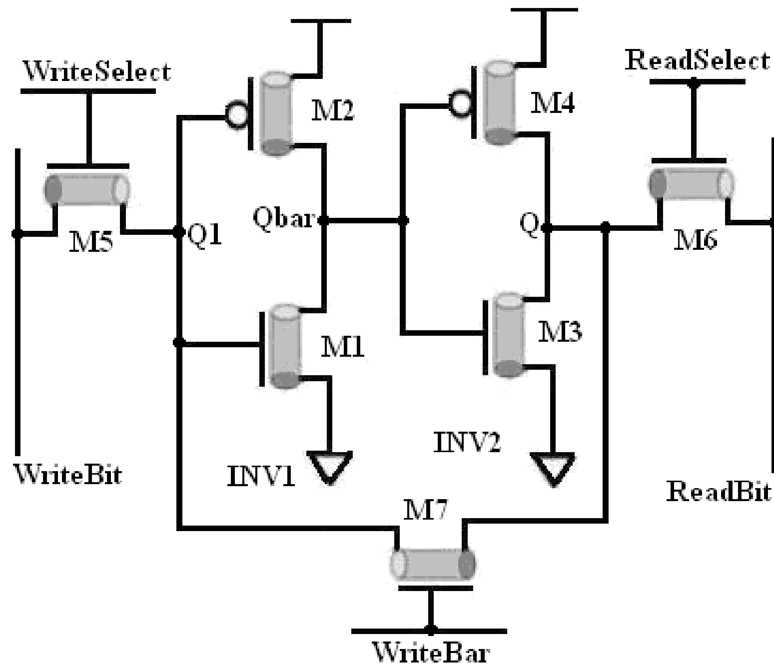


Figure 4. Proposed 7T CNTFET SRAM Cell

4.1. Read and Write Operation

Read operation starts by turning on a transistor M6 using a signal ‘ReadSelect’ and turning off the transistor M5. During this operation feedback path is connected by turning on ‘WriteBar’ signal. Then the stored data at a node ‘Q’ can be read at ‘ReadBit’. The read cycle is improved based on two aspects of the cell operation namely the ability to pre-charge the read bit line ‘ReadBit’ irrespective of the activity of the write bit line ‘WriteBit’ and device sizing of the read zero path with the pull-down transistor M3 of the second inverter made 8 times larger than the M6 to provide a fast path to ground.

The write operation starts by turning M7 off to cut off the feedback connection, thereby allowing for a fast transfer of the logic value from the write bit line ‘WriteBit’ into the memory cell. ‘WriteBit’ carries the input data, M5 is turned on by using a signal ‘WriteSelect’, while M6 is kept off as shown in Figure 3. The 7T SRAM cell looks like two cascaded inverters, INV1 followed by INV2. M5 transistor transfers the data from ‘WriteBit’ to Q1 which drives INV1, M1 and M2, to develop ‘Qbar’. Similarly, ‘Qbar’ drives INV2, M3 and M4, to develop ‘Q’, the cell data. Then, M5 is turned off and M7 is turned on to reconnect the feed back link between the two inverters to stably store the new data. Dynamic power reduction would result from the reduced switching activity during memory accesses. The ‘WriteBit’ line does not have to be pre-charged in preparation for the read operation and a write operation affects only a single bit line of the cell compared to both for the 6-transistor memory cell.

5. RESULTS AND DISCUSSIONS

The 7T SRAM Cell based on CNTFET is designed at 32nm technology. Another 6T SRAM cell at 32nm technology is also designed for comparison. This circuit is simulated in HSPICE using Stanford CNTFET model at 32nm feature size with supply voltage V_{DD} of 0.9V [21].
The following technology parameters are used for simulation of 6T and 7T SRAM cells using CNTFET Technology [22-24]:

- Physical channel length (L_channel) = 32.0nm
- The length of doped CNT source/drain extension region (L_sd) = 32.0nm
- Fermi level of the doped S/D tube (Efo) = 0.6 eV
- The thickness of high-k top gate dielectric material (T_{ox}) = 4.0nm
- Chirality of tube (m, n) = (19, 0)
- CNT Pitch = 10nm
- Flatband voltage for n-CNTFET and p-CNTFET (V_{fbn} and V_{fbp}) = 0.0eV and 0.0eV
- The mean free path in intrinsic CNT (L_{ceff}) = 200.0nm
- The mean free path in p+/n+ doped CNT = 15.0nm
- The work function of Source/Drain metal contact = 4.6eV
- CNT work function = 4.5eV

The sizing of a CNFET is equivalent to adjusting the number of tubes. In this 7T CNTFET SRAM Cell Circuit design we have chosen 3 tubes for M1, M2 and M5 transistors, 1 tube for M4 and M7 transistors, 8 tubes for M3 transistor and 6 tubes for M6 transistor for proper functionality of the cell.

Read delay, defined as the time delay between 50% ‘ReadSelect’ activation to when the sense amplifier has reached 90% of its full swing, should be measured at the worst case scenario. Because of the asymmetry of the proposed 7T cell, the read path when Q =”1”, represents the worst case read delay. The read cycle improvement is based on two aspects of the memory cell operation. Firstly the ability to pre-charge ‘ReadBit’ line irrespective of the activity of the ‘WriteBit’ line and secondly device sizing of the read zero path containing transistors M3 and M6, with the pull-down transistor M3 of the second inverter INV2 made 8 times larger to provide a fast path to ground.

For a write operation, the write delay is defined as the time between the activation 50% of ‘WriteSelect’ to when ‘Q’ is 90% of its full swing. The write delay is approximately equals the propagation delay of INV1 and INV2.

Because the write power consumption for a conventional 6T cell is independent of the input data, the activity factor of discharging the bit line α is equal to 1, because for any input data one of the bit lines is discharges. But this 7T CNTFET SRAM cell design uses only one bit line for writing and the discharging of the bit line ‘Writedata’ depends on the stored data, so the activity factor α is definitely less than 1. Dynamic power reduction would result from the reduced switching activity during memory accesses. The ‘WriteBit’ line does not have to be pre-charged in preparation for the read operation and a write operation affects only a single bit line of the cell compared to both for the 6T CNTFET SRAM cell.

The 7T CNTFET SRAM circuit is successfully simulated using HSPICE and simulation waveforms are measured using the HSPICE Cscope. The Simulation waveforms for successive Writes and Reads are shown in Figure 4 and the simulation results of Dynamic Power and Read Delay are tabulated in Table 1. This circuit is verified by successfully writing the data “1010101” into the cell using ‘WriteSelect’ and ‘WriteBit’ signals, as shown by the waveform Q and

correspond successfully reading of the data using the signal 'ReadSelect' as shown by the signal 'ReadBit' in Figure 4. The Dynamic Power and Read delay of 7T CNTFET SRAM Cell is reduced by 37.2% and 38.6 % respectively compared to 6T CNTFET SRAM cell
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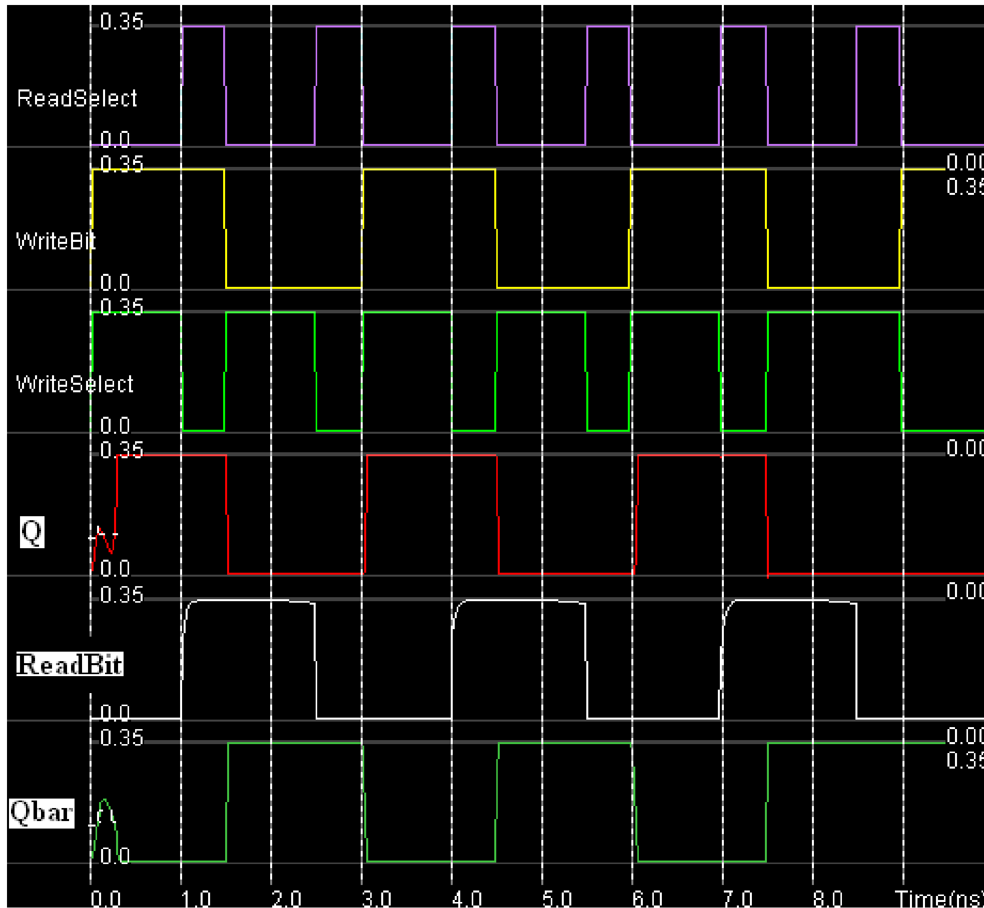

Figure 5. 7T CNTFET SRAM Cell Simulation Results

Table 1. Simulation Results

Sl. No.	**Parameter**	**6T CNTFET SRAM Cell**	**7T CNTFET SRAM Cell**
1	Dynamic Power (µW)	8.75	5.495
2	Read Delay (pS)	5.87	3.604

6. CONCLUSIONS

Carbon-based devices show promising features, so that they are considered as potential candidates to replace silicon based MOSFETs in the future. In this paper a SRAM Cell is designed using CNTFETs at 32nm Technology to reduce write-power dissipation and to reduce the read delay. This 7T CNTFET SRAM Cell circuit uses extra one transistor compared to conventional 6T SRAM Cell to reduce write-power. This circuit is designed and simulated in

HSPICE using Stanford CNFET model at 32nm and simulated results are compared with the simulated results of 6T CNTFET SRAM cell. The Simulation results are tabulated in table 1. The results shows that the Dynamic Power and Read delay of 7T CNTFET SRAM Cell is reduced by 37.2% and 38.6 % respectively compared to 6T CNTFET SRAM cell. The results proved that this circuit reduces write-power and read-delay to the significant effect. This proposed cell can be used in design of CNTFET based low-power SRAM Memories.

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