SELF CORRECTING MEMORY DESIGN FOR FAULT FREE CODING IN PROGRESSIVE DATA STREAMING APPLICATION

Harikishore.Kakarla[1], Madhavi Latha.M[2] and Habibulla Khan[3]

[1, 3]Department of ECE, KL University, Guntur, Andhra Pradesh, India.
[2]Department of ECE, JNTUH, Hyderabad, Andhra Pradesh, India
kakarla.harikishore@kluniversity.in

ABSTRACT

Fault diagnosis in processing digital system application has raised various limiting problems. While basic objective of fault tolerant systems is to minimize the fault occurring in the device, the processing error is an additional error to be considered. Past approaches were observed to be focusing much on internal fault in digital device, the error due to processing and communication is to be developed. In this paper a self correcting approach to memory design based on memory interface is proposed. The error approach observed in case of forwarding binary data to encode, store and retrieve with error free coding is proposed. The Process of memory error free coding results in higher reliability in case of bit and block coding.

KEYWORDS

Memory fault, progressive coding, memory section addressing, bit/block errors.

1. INTRODUCTION

Digital communication system is used to transport an information bearing signal from the source to a user destination via a communication channel. The information signal is processed in a digital communication system to form discrete messages which makes the information more reliable for transmission. During the process of communication there is a need for buffering of data at encoder and decode it back during retrieval. It is observed that during the process of data transferring there is a very heavy probability of data under process may get erroneous due to transition error or stuck at errors. To avoid such errors it is necessary to develop effective and efficient methodologies and tools such as memory test and repair memory built-in self-test (MBIST) generator redundancy scheme evaluator and MBISR schemes for optimal operations. There have been many MBISR architecture schemes reported recently including even a commercial implementation. An optimal solution called comprehensive real-time exhaustive search test and analysis (CRESTA) is equipped with parallel exhaustive analyzers, which is an extreme case due to very high area overhead. To reduce hardware overhead and trades time with area. Heuristic redundancy analysis/allocation (RA) algorithms are widely used to solve the NP-complete problem with reasonable time complexity, area, and repair rate. The tradeoff among repair rate, test time, and area is not straightforward. The spares are normally rows, columns, or words. However, as the size of the embedded static random access memory increases dramatically, recently RA algorithms have been limited to dealing with row/column spares. We do need more sophisticated spares to improve the spare utilization and repair efficiency. Defects can span multiple circuit elements and have been shown to occur in clusters on wafers and semiconductor chips (defect clustering), and failures also occur in clusters (failure clustering) with spatial locality that results in serious yield loss. Therefore, there have been numerous studies considering clustered failure repair. Moreover, cluster failures should be repaired together rather

DOI : 10.5121/vlsic.2012.3103

than individually because individual spares are inefficient for clustered failures .This paper present a effective approach of fault tolerance in memory element by an approach of introducing reference memory with an optimal addressing mode, simple and low resource consuming approach. The paper is further presents a store and forwarding communication approach for real time communication approach. The proposed self correcting approach for memory element is presented. The developed design and observations made are presented in the conclusion.

2. Progressive Data streaming approach

For the progressive processing of digital system, the data are transformed to a sequence of bit stream and passed over a digital processing for encoding, and decoding. In such processing the processed information's are temporarily stored in memory and are fetched when required. A conventional approach to such system is as shown in figure 1. For processing of information bit stream are fed into the encoder to encode the information vector, and the fault secure detector of the encoder verifies the validity of the encoded vector. If the detector detects any error, the encoding operation must be redone to generate the correct codeword. The codeword is then stored in the memory. During memory access operation, the stored codewords will be accessed from the memory unit.

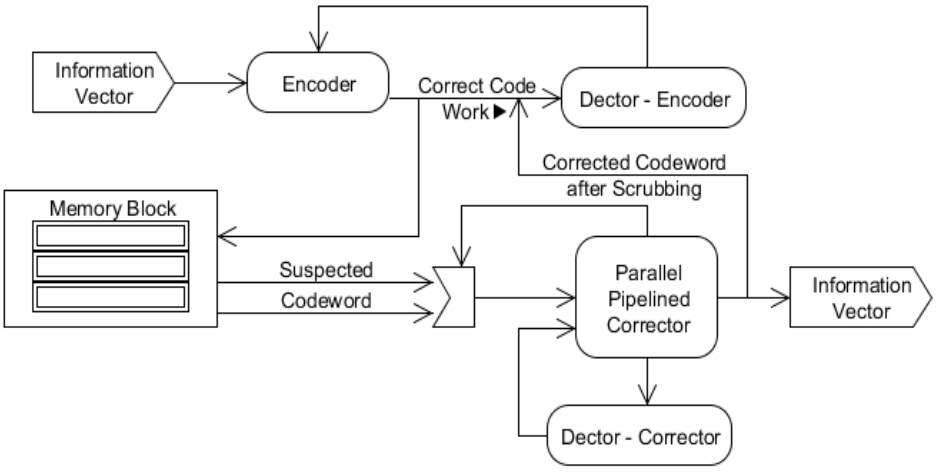

Figure 1: Coding approach for fault free memory interface.

Codewords are susceptible to transient faults while they are stored in the memory; therefore a corrector unit is designed to correct potential errors in the retrieved codewords. In this design all the memory words pass through the corrector and any potential error in the memory words will be corrected. Similar to the encoder unit, a fault-secure detector monitors the operation of the corrector unit. The Data bits stay in memory for a number of cycles and, during this period, each memory bit can be upset by a transient fault with certain probability. Therefore, transient errors accumulate in the memory words over time. In order to avoid accumulation of too many errors in any memory word that surpasses the code correction capability, the system must perform memory scrubbing. Memory scrubbing is the process of periodically reading memory words from the memory, correcting any potential errors, and writing them back into the memory. To perform the periodic scrubbing operation, the normal memory access operation is stopped and the memory performs the scrub operation. This approach is effective for processing error minimization in encoding, decoding and storage operation. While the approach is efficient in correcting coding errors, permanent stuck faults in memory blocks are not removed. Hence to achieve the objective of fault tolerance in case of permanent faults a block repair fault tolerant architecture is proposed memory section addressing (MSA) is proposed for high capacity interfacing memories.

3. Memory section addressing (MSA) approach

High density and high capacity memories are important components for successful implementation of system-on-chip designing. The main contributive part is the storage element as all the processed data are buffered or retrieved from these memories only. Since they occupy a large portion of area they have higher complexity and have higher fault possibility. The fault is due to the stuck faults occurred during fabrication process. These stuck faults are permanent faults and need to be overcome. As memories are very large a replacement of such device under fault condition would not be a cost effective approach. To achieve a fault tolerant mechanism a memory section addressing (MSA) is proposed, based on the secondary memory defining and addressing approach. The proposed approach divide the memory cell array into blocks and secondary memory slots are added at the block level as shown in the figure 2.

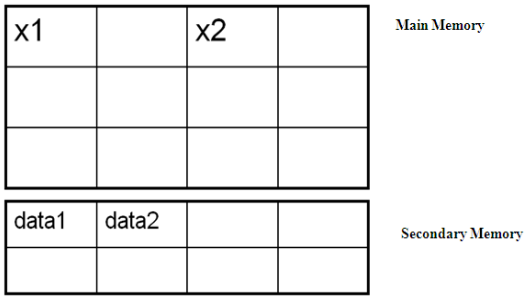

Figure 2: Memory Section Approach.

To evaluate the fault location the main memory unit is synchronized with the secondary memory locations. While storing a data in a fault location, if a fault is observed the fault bit or word is passed to secondary location and a address for faulty block mapping information is used. The proposed Block mapping approach is as shown in figure 3.

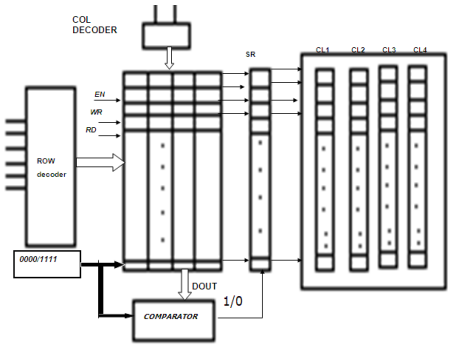

Figure 3: Faulty block mapping addressing approach.

For the processing of fault diagnosis a redundant fault tolerance system is developed. The approach for fault testing is as outlined. To process the fault detection initially the memory is filled with all 1's the output DOUT is compared with 1's in block wise so that if any mismatch is found the comparator will set the status signal to be 1 to indicate the fault in the memory location . Then the address of the faulty block memory location is stored in a register. Similarly the main memory is tested for stuck_at_1 faults by filling all 0's into the main memory and comparing it with all 0's in block wise. The faulty addresses of the main memory are buffered and stored in a defined mapping registers. The addressing of such a faulty memory is as shown in figure 4.

	col0	col1	col2	col3
row0	0000	0000	0001 x	0001 x
row1	0000	0000	0000	0000
row2	0000	0000	0001 x	0000
row3	0000	0000	0000	0000
row4	0000	0000	0000	0001 x
row5	0000	0000	0000	0000
	0000	0000	0000	0001 x

Figure 4: Fault coding addressing for a fault memory location.

For the integration of fault tolerance in memory interface the system developed is as presented in figure 5 below.

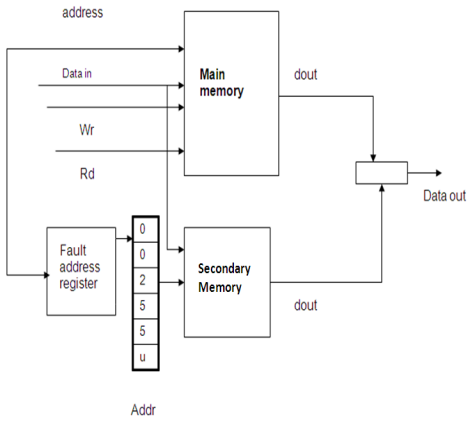

Figure 5: Proposed MSA Fault Tolerant system.

When a main memory access is requested, the word address of the memory cells is compared with faulty cell address. If a match is found then the write or read operation is done through the corresponding spare memory. Otherwise normal read or write operation is done on the location of that address.

4. RESULT OBSERVATION

To evaluate the operational performance the memory addressing allocation of fault location has been done at bit level and block level. In bit level location allocation in secondary location is done for each bit in the memory array and is tested and locations are allocated in bit wise manner. This increases the repair rate of memory, with minimum processing overhead. In word level, full secondary row is allocated even for a single bit fault in the memory. The observations made for such system is as outlined below,

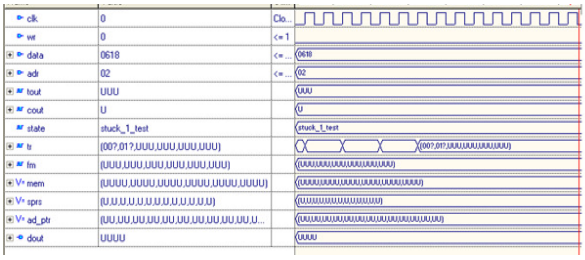

Figure 6: The timing simulation result for stuck fault at logic High.

Figure illustrates the timing simulation result for the developed approach. For the evaluation of the suggested approach a stuck at fault is modeled, and the result observed for the fault condition is seen.

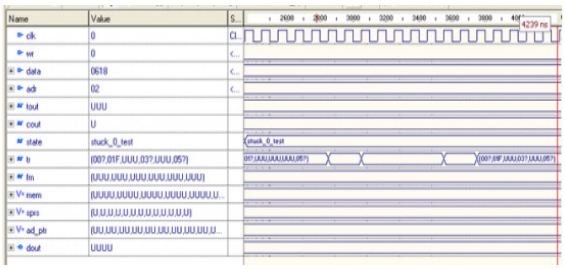

Figure 7: The timing simulation result for stuck fault at logic Low.

A fault condition for stuck at zero condition is also derived and the observations were made to evaluate the memory operation at stuck -0 operation.

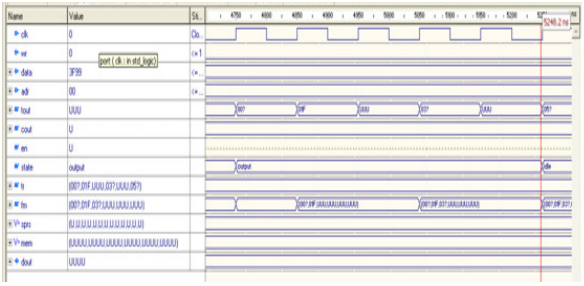

Figure 8: Simulation result illustrating faulty addressing mode.

For evaluating the operational functionality the memory were addressed with fault location, and is tested for data retrieved for algorithm reliability. The approach shows that even with the fault addressing the reading information is observed with correct data retrieved due to proposed approach.

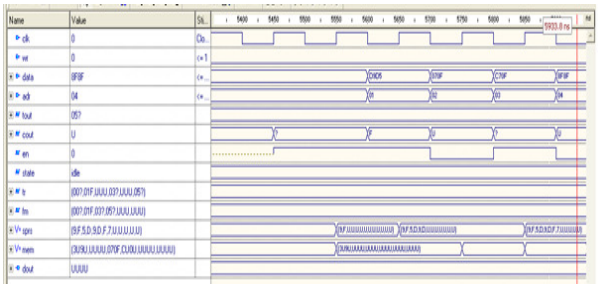

Figure 9: Result observation for fault memory and MSA operation.

The observation with the incorporation of MSA approach is observed. The fault condition is observed to be overcome with the incorporation of MSA approach.

Figure 10: Result observation for read operation at addressed location.

The result observation for developed coding approach with address location is developed. The observation for read operation for the addressed location is seen and it is observed that even with error coding the approach overcome the memory errors.

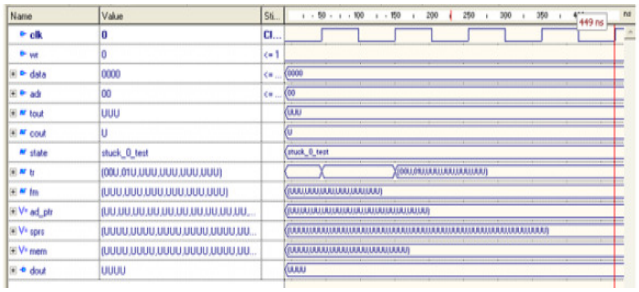

Figure 11: Row level redundancy coding for block errors.

Row based error coding is evaluated in the designed memory unit. The effectiveness of the algorithm over block error estimation is evaluated, and the performance is tested for error in row level error in multiple locations.

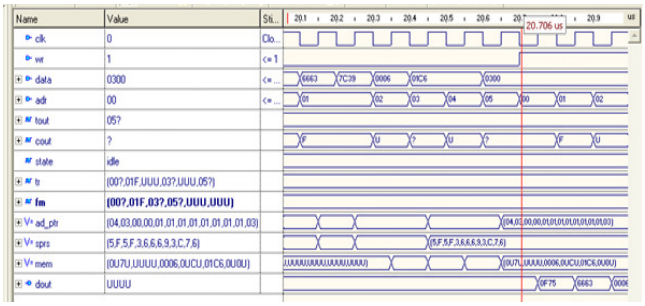

Figure 12: Bit level redundancy coding for 1-bit error.

The proposed approach is also evaluated for a bit error, where a stuck-at-1 and stuck-at-0 error is evaluated at single bit locations. The effectiveness of the proposed coding is developed for block and bit based errors.

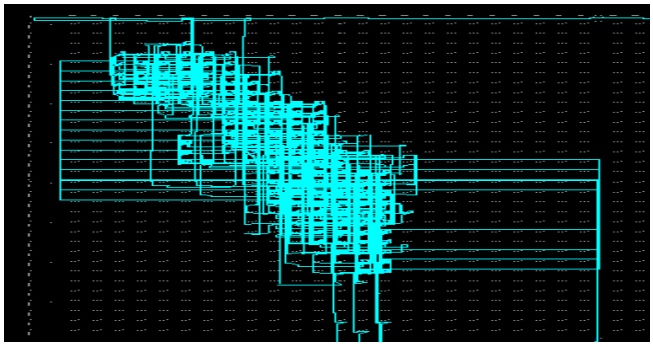

Figure 13: Logical placement for the developed logical unit.

For the evaluation of the developed approach of a targeted FPGA unit, the developed HDL definition is targeted over Xilinx Vertex device and the level of implementation and area coverage is observed as illustrated in figure 13.

Design Statistics

# IOs	: 26
Cell Usage	
# BELS	: 7087
Macro Statistics	
# Registers	: 951
Maximum operating Frequency	: 267.188MHz

The implementation specification of the developed system is obtained is as outlined above. The Maximum operating frequency for the developed system is found to be 267.188MHz and the logical block set required for implementation is found to be 7087 BELs.

5. Conclusion

An efficient error free coding scheme based on memory section addressing is proposed. The incorporation of the developed approach for error minimization is observed to be effective in removing error in memory location which is fixed stuck faults. The developed method is optimal in usage of error free data retrieval for progressive store and forward operation in real time applications. The approach of encoding error minimization, decoding error minimization and memory error minimization is proposed in this paper to achieve optimized error minimization in memory based data streaming.

REFERENCES

[1] L.T. Wang, C.-W. Wu, and X. Wen, Design for Testability: VLSI Test Principles and Architectures. San Francisco, CA: Morgan Kaufmann, 2006.

[2] International Technology Roadmap for Semiconductors (ITRS), Semiconductor Industry Association, Sematech, Hsinchu, Taiwan, Dec. 2009.

[3] Gary C.T. Chow, K.W. Kwok, Wayne Luk, and Philip H.W. Leong. Mixed precision comparison in reconfigurable systems. In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 17–24, 2011.

[4] C. Cheng, C.-T. Huang, J.-R. Huang, C.-W. Wu, C.-J. Wey and M.-C. Tsai, "BRAINS: A BIST compiler for embedded memories," in Proc. IEEE Int. Symp. DFT VLSI Syst., Oct. 2000, pp. 299–307.

[5] R.-F. Huang, J.-F. Li, J.-C. Yeh and C.-W. Wu, "Raisin: Redundancy analysis algorithm simulation," IEEE Des. Test Compute. vol. 24, no. 4, pp. 386–396, Jul.–Aug. 2007.

[6] M.-S. Lee, L.-M. Denq and C.-W. Wu, "BRAINS+: A memory built-in self-repair generator," in Proc. 1st VTTW, Jul. 2007, Paper 1.2.

[7] T. Kawagoe, J. Ohtani, M. Niiro, T. Ooishi, M. Hamada, and H. Hidaka, "A built-in self-repair analyzer (CRESTA) for embedded DRAMs," in Proc. ITC, 2000, pp. 567–574.

[8] X. Du, S. M. Reddy, W.-T. Cheng, J. Ray hawk, and N. Mukherjee, "At speed built-in self-repair analyzer for embedded word-oriented memories," in Proc. 17th Int. Conf. VLSI Des., 2004, pp. 895–900.

[9] P. Ohler, S. Hellbrand, and H. J. Wunderlich, "An integrated built-in test and repair approach for memories with 2-D redundancy," in Proc. 12th IEEE ETS, May 2007, pp. 91–96.

[10] J. Lee, K. Park, and S. Kang, "An area-efficient built-in redundancy analysis for embedded memories with optimal repair rate using 2-D redundancy," in Proc. ISOCC, 2009, pp. 353–356.

[11] S.-K. Lu and C.-H. Hsu, "Built-In self-repair for divided word line memory," in Proc. IEEE ISCAS, May 2001, pp. 13–16.

[12] V. Schober, S. Paul, and O. Picot, "Memory built-in self-repair using redundant words," in Proc. ITC, 2001, pp. 995–1001.

[13] Elaine Ou and Philip Leong. Emerging non-volatile memory technologies for reconfigurable architectures. In IEEE International Midwest Symposium on Circuits and Systems (Special Session on Reconfigurable Architecture), pages 1–4, 2011.

[14] M.Karmani, C.Khedhiri and B.Hamdi, "Design and test challenges in Nano-scale analog and mixed CMOS technology", International Journal of of VLSI design & Communication Systems, 2011.

[15] D. M. Blough, "Performance evaluation of a reconfiguration-algorithm for memory arrays containing clustered faults," IEEE Trans. Reliable., vol. 45, no. 2, pp. 274–284, Jun. 1996.

[16] T. Kirihata, Y. Watanabe, W. Hing, J. K. DeBrosse, M. Yoshida, D. Kato, S. Fujii, M. R. Wordeman, P. Poechmueller, S. A. Parke, and Y. Asao, "Fault-tolerant designs for 256Mb DRAM," IEEE J. Solid-State Circuits, vol. 31, no. 4, pp. 558–566, Apr. 1996.

Authors

1. **Harikishore.Kakarla** was born in Vijayawada, Krishna (Dist.), Andhra Pradesh, India. He received B.Tech in Electronics and Communication Engineering from, JNTU, Hyderabad, Andhra Pradesh, India, M.Tech from SKD University, Anantapur, Andhra Pradesh, India. He is pursuing Ph.D in the area of VLSI in KL University, Vijayawada, Andhra Pradesh, and India. Presently he is working as a Assistant Professor, Department of Electronics and Communication Engineering, KL University, Guntur, Andhra Pradesh, India, where he has been engaged in teaching, research and development of Low-power, High-speed CMOS VLSI SoC, Memory Processors LSI's, ASIC Fault Testing, Embedded Systems and Nanotechnology. He has published 08 International Journals and 01 National Conference Level.
E-Mail: Kakarla.harikishore@kluniversity.in

2. **Madhavi Latha. M** was born in Guntur (Dist.,), Andhra Pradesh, India. She received B.E in Electronics and Communication Engineering from Acharya Nagarjuna University, Guntur, Andhra Pradesh, India, M.Tech from JNTU, Hyderabad, India. She received Ph.D degree in Engineering from JNTU, Hyderabad, Andhra Pradesh, India. Currently, she is working as Professor and Head for Department of Electronics and Communication Engineering, JNTUH, Hyderabad, Andhra Pradesh, India and currently working in VLSI field. Her research interest includes design of Low power and mixed signal

circuits. She has published 34 publications in various journals and conferences at National and International level and presented papers in conferences held at Lasvegas, Lousiana, USA and Iunstrruck, Austria presently guiding nine students for Ph.D and one student for M.S. She has conducted ten UGC refresher courses and in DSP, VLSI & Embedded systems, workshops in EDA Tools for VLSI, CMOS & ASIC Designs, MATLAB Programming and Applications.

3. **Habibulla Khan** was born in Vijayawada, Krishna (Dist.), Andhra Pradesh, India. He received B.Tech in Electronics and Communication Engineering from VR Siddhartha Engineering College, Vijayawada, Andhra Pradesh, India, M.Tech from CIT Engineering College, Coimbatore, Tamilnadu, India. He received Ph.D degree in Engineering from Andhra University, Visakhapatnam, Andhra Pradesh, India. Currently, he is working as Professor and Head for Department of Electronics and Communication Engineering, KL University, Vijayawada, Andhra Pradesh, India, and currently working in RADAR and MICROWAVE Engineering field. He has published 20 publications in various journals and conferences at National and International level and presented papers in conferences.