A 3 – 14 GHZ LOW NOISE AMPLIFIER FOR ULTRA WIDE BAND APPLICATIONS

Vaithianathan Venkatesan[1,*], Raja Janakiraman[2] and Srinivasan Raj[3]
Aishwarya Prabakaran[4], Anupreethi Balaji Ranganathan[5], Divya Santhanam[6]

[1,4,5,6]Department of Electronics and Communication Engineering, Sri Sivasubramaniya Nadar College of Engineering, Chennai, India
vaithianathanv@ssn.edu.in[1]
aishwaryaprabakar@gmail.com[4], anupreethi90@yahoo.com[5],
divya.santhanam54@gmail.com[6]
[2]Department of Electronics and Communication Engineering, Anna University of Technology, Tiruchirappali, India
rajajanakiraman@gmail.com[2]
[3]Department of Information Technology, Sri Sivasubramaniya Nadar College of Engineering, Chennai, India
srinivasanr@ssn.edu.in[3]

ABSTRACT

This paper presents an ultra wide band (UWB) low noise amplifier (LNA) with very high gain, better input matching, low noise figure, better linearity and low power consumption. A dual source degenerated resistive current reuse is used as an input stage and a cascode stage with shunt-series peaking is used to enhance the bandwidth and reverse isolation. The proposed LNA achieves a peak power gain of 20.92 dB at 9 GHz while achieving a gain greater than 20.3 dB over 3 – 14 GHz bandwidth. The achieved noise figure is in the range of 3.72 – 4.78 dB, while the input matching and the output matching are kept below –9 dB and –10 dB respectively. The reverse isolation is below –52 dB throughout the entire band. This LNA ensures better linearity with an IIP3 of 4 dBm at 9 GHz with very low power consumption of 5.876 mW at 1 V supply.

KEYWORDS

Dual Source Degenerated Current Reuse, Shunt-Series Peaking, Power Gain, Noise Figure, Input Third Order Intercept Point (IIP_3)

1. INTRODUCTION

In recent years, the academia and industry put forth their interest in UWB technology because this technology offers a promising solution to the radio frequency (RF) spectrum drought by allowing new services to coexist with other radio systems with minimal or no interference [1]. UWB technology is suitable for short range and high speed wireless applications which include cognitive radio, ground penetrating radars, imaging and surveillance systems, safety/health monitoring and wireless home video links, etc.

In February 2002, the Federal Communication Committee (FCC) approved the First Report and Order (R&O) for commercial use of UWB technology under strict power emission limits for various devices. The UWB signals have an average power spectral density limit of –41dBm/MHz in the 3.1 – 10.6 GHz. As defined by the FCC, UWB signals must have bandwidth of more than

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500 MHz or fractional bandwidth larger than 20 percent at all times of transmission. The fractional bandwidth is defined as the ratio of bandwidth to centre frequency as given in equation (1).

$$B_f = \frac{BW}{f_{center}} 100\% = \frac{f_h - f_l}{[f_h + f_l]/2} 100\% \quad (1)$$

where f_h and f_l are highest and lowest cut-off frequencies at the –10 dB point of a UWB pulse spectrum, respectively.

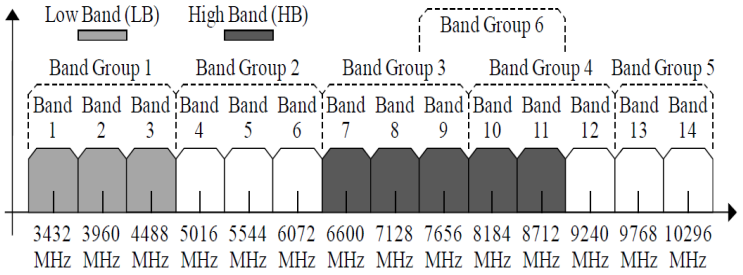

Figure 1. UWB Standards

There are two types of UWB Communication systems based on direct sequence CDMA (DS-CDMA) approach and multi-band orthogonal frequency division multiplexing (MB-OFDM) approach [2]. The DS-UWB is a single-band approach and is fundamentally different from all other communication techniques because it employs extremely narrow RF pulses to communicate between transmitters and receivers. Utilizing short-duration pulses as the building blocks for communication directly generates a very wide bandwidth and offers several advantages, such as large throughput, robustness to jamming, and coexistence with current radio services.

As shown in Figure 1, the entire band is divided into lower and upper bands. The lower band occupies the spectrum in the range of 3.1 GHz to 4.85GHz while the upper band falls in the range of 6.2GHz to 9.7GHz. The DS-CDMA approach also called impulse radio provides data rates from 28 to 1320 Mb/s within the transmission bands from 3.1 to 4.85 GHz and from 6.2 to 9.7 GHz. On the other hand the MB-OFDM based UWB approach uses the whole 7.5 GHz range by dividing it into 14 bands with bandwidth greater than 500MHz as in Figure 1. This is organized in five groups and the operation within the first group is mandatory, while all the other groups are optional. This approach is same as the narrowband frequency-hopping technique where it offers the advantage of avoiding transmission over certain bands, to prevent potential interference.

1.1 Conventional LNA

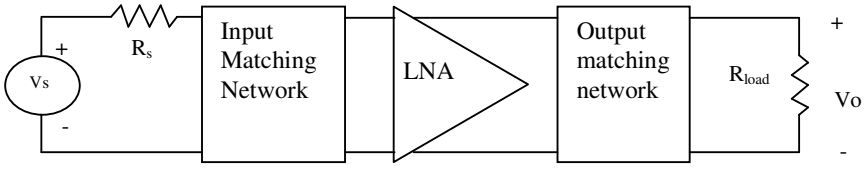

Figure 2. Generalized LNA Topology

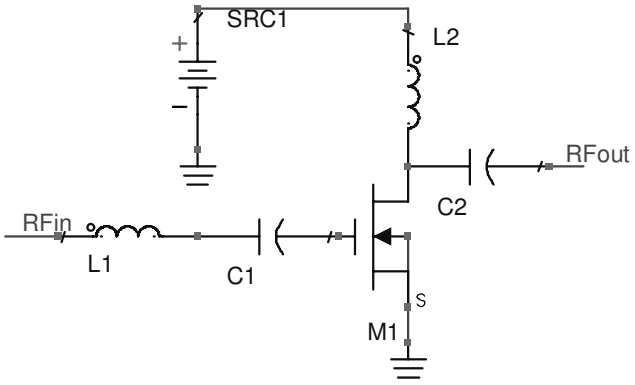

Figure 3. Circuit Diagram of Conventional LNA

Figure 2 shows the block diagram of generalized LNA topology. Input matching and output matching networks are part of LNA. The LNA is to be designed in such a way that it provides maximum gain, low noise figure and good input and output matching. Figure 3 shows the circuit diagram of conventional LNA. L_1 and C_1 are used for input matching. Common source amplifier with inductive peaking is used as a core stage. The use of common source amplifier is to improve the power gain and inductive peaking is used to enhance the bandwidth. The output matching is achieved through capacitor C_2. The results achieved through this circuit are far below the desired level to be compared with the other LNA results. Hence many other techniques have to be adopted to achieve the desired results. One such design is discussed in this paper.

2. PROBLEM STATEMENT

Even though several favourable features are available with the UWB systems, serious challenges still exist for the realization of UWB receiver front-end circuits, especially for the LNA. The received UWB signal exhibits very low Power-Spectral Density (PSD) at the receiver antenna, resulting in a received signal power that is typically three orders of magnitude smaller than that of the narrow-band transmission systems. The ultimate use of the LNA is to amplify the weak signal received from the antenna to acceptable levels while trying to cut out the additional self generated noise [3]. The main figure of merits of LNA are less noise figure, high power gain, good input & output impedance matching, low power consumption, good reverse isolation, acceptable linearity (low distortion) and stability.

Most of the recent works done on the LNA have focused on achieving an optimal trade-off between the LNA parameters through different topologies. The distributed amplifier topology provides moderate flat gain with large power consumption [4]. The CG amplifier topology [5] achieves wideband input matching and better input-output isolation. But it exhibits high noise figure and low power gain. The inductive source degenerated LNA in [6] provides wider bandwidth, high power gain and better noise figure with large power consumption. The resistive shunt feedback amplifier employed in [7] provides a low power gain and high noise figure. The resistive shunt feedback amplifier faces a tough task for providing high gain and low noise figure while achieving better input impedance matching. From the survey of recent works on LNAs, it is learnt that a low power LNA is required while providing high gain, low noise figure and better linearity.

In this paper, a resistive current reuse UWB LNA with dual source degeneration to obtain noise and input matching is presented. The shunt-series peaking technique is used to enhance the bandwidth. Chapter 3 explains the operation of the proposed LNA. The proposed LNA is designed using 90nm CMOS technology and its various performance parameters are analyzed

using Agilent ADS simulator. Chapter 4 presents the simulation results and compares with the recently reported LNAs. Chapter 5 presents the conclusion.

3. PROPOSED LOW NOISE AMPLIFIER

The circuit diagram of the proposed LNA is shown in the Figure 4. The LNA circuit is composed of three stages namely dual-source degenerated resistive current reuse, cascode amplifier with shunt-series inductive peaking and common drain amplifier.

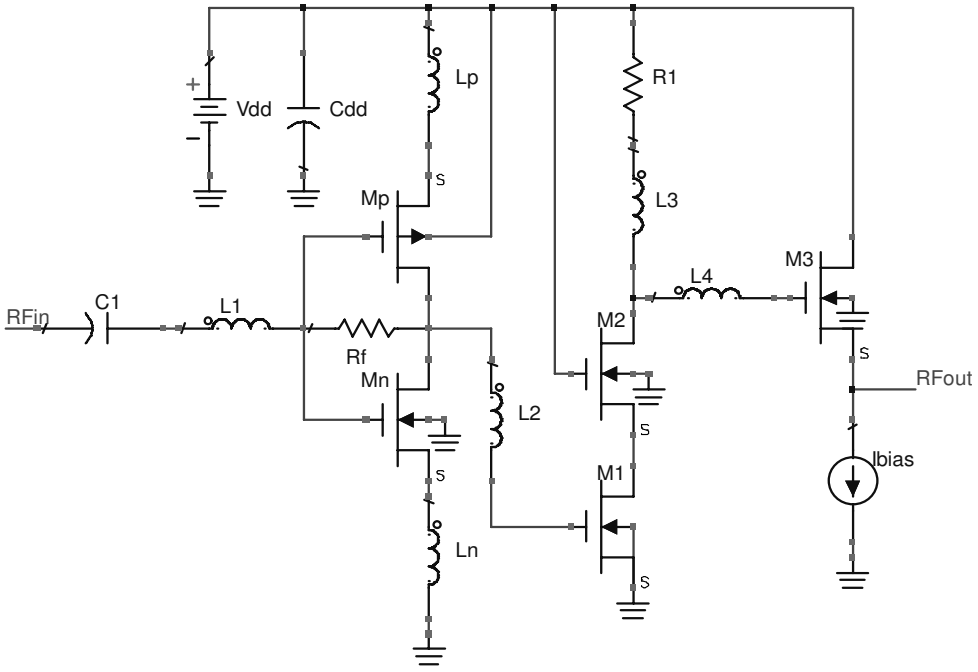

Figure 4. Proposed LNA Circuit

3.1. Input Stage

Figure 5 shows the small signal equivalent circuit of the input stage. The resistive current reuse topology, when compared with the other reported topologies, provides high gain, low noise figure with low power dissipation and high linearity. The high gain is achieved by increased transconductance provided by this topology. The overall circuit transconductance is increased by stacking NMOS and PMOS in complementary push-pull configuration as shown in Figure 4. The series L1 and C1 along with source degenerated inductors and parasitic capacitances of the transistors forms a multiple LC network which is useful for wideband input matching to 50Ω. The same DC current is used in the two transistors leading to low power consumption. The main drawback of this topology is the low 3-dB bandwidth attained.

3.1.1. Input Matching

The current reuse topology uses two common source amplifiers with voltage shunt feedback technique. The input impedance of the first stage has two components, one due to the feedback and the other due to the inductively degenerated common source amplifier as shown in (2). The input impedance can be calculated as:

$$Z_{in} = sL_1 + \frac{1}{sC_1} + Z_s \parallel Z_f \tag{2}$$

$$Z_s = \left(sL_n + \frac{1}{sC_{gsn}} + \frac{g_{mn}L_n}{C_{gsn}} \right) \parallel \left(sL_p + \frac{1}{sC_{gsp}} + \frac{g_{mp}L_p}{C_{gsp}} \right) \tag{3}$$

$$Z_f = \frac{R_f + \left(\frac{1}{g_{mn}} \parallel r_{on} + sL_n \right) \parallel \left(\frac{1}{g_{mp}} \parallel r_{op} + sL_p \right)}{1 + g_m \left[R_f + \left(\frac{1}{g_{mn}} \parallel r_{on} + sL_n \right) \parallel \left(\frac{1}{g_{mp}} \parallel r_{op} + sL_p \right) \right]} \tag{4}$$

where Z_s and Z_f are the input impedance of the dual source inductive degeneration part and voltage shunt feedback part.

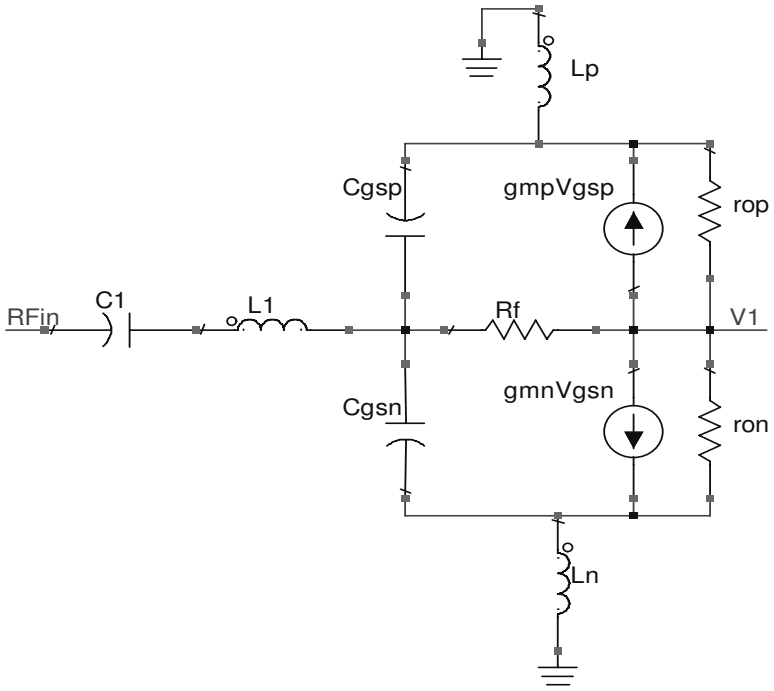

Figure 5. Equivalent Circuit for First Stage

3.1.2. Gain

The gain of the first stage is given by

$$A_{v1} \approx g_m \left[R_f \parallel \left(\frac{1}{g_{mn}} \parallel r_{on} + sL_n \right) \parallel \left(\frac{1}{g_{mp}} \parallel r_{op} + sL_p \right) \parallel Z_{in2} \right] \tag{5}$$

$$g_m = \frac{g_{mn}}{1 + sL_n g_{mn}} + \frac{g_{mp}}{1 + sL_p g_{mp}} \tag{6}$$

$$Z_{in2} \approx sL_2 \tag{7}$$

Thus gain increases with increase in transconductance and with an optimum high value of the feedback resistor R_f as observed from (5).

3.1.3. Noise Figure

The noise figure of the overall LNA is dominated by the noise figure of the first stage which is the resistive current reuse with dual inductive degeneration stage. The noise figure of the first stage is given by equation (8)

$$NF \approx 1 + \frac{R_s}{R_f}\left(1 + \frac{1}{g_m R_s}\right)^2 + \gamma \frac{\omega_0^2 \left(R_s + \omega_T \left(L_n \parallel L_p\right)^2 C_{gs}^{2g}\right)}{g_m R_s} \tag{8}$$

where R_s is the source resistance, R_f is the feedback resistance, g_m is the total transconductance, ω_0 is the resonant frequency of the LC network formed by L_1, L_n, L_p and overall C_{gs} of the two transistors. $\omega_T = \frac{g_m}{C_{gs}}$ is the unity current gain frequency and γ is a process dependent coefficient which is equal to 2/3 for long channel transistors and is a larger value for sub micron transistors. As we can see from the expression, the noise figure is low when the value of R_f is high and when g_m is high. Also from the third term which is a result of the source degeneration we can infer that the Q of the source inductors when high yields a low noise figure**.**

3.1.4. Bandwidth

The 3-dB bandwidth of the first stage is as derived as (9)

$$BW \approx \frac{\left(1 + A_{v1}\right)}{R_f \left(C_{gsn} + C_{gsp}\right)} \tag{9}$$

When the value of R_f is very high, the noise figure is reduced but the bandwidth attained is low. So, an optimum value of R_f is chosen to reduce noise figure. Bandwidth enhancement techniques are used in the next stage to enhance the bandwidth.

3.1.5. Linearity

Linearity is very important criterion since it defines the upper limit of detectable RF input power and sets the dynamic range of the receiver. The parameters used to describe the linearity of an amplifier are 1 dB compression point (P_{1dB}) and IIP_3. This is known as 1 dB compression point and is defined as the level at which the gain drops by 1 dB. This is the result of the saturation effect that begins once the main component of the output signal stops following the input signal with ideal ratio. For the IIP_3, the inter modulation products will increase in amplitude by 3 dB when the input signal is raised by 1 dB. For an UWB LNA only IIP_3 is very important since the UWB signal seldom suffers from gain compression in the LNA due to the low power of the received signal. Designing a LNA with high linearity is a challenging task because of the gain reduction and interference due to other standards. To improve linearity, a complementary push-pull amplifier is used at the first stage. The output of the LNA can be expressed as,

$$Y = b_1 X + b_2 X^2 + b_3 X^3 \tag{10}$$

$$b_1 = \frac{a_1}{1+c_0}\ ,\ b_2 = \frac{a_2}{(1+c_0)^3} \text{ and } b_3 = \frac{1}{(1+c_0)^4}\left(a_3 - \frac{2a_2^2}{a_1}\frac{c_0}{1+c_0}\right) \tag{11}$$

where b_1, b_2 and b_3 are the closed loop gain and second/third order non-linear coefficients respectively. The open loop gain is given by $c_0 = a_1\beta$, where β is the linear feedback factor. IIP_2 and IIP_3 points of the amplifier without feedback and with feedback are given as:

$$A_{IIP_2,amplifier} = \sqrt{\frac{a_1}{a_2}} \tag{12}$$

$$A_{IIP\,2,closedloop\ system} = \sqrt{\left|\frac{b_1}{b_2}\right|} = \sqrt{\left|\frac{a_1}{a_2}\right|(1+c_0)^2} \tag{13}$$

$$A_{IIP_3,amplifier} = \sqrt{\frac{4}{3}\frac{b_1}{b_3}} \tag{14}$$

$$A_{IIP\,3,closedloop\ system} = \sqrt{\frac{4}{3}\frac{b_1}{b_2}} = \sqrt{\frac{4}{3}\frac{a_1}{a_2}\frac{(1+c_0)^3}{\left(1-\frac{2a_2^2c_0}{a_1a_3(1+c_0)}\right)}} \tag{15}$$

A_{IIP3} of the amplifier with feedback is improved by a factor of $(1+c_0)^{3/2}$ when $a_2 \approx 0$. The aim of linearization is to make a_2, a_3 small enough to be negligible. In the proposed LNA, the complementary push-pull amplifier is used to improve linearity. The drain current of NMOS and PMOS are as follows:

$$I_{dn} = a_{1n}V_{gs} + a_{2n}V_{gs}^2 + a_{3n}V_{gs}^3 + \ldots \tag{16}$$

$$I_{dp} = -a_{1p}V_{gs} + a_{2p}V_{gs}^2 - a_{3p}V_{gs}^3 + \ldots \tag{17}$$

$$I_{dout} = I_{dn} - I_{dp} = (a_{1n} + a_{1p})V_{gs} + (a_{2n} - a_{2p})V_{gs}^2 + (a_{3n} + a_{3p})V_{gs}^3 \tag{18}$$

The frequency term $\omega_1 + \omega_2$ in the second order inter modulation product lies within the operating band and hence causes second order non-linearity. This effect can be cancelled by the use of complementary push-pull amplifier. The frequency term in the third order inter-modulation product $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ lies within the operating band and hence causes third order non-linearity. The value of IIP_3 can be improved by increasing a_2 and reducing a_3 as shown in (15).

3.2. Cascode Stage

The equivalent circuit of the cascode stage is shown in Figure 6. An inductor L2 is also used to compensate for the low 3-dB bandwidth due to the load capacitance of the current reuse technique. The cascode stage with shunt –series inductive peaking is used to enhance overall bandwidth. The cascode configuration also provides good reverse isolation and improves the gain.

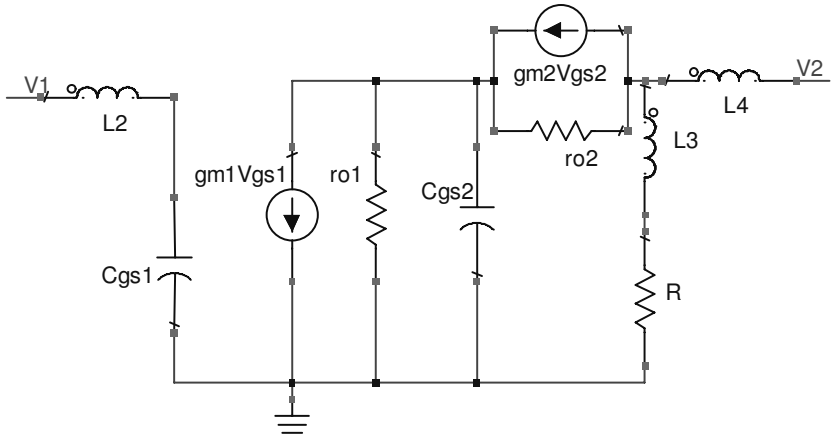

Figure 6. Equivalent Circuit for Cascode Stage

3.2.1. Gain

The gain of the second stage is given by

$$A_{v2} = A_{v21} * A_{v22} \tag{19}$$

$$A_{v21} = -\frac{g_{m1}}{sC_{gs2}} \tag{20}$$

$$A_{v22} = g_{m2}\left(r_{d3} + \frac{(sL_3 + R_1)sL_4}{sL_3 + R_1 + sL_4} \right) \tag{21}$$

3.2.2. Bandwidth

The shunt-series peaking technique is used to enhance the bandwidth of the proposed LNA. The bandwidth enhancement contributed by this configuration can be estimated by analysing the effect of the shunt and series inductors independently. While the circuit is operating only with the load resistor, the power gain is reduced at high frequencies since the impedance of the load capacitance decreases as the frequency increases. An inductor is added in series with the load resistance to compensate this gain roll-off. This is called shunt peaking since the output is taken in shunt with this inductor. The impedance of this inductor increases with the increase in frequency which offsets the decrease in impedance of the load capacitor. Thus it provides almost constant net impedance over wide range of frequency. In the time domain this effect can be analysed using the step response. This extra inductor delays the current flow through the series load resistor, thus making more current available for charging the load capacitor. This improves the rise time and hence the bandwidth. Mathematically the bandwidth enhancement can be expressed as in equation (22)

$$\frac{\omega}{\omega_1} = \sqrt{-\frac{m^2}{2} + m + 1\sqrt{\left(-\frac{m^2}{2} + m + 1\right)^2 + m^2}} \tag{22}$$

where m is the ratio of the RC and L/R time constants and ω_1 is the uncompensated 3-dB bandwidth. The value of m is chosen appropriately for the desired bandwidth with the constraint that peaking should be kept at a minimum so as to achieve a flat gain. For a nominally flat gain m

can be set to 2 which yield a bandwidth 1.85 times greater than the uncompensated case. The output capacitance of the amplifier is separated from the load capacitance using the series inductor thus further enhancing the bandwidth. This is called series peaking. The maximum bandwidth attainable in the series peaking is $\sqrt{2}$ times that of the shunt peaking case. So, by using shunt-series peaking, a very wide bandwidth is obtained.

3.3. Output Stage

The output impedance of the common gate stage in the cascode is high. Hence for output impedance matching, a common drain stage is added. The small signal equivalent circuit of the last stage is given in Figure 7.

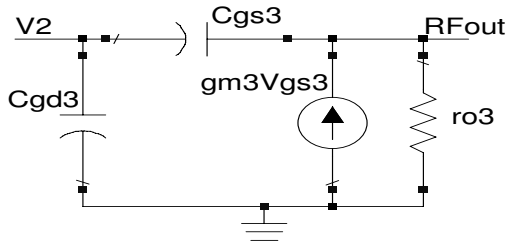

Figure 7. Equivalent Circuit for Output Stage

The gain of the third stage is given by (23)

$$A_{v3} = \frac{g_{m3} r_{03}}{1 + g_{m3} r_{03}} \tag{23}$$

The gain of the common drain amplifier is approximately not equal to 1 even when $g_{m3} r_{03} >> 1$. Hence the third stage gain is not approximately equal to 1. The overall gain of the LNA is calculated after considering the loss contributed by the common drain stage.

4. SIMULATION RESULTS AND DISCUSSION

The proposed LNA circuit is designed with 90 nm CMOS technology and its performance is verified by simulating the circuit using Agilent's ADS simulator. The simulation results of the proposed LNA are given in Fig 8 to 15.

4.1. Power Gain (S_{21})

To compensate noise contribution of subsequent stages in the receiver chain, it is desirable to have a LNA with power gain (S_{21}) more than 20 dB. So, in our circuit by using both current reuse and shunt- series peaking techniques, power gain of more than 20.3 dB is achieved over the entire bandwidth of 3 – 14 GHz while the peak power gain of 20.92 dB is achieved at 9 GHz. This is illustrated in Fig 8.

4.2. Noise Figure (NFmin)

The use of dual-source degenerated resistive current reuse enables us to achieve the noise figure of our proposed circuit in the range of 3.72 - 4.78 dB in the entire band as shown in Figure 9. This ensures that our proposed LNA introduced very little self-generated noise while providing very high gain.

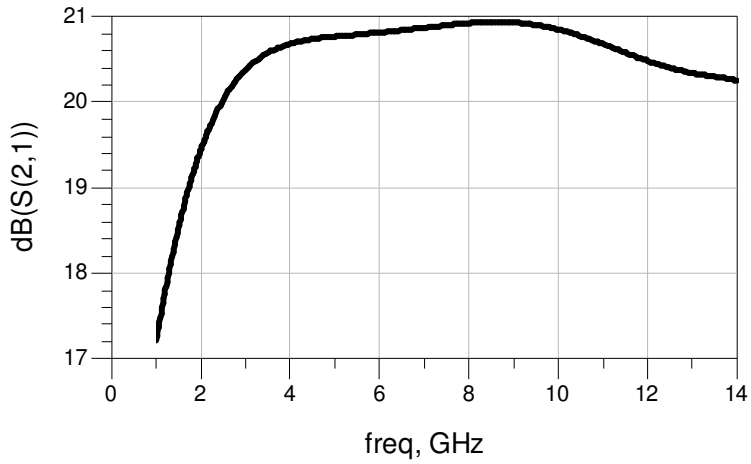

Figure 8. Power Gain (S_{21})

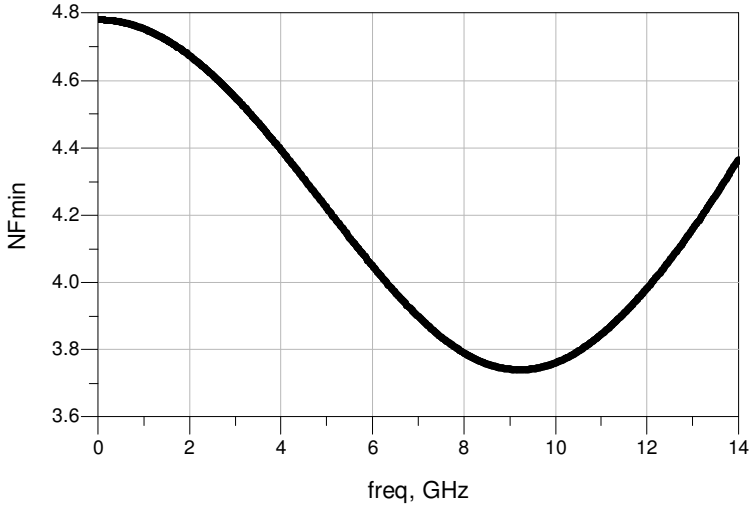

Figure 9. Noise Figure (NFmin)

4.3. Input Matching (S_{11})

In general, it is difficult to achieve both noise matching and power matching simultaneously in an LNA design, since the source admittance for minimum noise is usually different from the source admittance for maximum power delivery. A simultaneous noise figure and input matching approach is achieved by using dual-source degenerated resistive current reuse along with an input filter network. Its typical value should be always less than –10 dB while maintaining lowest noise figure. In our proposed LNA, a minimum of – 25 dB is achieved at 9.5 GHz while less than –9 dB is achieved throughout the bandwidth as presented in Fig 10.

4.4. Output Matching (S_{22})

It is also required to make sure the output matching network does not change the DC bias of the active device. Since source follower is having very low output impedance, it is very easy to achieve the required output matching without any filter network at the output. By using a source

follower as output matching network, a minimum of –33 dB is achieved at 9.3 GHz while less than –10 dB is achieved throughout the bandwidth. This is shown in Fig 11.

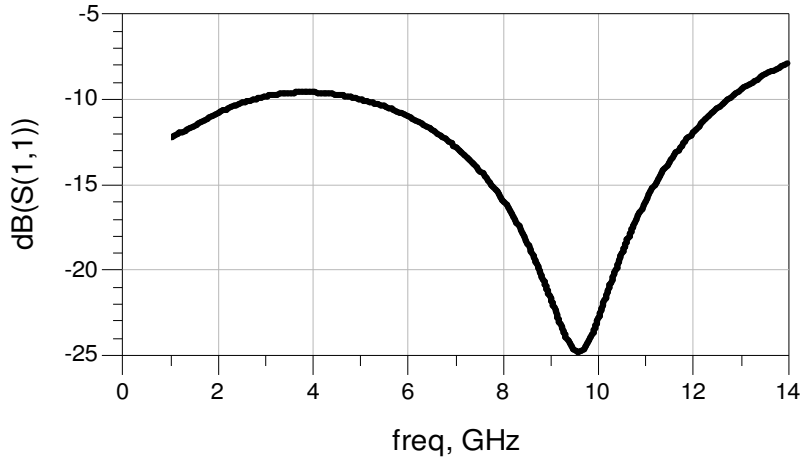

Figure 10. Input Matching (S_{11})

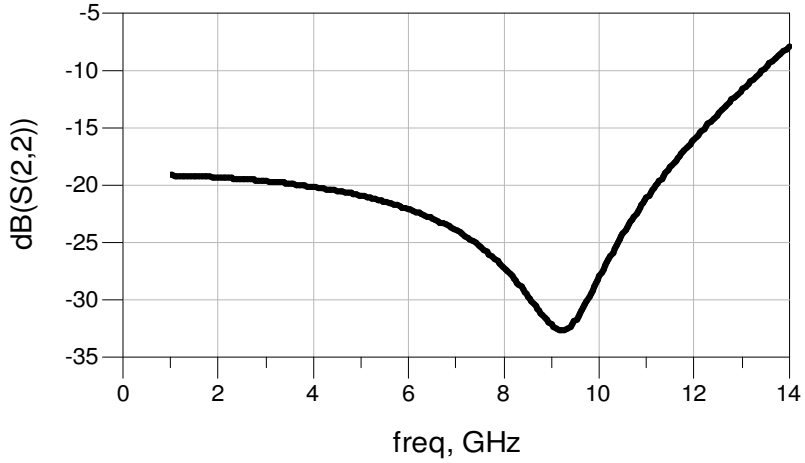

Figure 11. Output Matching (S_{22})

4.5. Reverse Isolation (S_{12})

The input–output isolation (S_{12}) is very important parameter to ensure better stability. Since the cascode stage eliminates the Miller capacitance, it is chosen to provide better isolation. In our proposed circuit, better input–output isolation of less than –52 dB is achieved throughout the bandwidth as shown in Fig 12.

4.6. Stability (StabFact)

The stability of an amplifier, or its resistance to oscillate, is a very important consideration in a design of an LNA and can be determined from the S parameters, the matching networks, and the terminations [16]. The stability factor, `*K*' is calculated over the frequency band 3.1 to 10.6 GHz by using the equation (24).

$$K = \frac{1+|S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad (24)$$

The circuit offers unconditional stability since value of K is greater than 1 which is evident from the simulation results as shown in Figure 13.

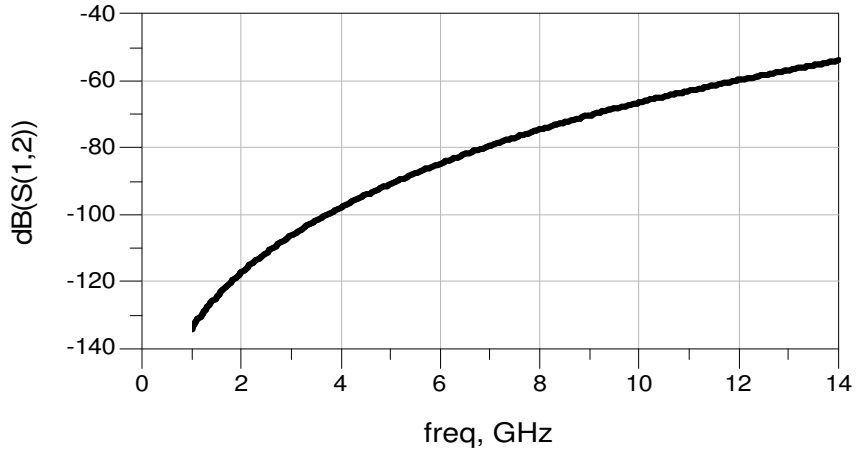

Figure 12. Reverse Isolation (S_{12})

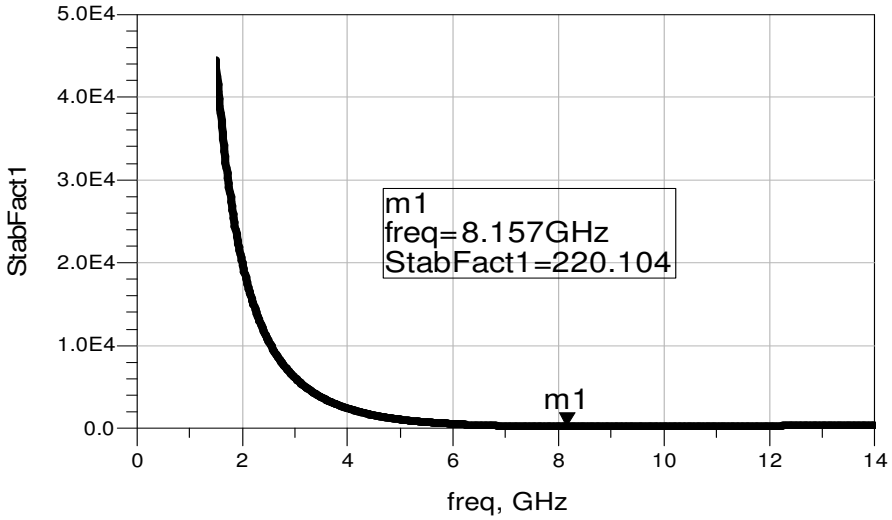

Figure 13. Stability Factor (StabFact)

4.7. Linearity (IIP_3)

The two test zones of – 20 dBm separated by 200 MHz with sweeping frequency range from 2 to 12 GHz are used to measure the linearity of the proposed LNA. From the simulation result as shown in Figure 12, the achieved in band IIP_3 is 4 dBm at the frequency of 9 GHz.

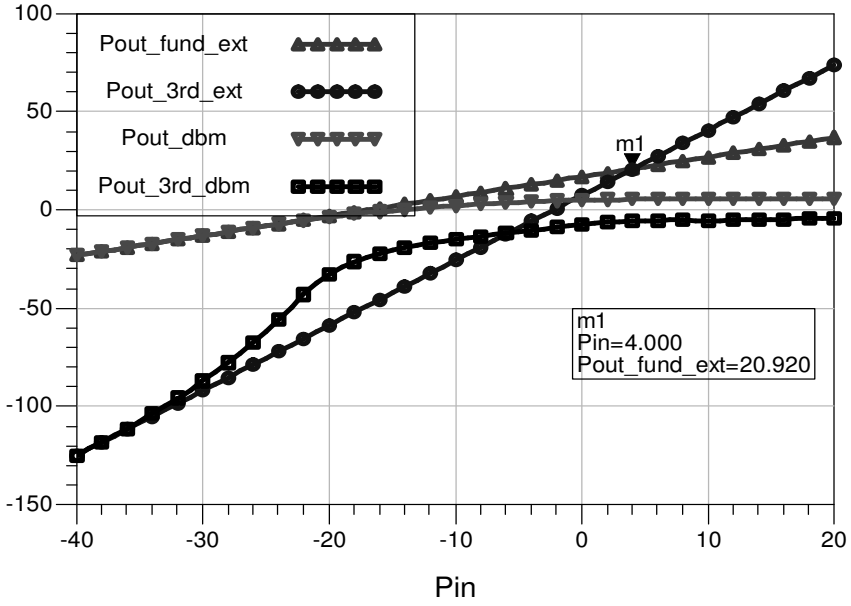

Figure 14. Input Third Order Intercept Point (IIP_3)

freq	I_Probe1.i
0.0000 Hz	5.876 mA

Figure 15. DC Power Consumption at 1V

4.7. Power Consumption

The proposed circuit draws a dc current of 5.876 mA while operating with 1 V power supply which in turn leads to a dc power consumption of 5.876mW.

The Table 1 illustrates the summary of the simulation results for the proposed LNA. The performance of the proposed LNA is compared with the performance of the recently reported LNAs.

Table.1 Simulation Summary & Performance Comparison

Parameters	[8]	[9]	[10]	[11]	This work
Technology	90nm	90nm	90nm	90nm	90nm
3-dB BW (GHz)	2 – 12	14.5	0.5 – 8.2	4 – 8	3 – 14
Gain S_{21}(dB)	12	10	12.5	12.2	20.3
NF (dB)	5.5-8	5.8 – 6	1.9 – 2.6	2 – 2.4	3.72- 4.78
Input Matching S_{11} dB	< –10	< –10	–- 13	< – 5	< – 9
Reverse Gain S_{12}(dB)	-	-	-	-	< – 52
Output Matching S_{22} (dB)	< –10	-	< –10	< – 10	< – 10
Linearity IIP_3 (dBm)	– 4	– 4	–	– 7	4
Power (mW)	17	30	42	9.2	5.876

5. CONCLUSIONS

In this paper, an ultra wide band (UWB) low noise amplifier (LNA) is presented with a dual source degenerated resistive current reuse as an input stage and a cascode stage with shunt-series peaking as a core stage. The cascode stage with shunt-series peaking is used to enhance the bandwidth and reverse isolation. The proposed LNA achieved a peak power gain of 20.92 dB at 9 GHz while achieving a gain greater than 20.3 dB over 3 – 14 GHz bandwidth. The achieved noise figure is in the range of 3.72 – 4.78 dB, while the input matching and the output matching are kept below –9 dB and –10 dB respectively. The reverse isolation is below –52 dB throughout the entire band. This LNA ensures better linearity with an IIP3 of 4 dBm at 9 GHz with very low power consumption of 5.876 mW at 1 V supply. Thus our LNA claims the advantage of having very high gain, better input matching, low noise figure, better linearity and low power consumption.

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Authors

V.Vaithianathan received the B.E degree in ECE from Bharathidasan University, Trichy (TN) in 1997, M.Tech degree in VLSI System Design from Regional Engineering College, Warangal (AP) in 2001. He is currently working as an Assistant Prof in ECE Department, SSN College of Engg, Chennai. His areas of interest are RF Microelectronics, Analog & Mixed VLSI, Low Power VLSI Design and ASIC Design. He has published about 20 papers in national and international conferences and 3 papers in International Journals.

Dr J.Raja obtained his Bachelor's degree in the area of Electronics and Communication Engineering and did his Master's in Control and Instrumentation in the year 1988 and Jan 1992 respectively. He pursued his research in the area of ATM networks. He proposed modification in the ATM switching architectures by employing coding techniques as part of his Ph.D. thesis and obtained his Ph.D. degree in the year 2003.

Currently he is guiding research scholars in the areas of Error Control Coding, WSN Routing Techniques. He has around 18 years of teaching experience. He has taught the courses like Digital Communication Techniques, High Speed Communication Networks, and Communication Switching Systems at both under graduate and post graduate level. Currently he is heading the department of Electronics and Communication Engineering at Anna University, Tirchirappalli, Tamilnadu. He has published about 15 papers in national and international journals and about 35 papers in various conferences.

R Srinivasan obtained his MS (By research) degree from the department of electrical engineering, Indian Institute of Technology, Madras in the year 1998. His MS research thesis was on quantum well lasers and quantum well infrared photo-detectors. He received his Ph.D. degree from the department of electrical communication engineering, Indian Institute of Science, Bangalore in the year 2007. His dissertation was on RF CMOS device engineering and its performance analysis.

To his credit he has 8 journal papers and 8 conference papers. He has experience both in industry as well as in academics. After happy years in industry, he joined as a faculty member in the department of Information Technology, SSN College of Engineering, Kalavakkam - 603110, India in December 2007. His current research areas of interest include VLSI, nano-scale MOSFETs, micro-electronics and analog circuits.

Aishwarya Prabakaran is a final year student of Bachelor of Engineering (B.E.) in Electronics and Communication at SSN College of Engineering, Kalavakkam, Chennai. Her areas of interest are in the field of Analog and Mixed Signal VLSI. She is currently working in the field of LNA design for UWB transceivers, along with Asst. Prof. V. Vaithianathan, of the ECE Dept, SSN College of Engineering, Chennai.

Anupreethi Balaji Ranganathan is a final year student of Bachelor of Engineering (B.E.) in Electronics and Communication at SSN College of Engineering, Kalavakkam, Chennai. Her areas of interest are in the field of Analog and Mixed Signal VLSI. She is currently working in the field of LNA design for UWB transceivers, along with Asst. Prof. V. Vaithianathan, of the ECE Dept, SSN College of Engineering, Chennai.

Divya Santhanam is a final year student of Bachelor of Engineering (B.E.) in Electronics and Communication at SSN College of Engineering, Kalavakkam, Chennai. Her areas of interest are in the field of Analog and Mixed Signal VLSI. She is currently working in the field of LNA design for UWB transceivers, along with Asst. Prof. V. Vaithianathan, of the ECE Dept, SSN College of Engineering, Chennai.